Design of High-speed Front-ends for HV-MAPS

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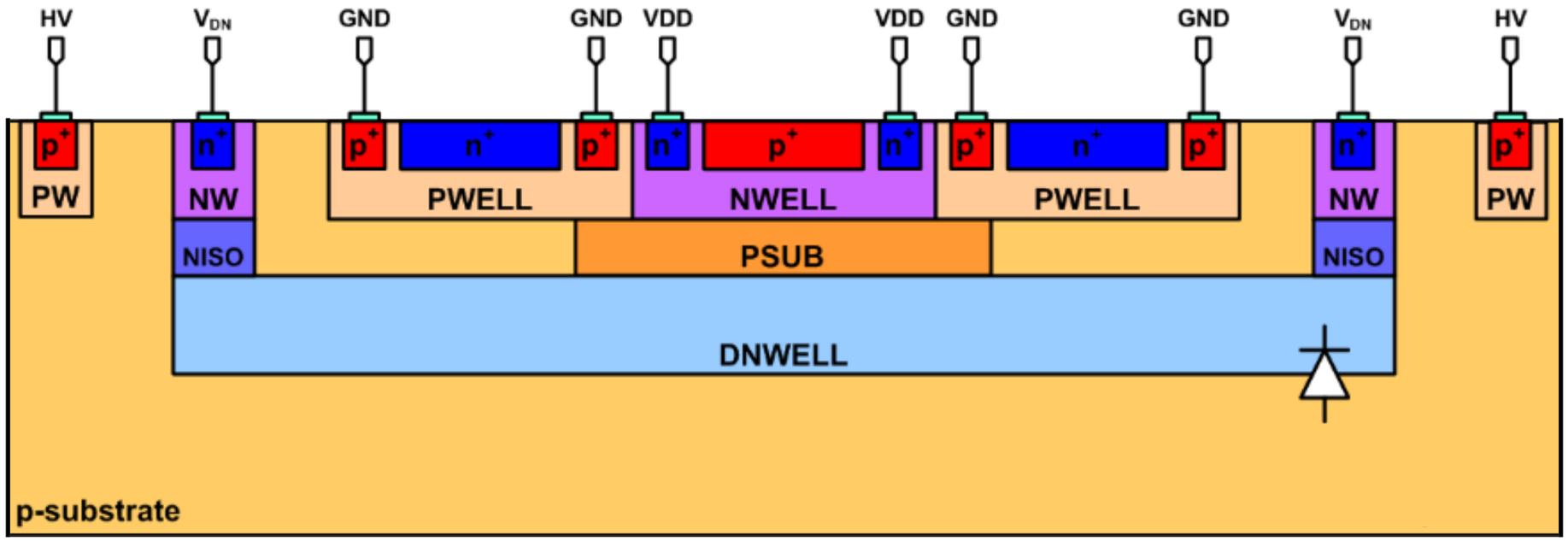
Outline

- **Introduction**
  - HV-MAPS
  - RD50-ENGRUN1
- **Design of high-speed front-ends**
  - Linear discharge CSA
  - Switched discharge CSA
  - Simulation results
  - Preliminary layouts
- **Outlook**

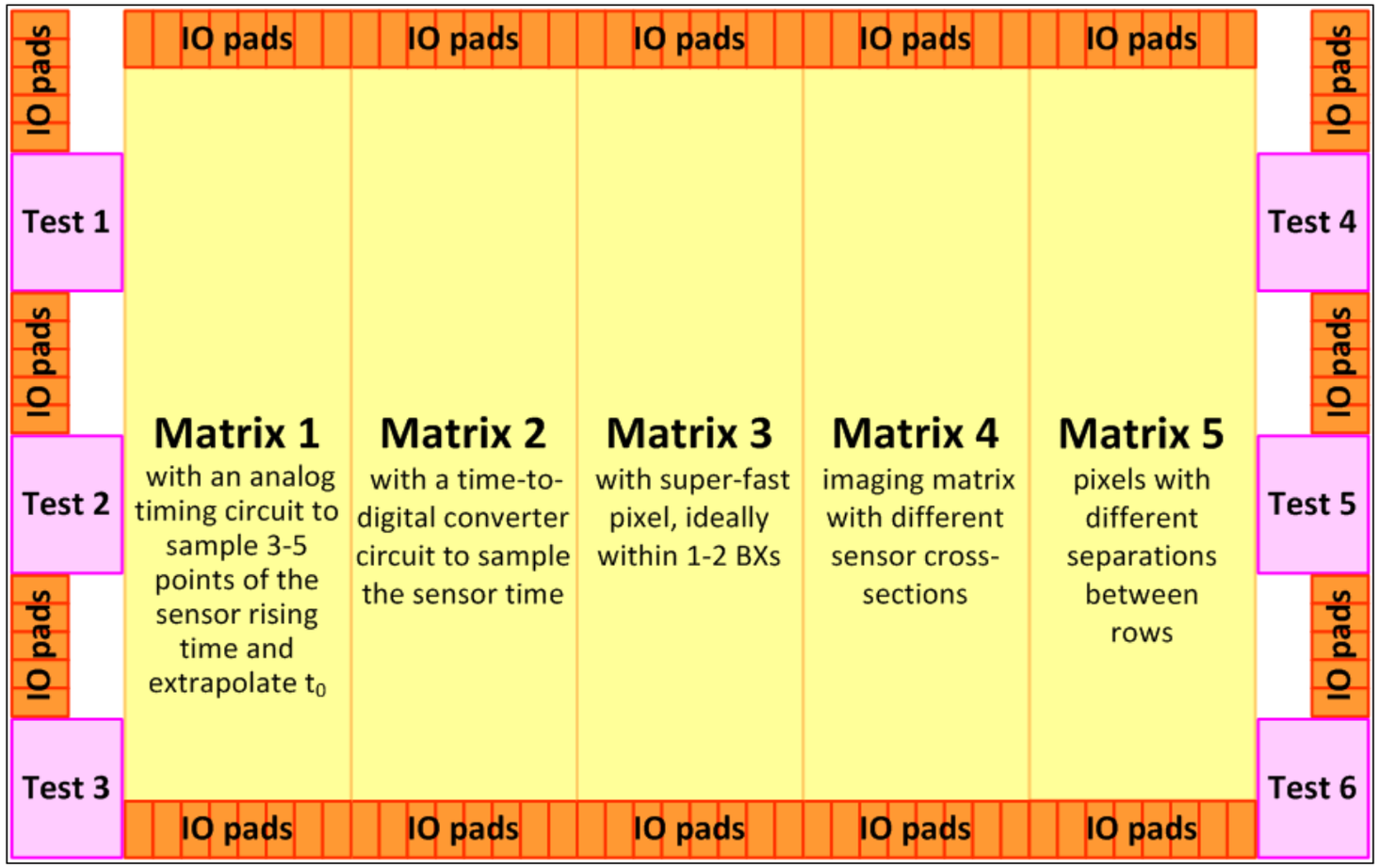
Introduction to HV-MAPS

- **HV-MAPS** stems from the combination of **HV-CMOS** (High-voltage COMS) and **MAPS** (Monolithic Active Pixel Sensor) technologies inheriting all of their advantages:
  - **less material budget**, **less cost**, **shorter production time**
  - **fast charge collection**, **good radiation tolerance** ($2 \sim 3 \times 10^{15}\, n_{eq}/cm^2$)
- It can be potentially used in the following experiments:
  - Mu3e experiment at PSI (first application of HV-CMOS detectors)
  - ITk in ATLAS Phase II Upgrade
  - CLIC



RD50-ENGRUN1

- A large area HV-MAPS demonstrator **RD50-ENGRUN1** including several matrices dedicated to improving the time resolution and signal processing speed is being designed within the RD50 collaboration.
- It also aims at testing new sensor cross-sections, and influence of a wide range of irradiation flux on the sensors.
  - **Technology**: 150 nm HV-CMOS from LFoundry S.r.l
  - **Design efforts** from: Uni. Liverpool, FBK, IFAE, Uni. Barcelona, Uni. Seville



floorplan of RD50-ENGRUN1

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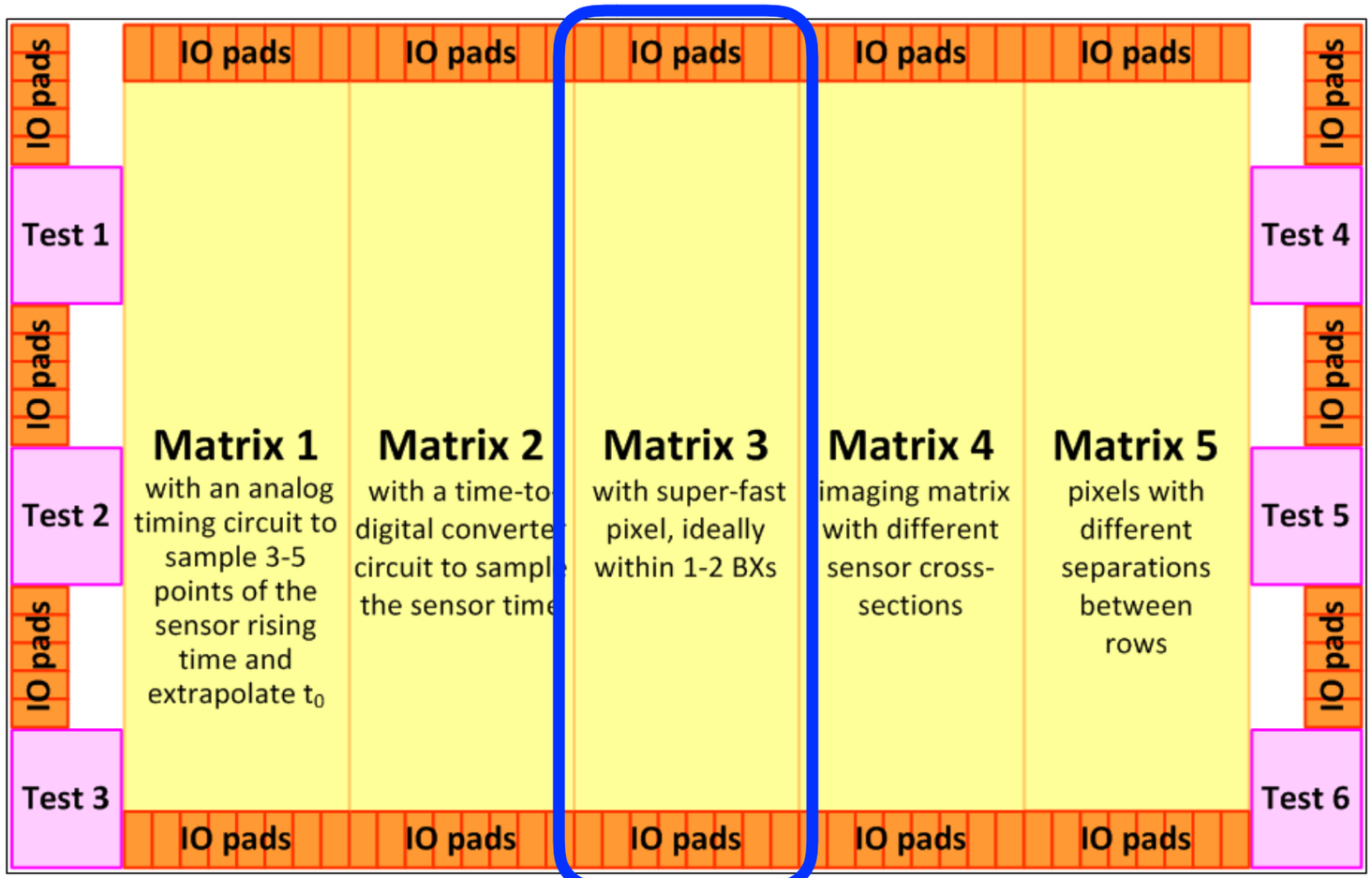
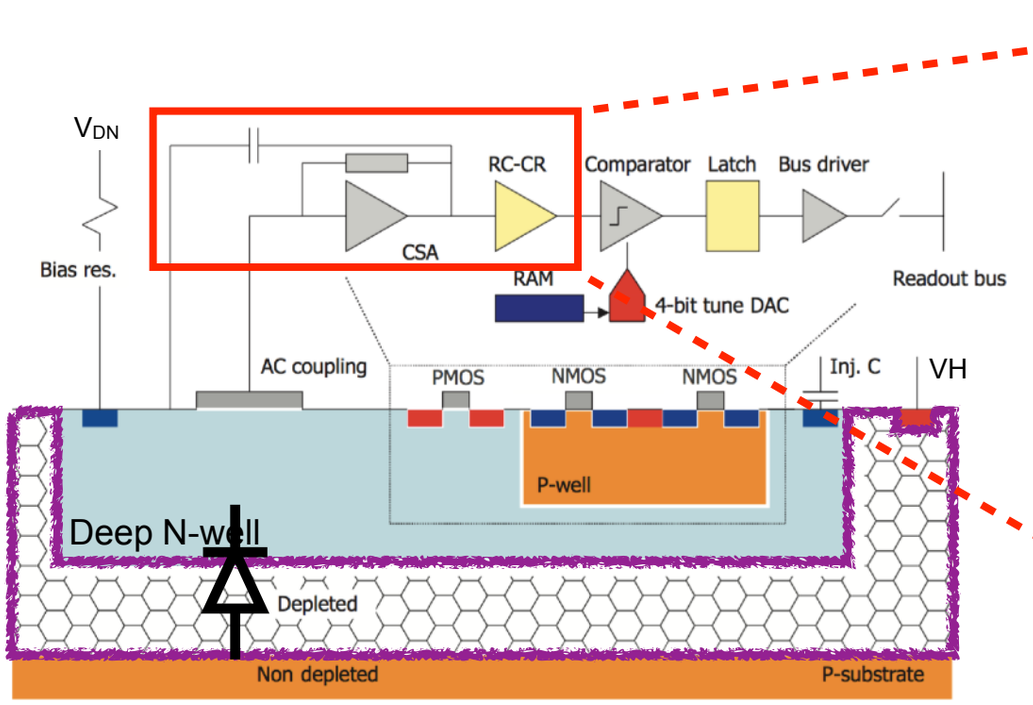


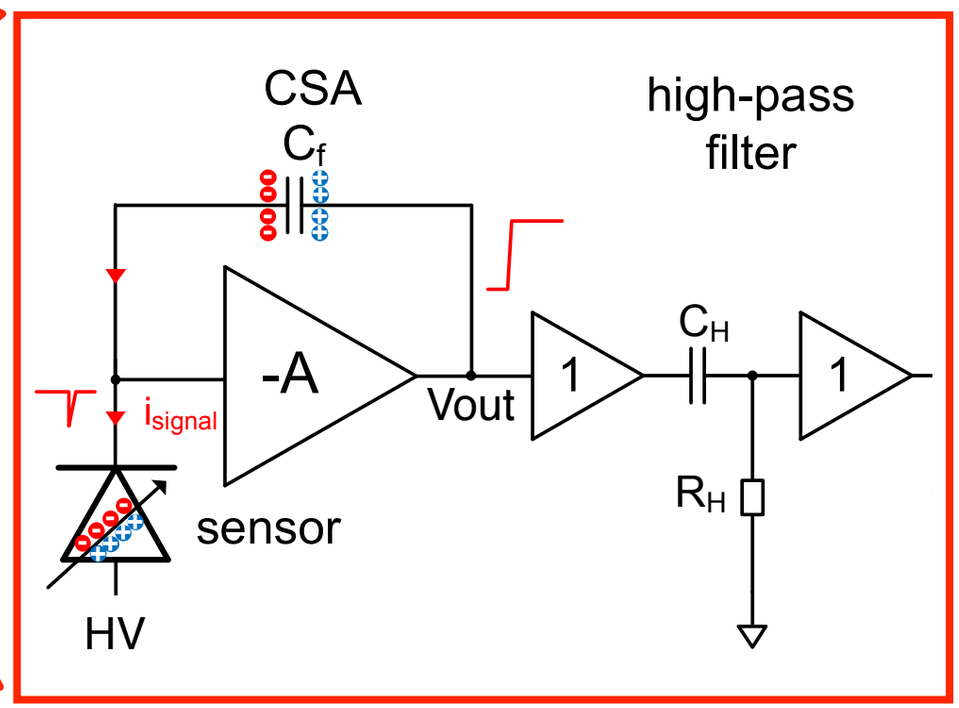
floorplan of RD50-ENGRUN1

- In Matrix 3, several different flavoured HV-MAPS pixel types using different high-speed readout front-end circuits will be implemented.

High-speed front-ends

- The readout front-end circuit is generally composed of a **Charge Sensitive Amplifier** (**CSA**), a high-pass filter and a comparator. The CSA mainly determines the processing speed. A pre-amplifier with gain of -A and a feedback capacitor C_f constitute a CSA.
- The negative feedback loop forces charges generated in the depleted region to integrate on C_f and forms a voltage rise (ΔVout) on the output of the CSA. **The pre-amplifier decides the voltage rising speed.** 3 types of pre-amplifiers based on the single folded cascode architecture have been designed.





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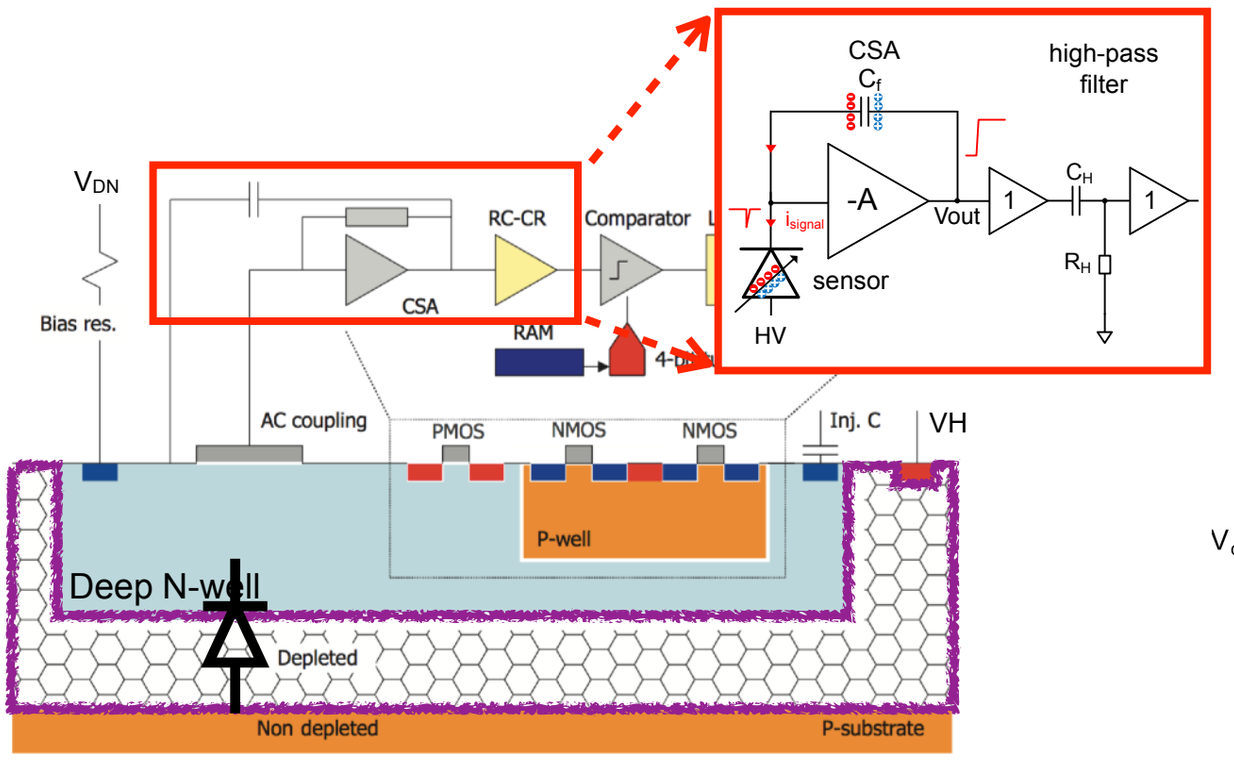
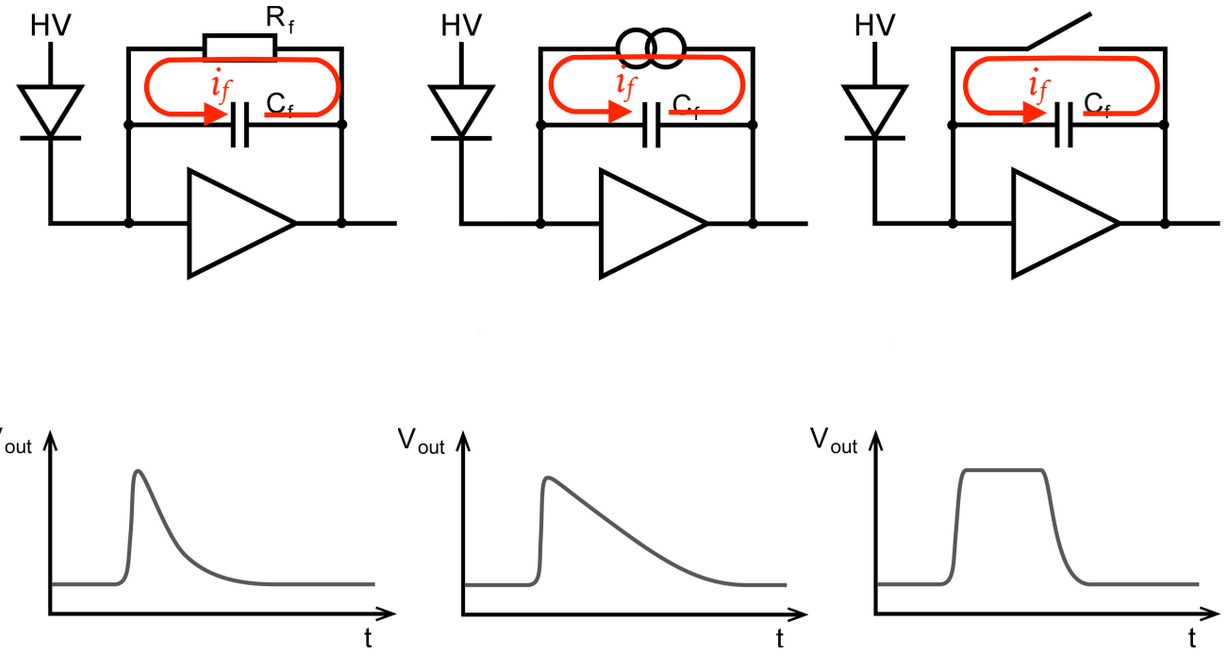
- To finish processing a particle hit and also avoid saturation on Vout, C_f needs to be discharged. **The discharge process decides the voltage falling speed**, 3 possible methods are:
  - **Resistive discharge**: C_f is discharged exponentially through the RC loop.
  - **Linear discharge**: C_f is discharged linearly by a constant current source.
  - **Switched discharge**: C_f is discharged immediately when the switch is closed.





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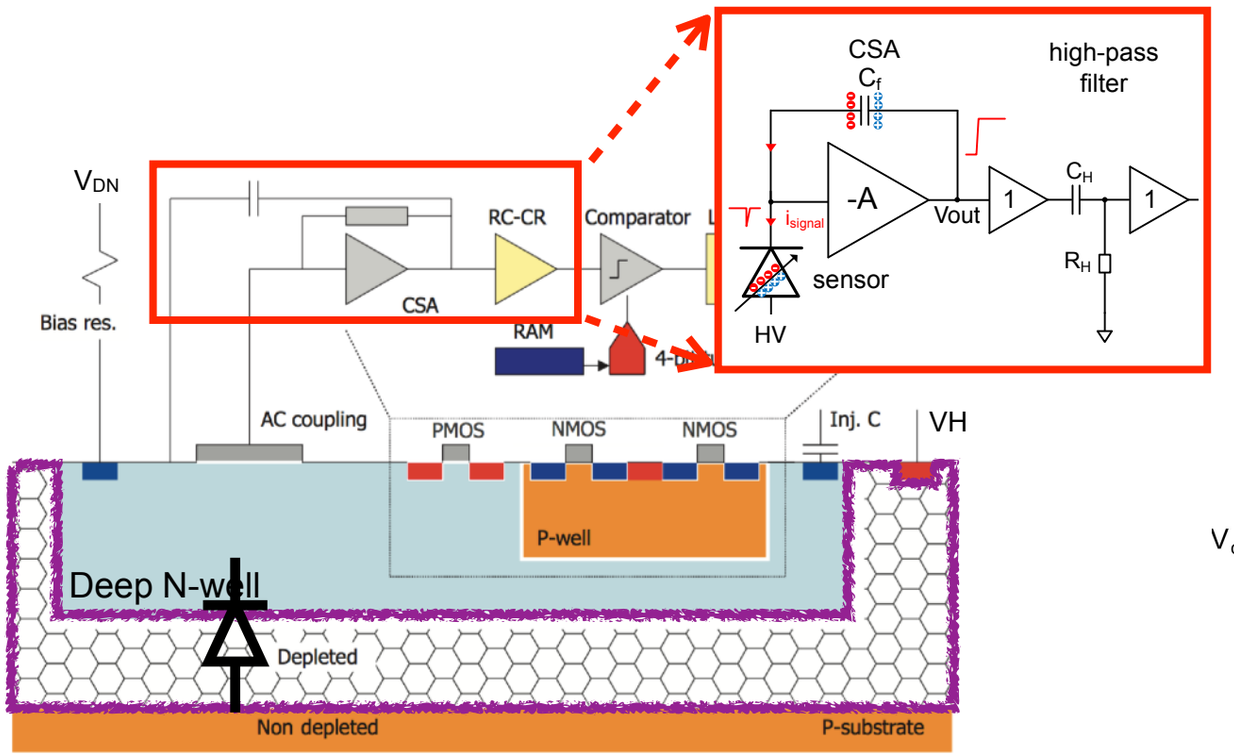
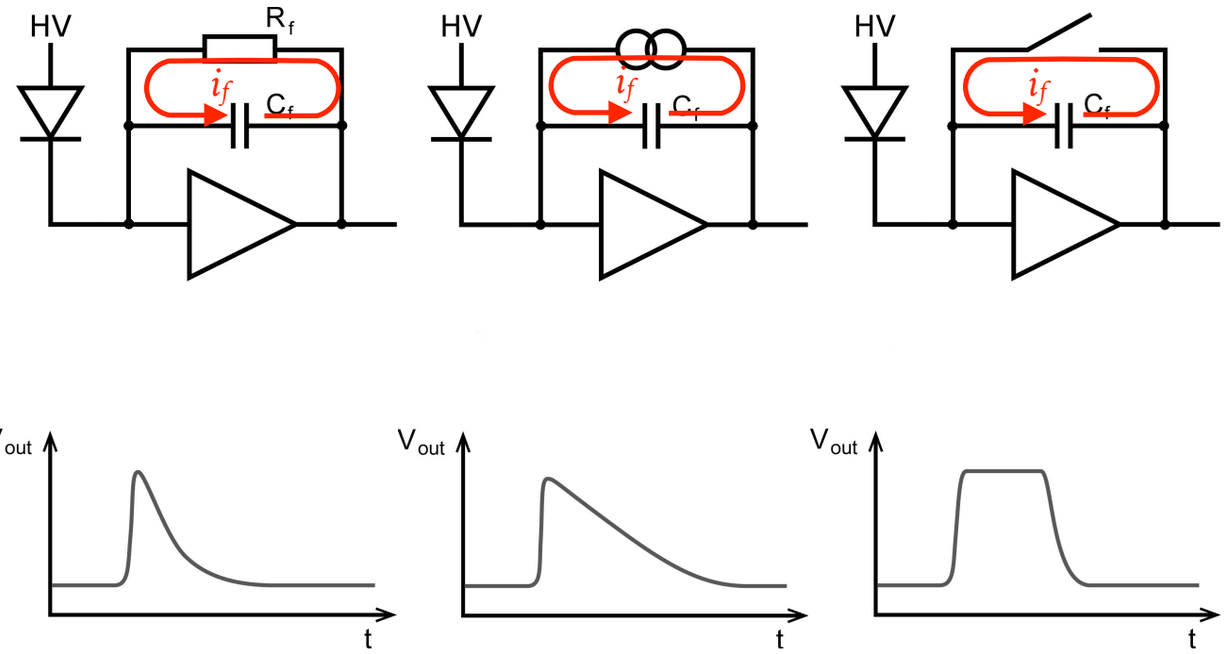
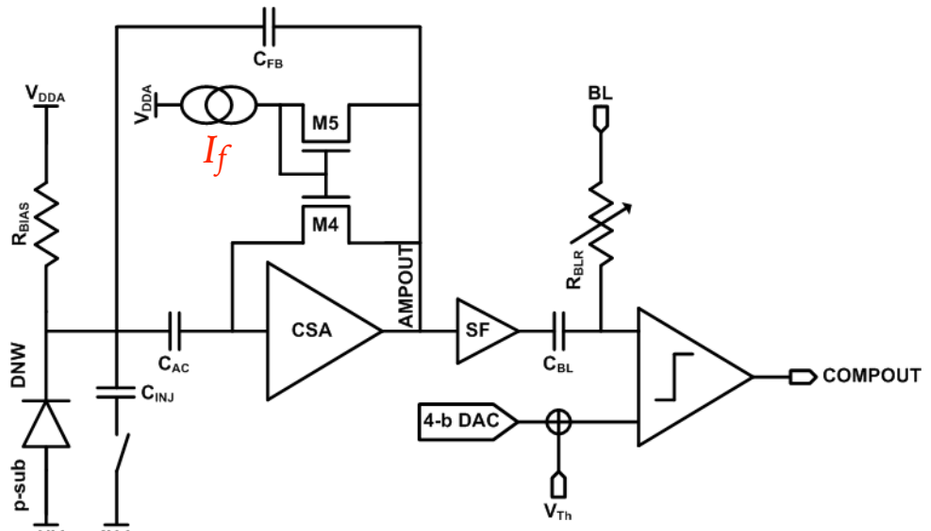
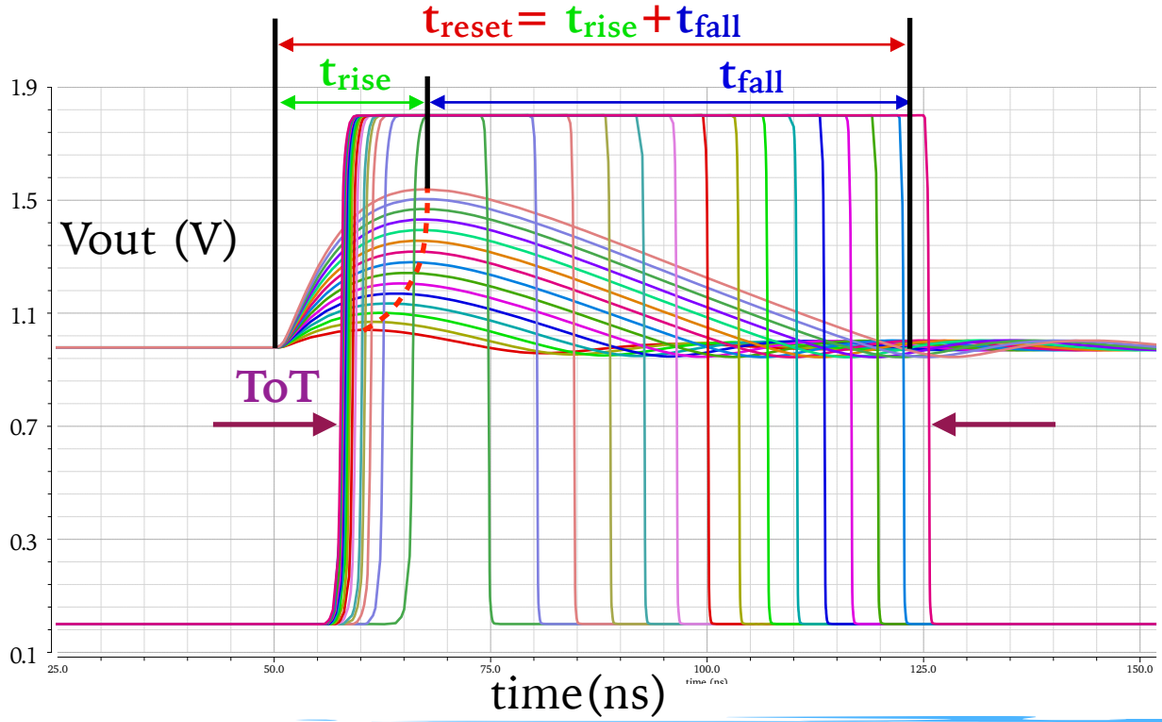


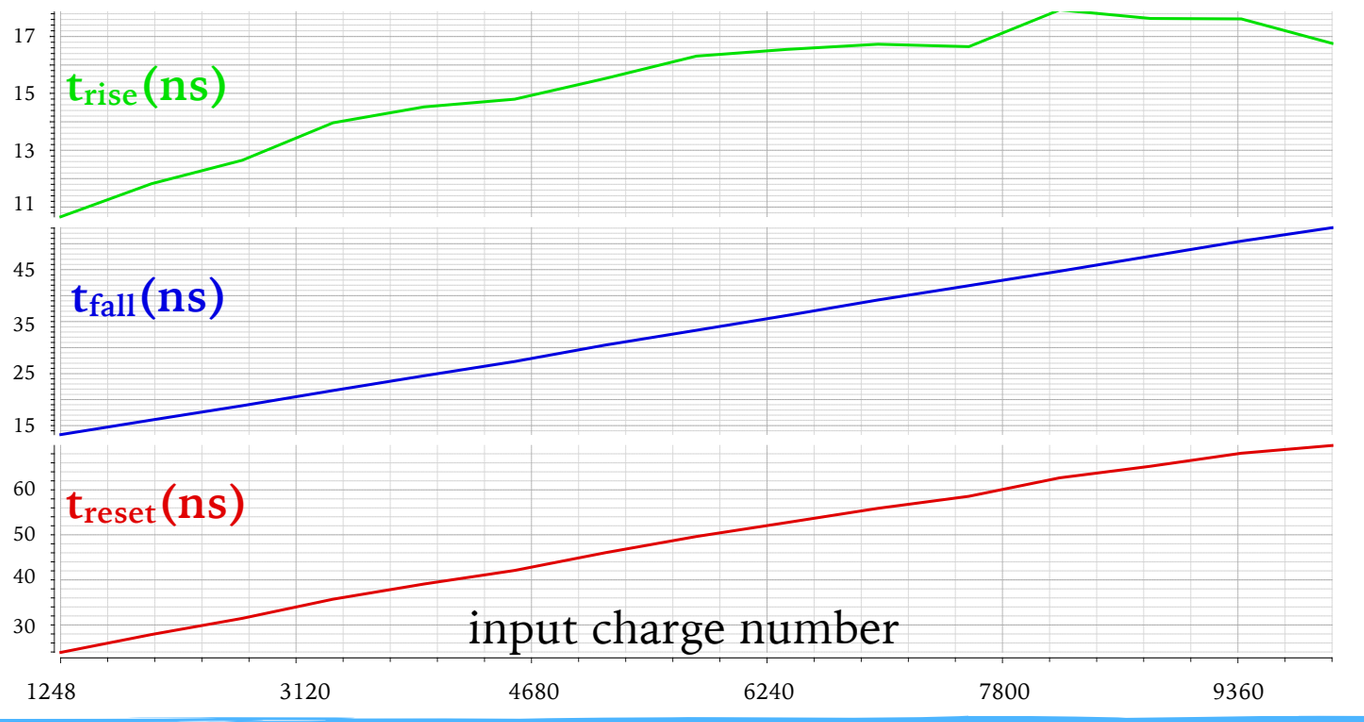


Linear discharge CSA

- A current mirror conducting I_f functions as the constant current source in the linear discharge CSA that has a straight falling edge on its output voltage.
- The triangle-shaped waveform of Vout makes it possible of using **Time over Threshold** (**ToT**) to measure the number of charges generated by a particle.
- increase of rise time (t_{rise}) is small. Fall time (t_{fall}) increases linearly with the charge number. The total processing time (t_{reset}) also grows linearly and can be less than 50 ns for a 5000 e- signal.

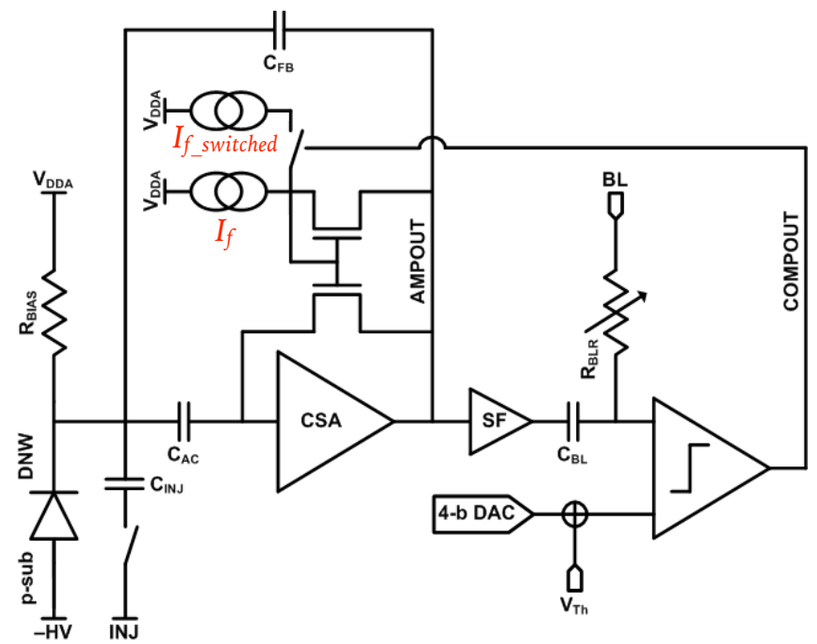


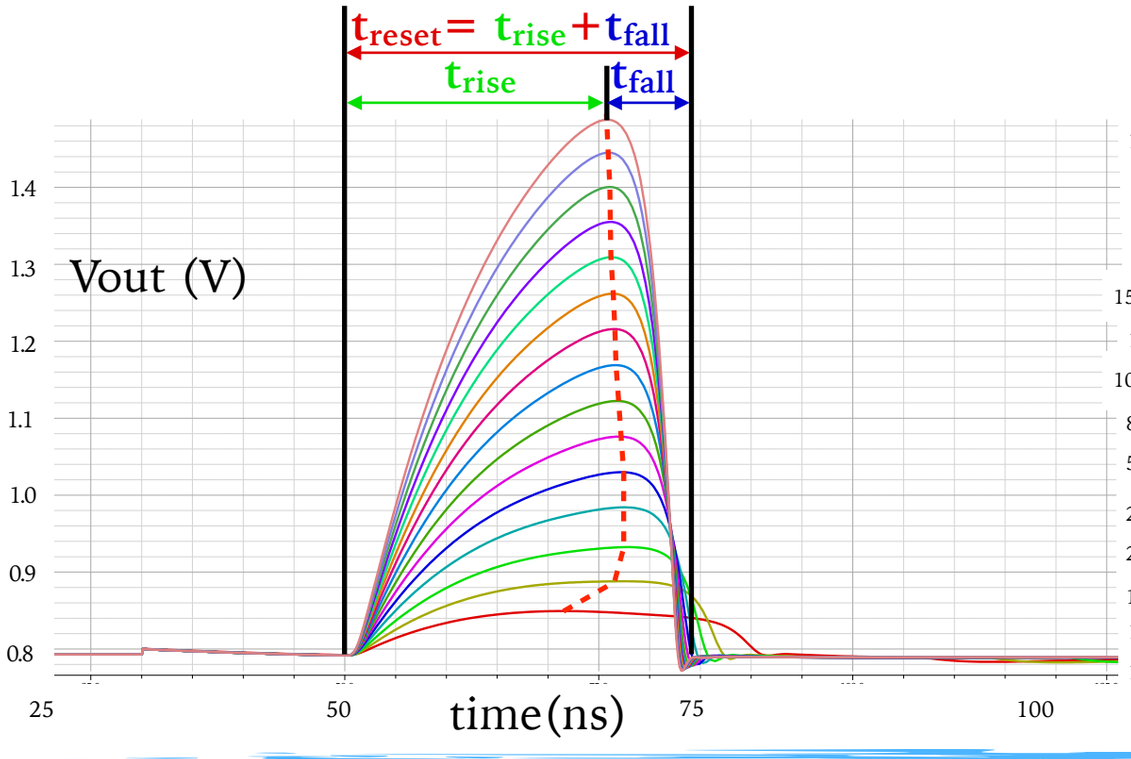


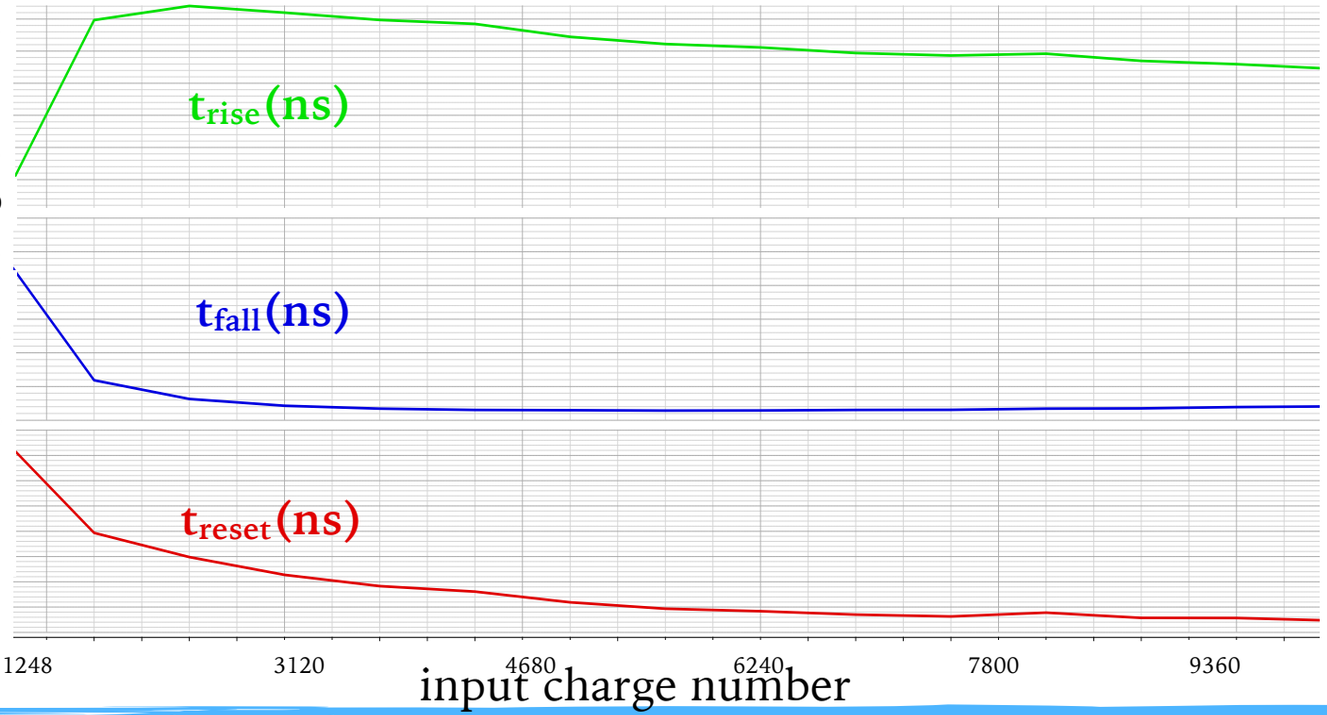


Switched discharge CSA

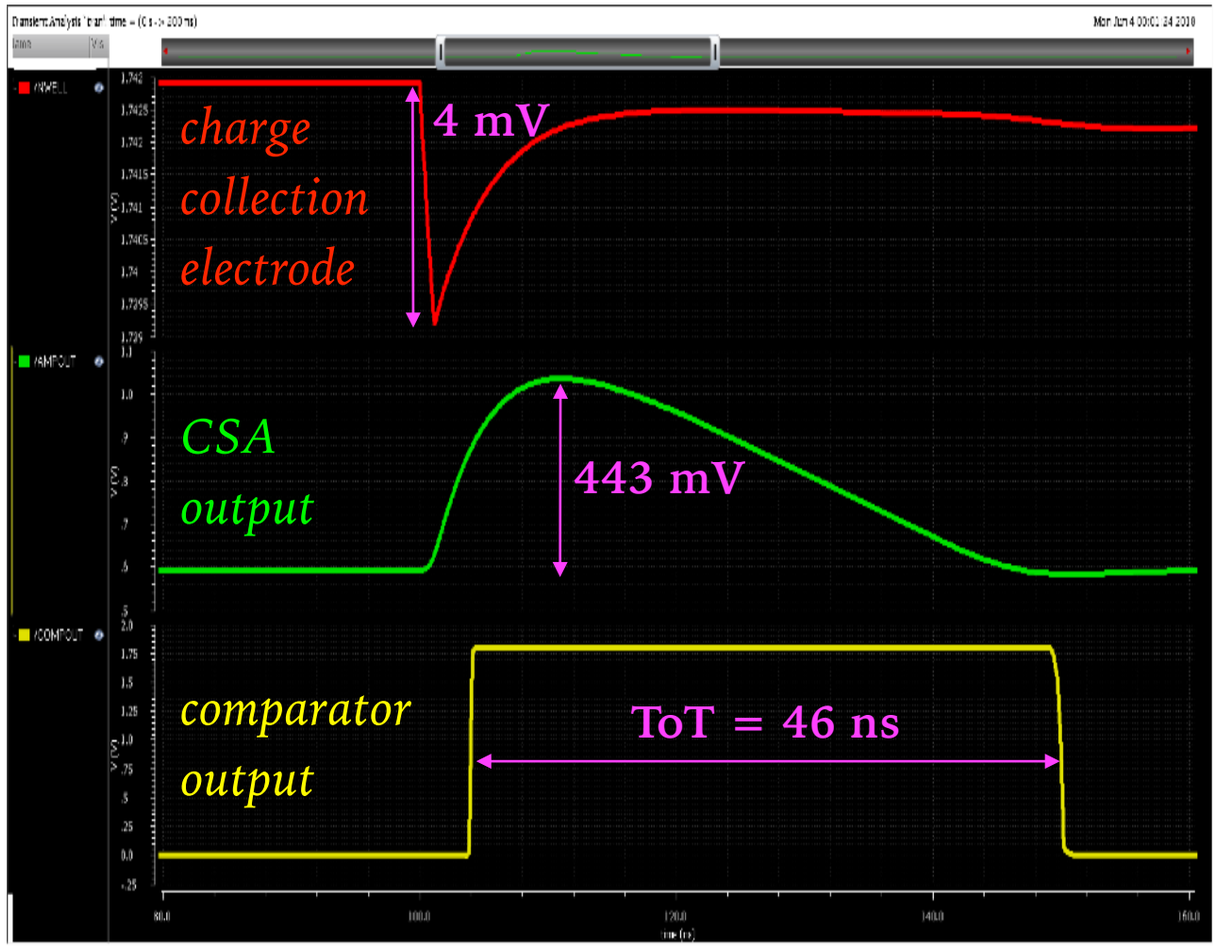
- The switched discharge CSA uses the comparator's output to control the discharge circuit that resets the CSA with a switched large current $I_{f\_switched}$ when a particle hit is detected. The discharge process is done almost immediately.
- The vertical falling edge of Vout makes **ToT** unrelated to the number of charges. Only measuring of the rising edge time stamp is necessary.
- Both rise time (t_{rise}) and fall time (t_{fall}) changes a little with the charge number. The total processing time (t_{reset}) stays constantly below 20 ns now matter how many input charges.



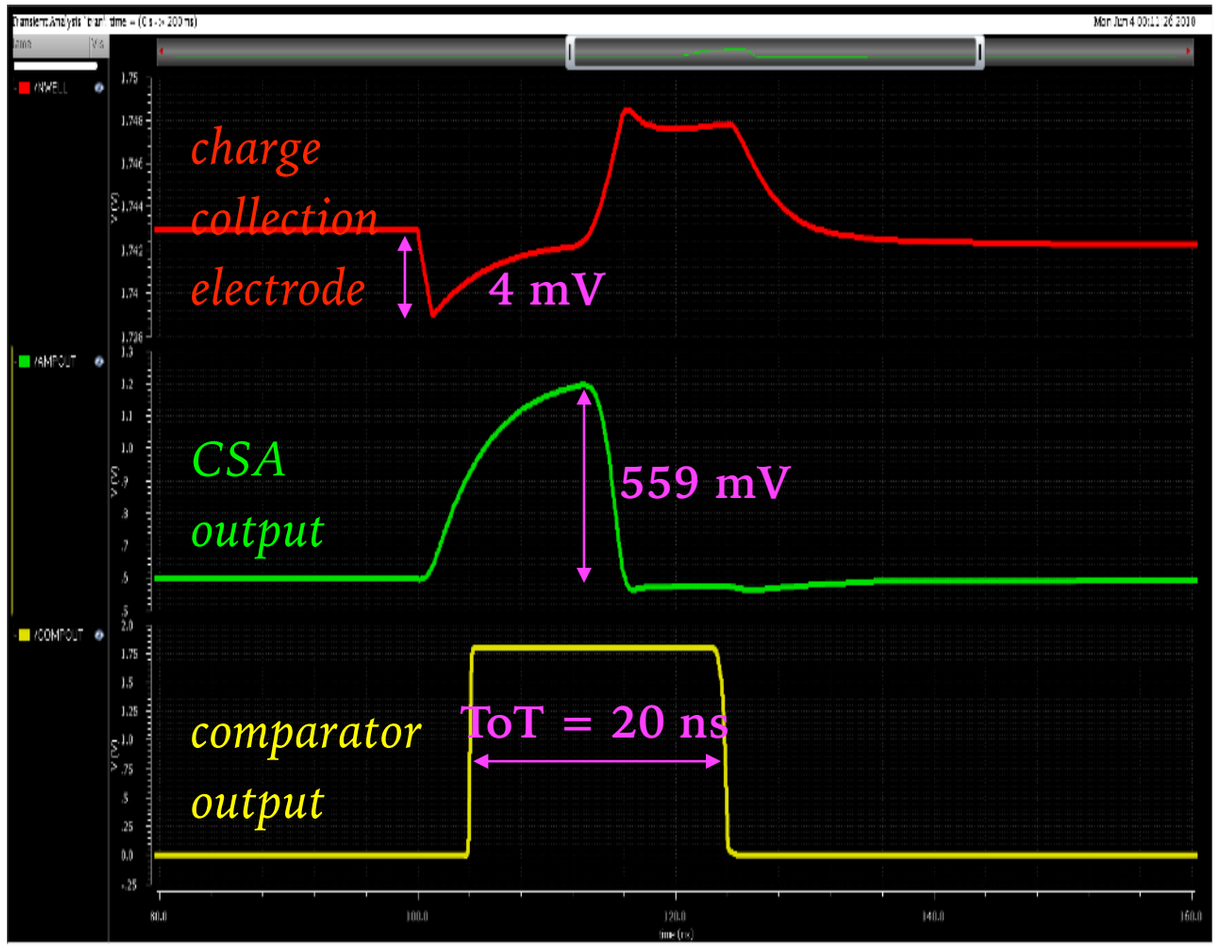




Simulation results



Linear_CSA_V1



Switched_CSA_V1

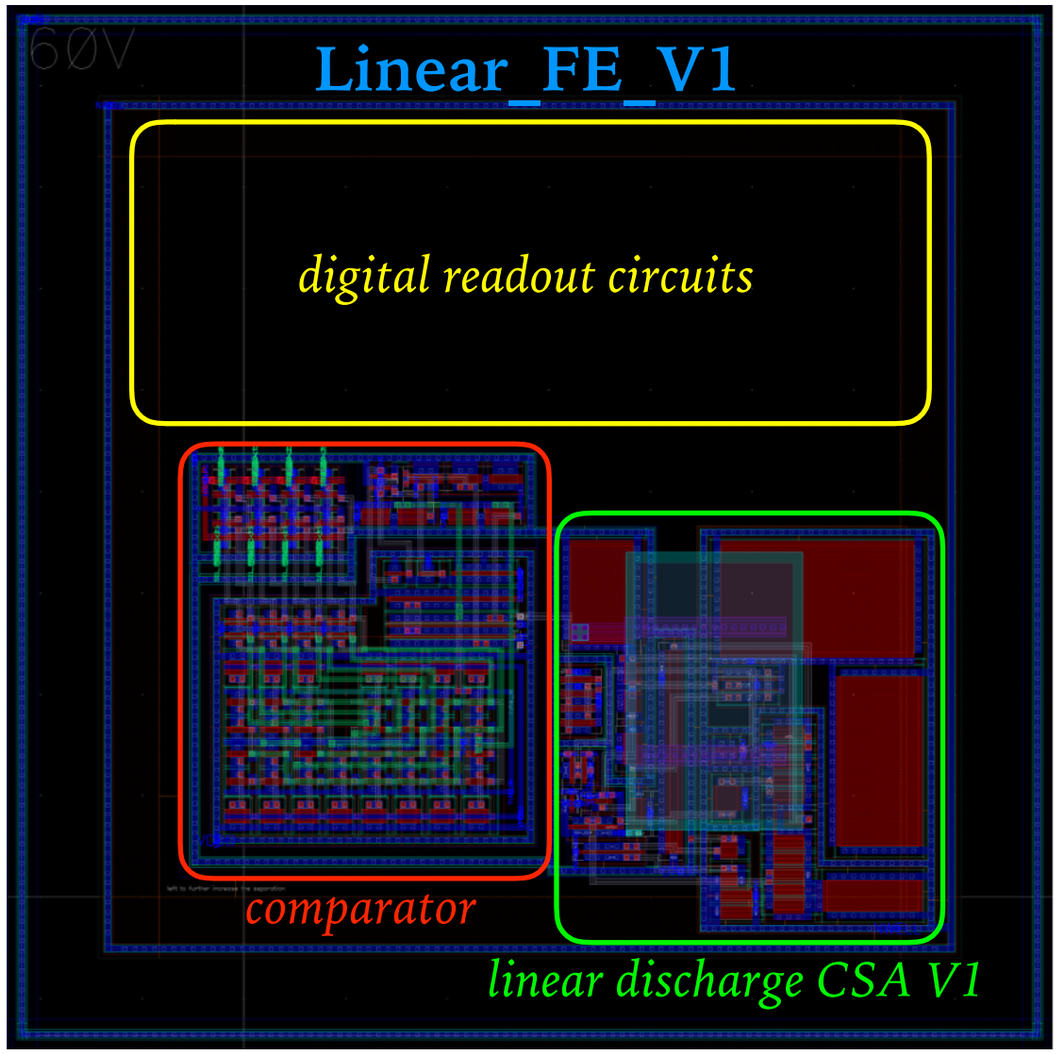
- Combining linear discharge method or switched discharge method with the first type of pre-amplifier forms CSAs Linear_CSA_V1 and Switched_CSA_V1 respectively. Simulation results of these two front-ends for a 5000 e- input are shown above.
- The Linear discharge CSAs have high processing speed and provide ToT information for measuring input signal strength. The Switched discharge CSAs have even shorter processing time, but are not able to tell signal strength from ToT.

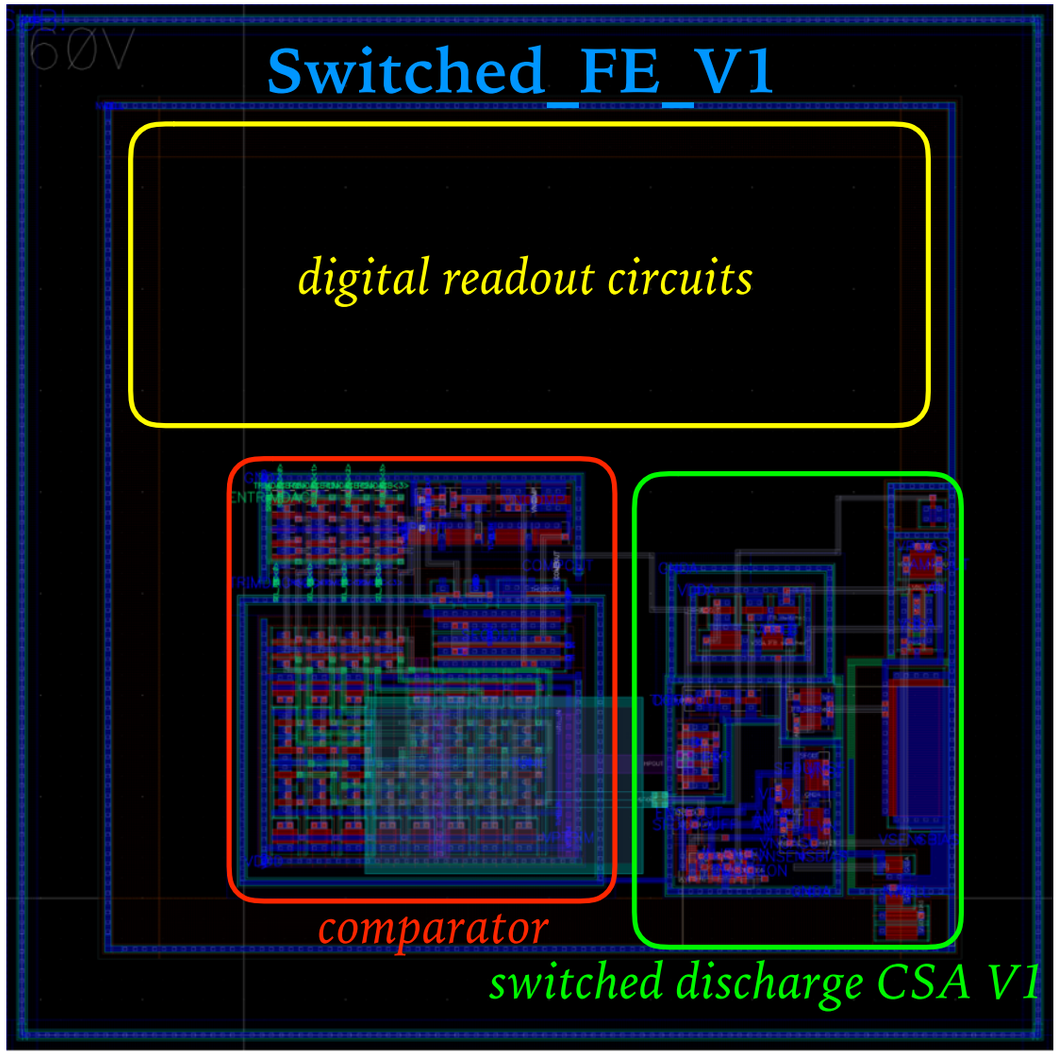
Simulation results

input: 5000 e⁻ @ HV = -60 V	Linear_CSA_V1	Linear_CSA_V2	Linear_CSA_V3	Switched_CSA_V1	Switched_CSA_V2	Switched_CSA_V3
C_{input}	145 *fF*	145 *fF*	145 *fF*	155 *fF*	155 *fF*	155 *fF*
ΔVout	345.5 mV	291.8 mV	429 mV	461 mV	406 mV	448.6 mV
ENC	94 e⁻	36 e⁻	42 e⁻	93 e⁻	30 e⁻	64 e⁻
t_{ries}	9.7 ns	9.5 ns	11.6 ns	12.4 ns	12.3 ns	9.9 ns
t_{fall}	36.2 ns	35.6 ns	32.5 ns	5.7 ns	5.8 ns	6.5 ns
t_{reset}	45.9 ns	45.1 ns	44.1 ns	18.1 ns	18.1 ns	16.4 ns
Power cons.	21.9 μW	22.3 μW	23.4 μW	22.4 μW	22.7 μW	23.9 μW

- 6 front-ends flavours are possible as combinations of 3 types of pre-amplifier and 2 discharge methods. The results listed above are based on simulations that use schematic models.
- Further post-layout simulations will be performed to decide which flavours to be fabricated.

Preliminary layouts



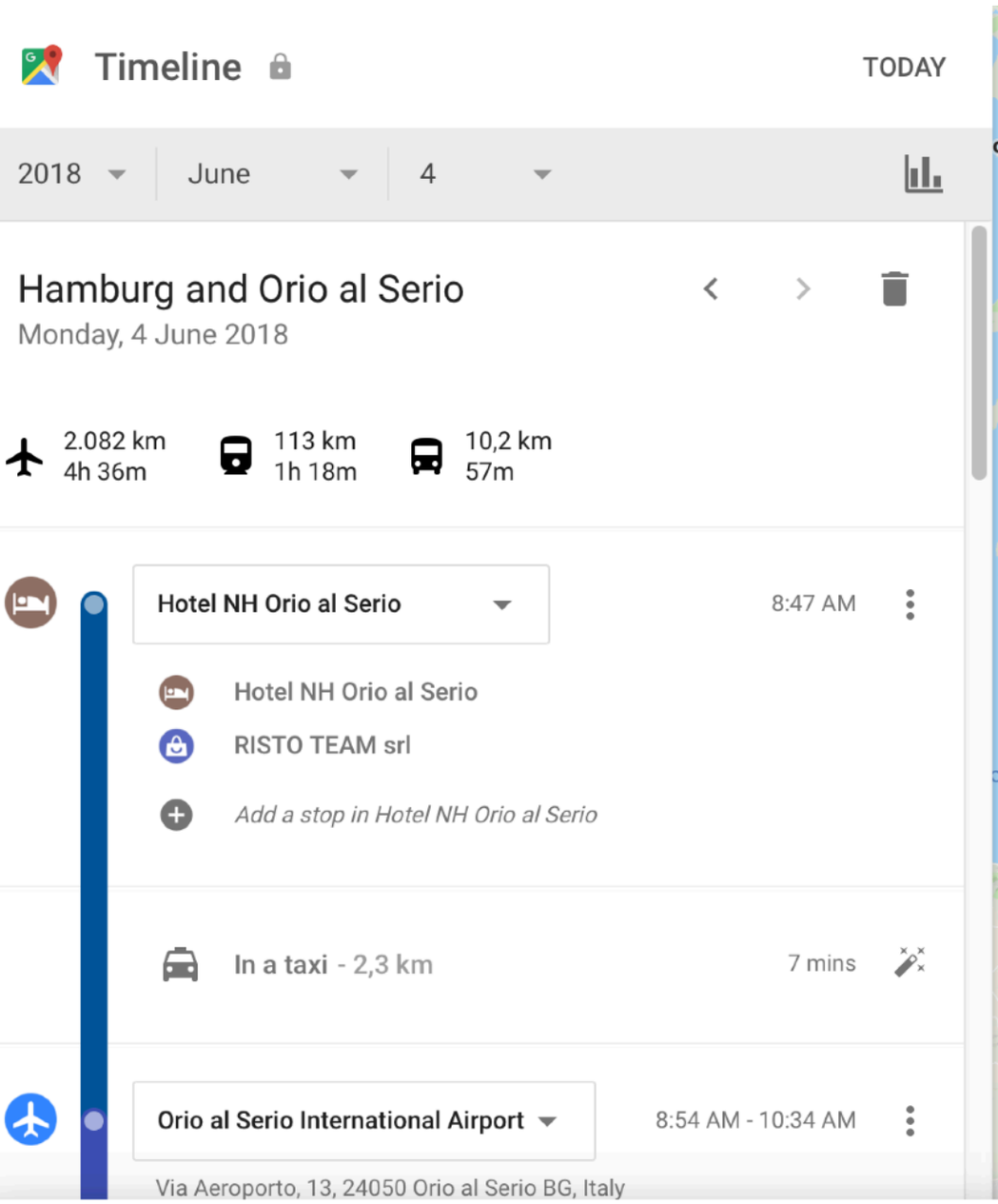


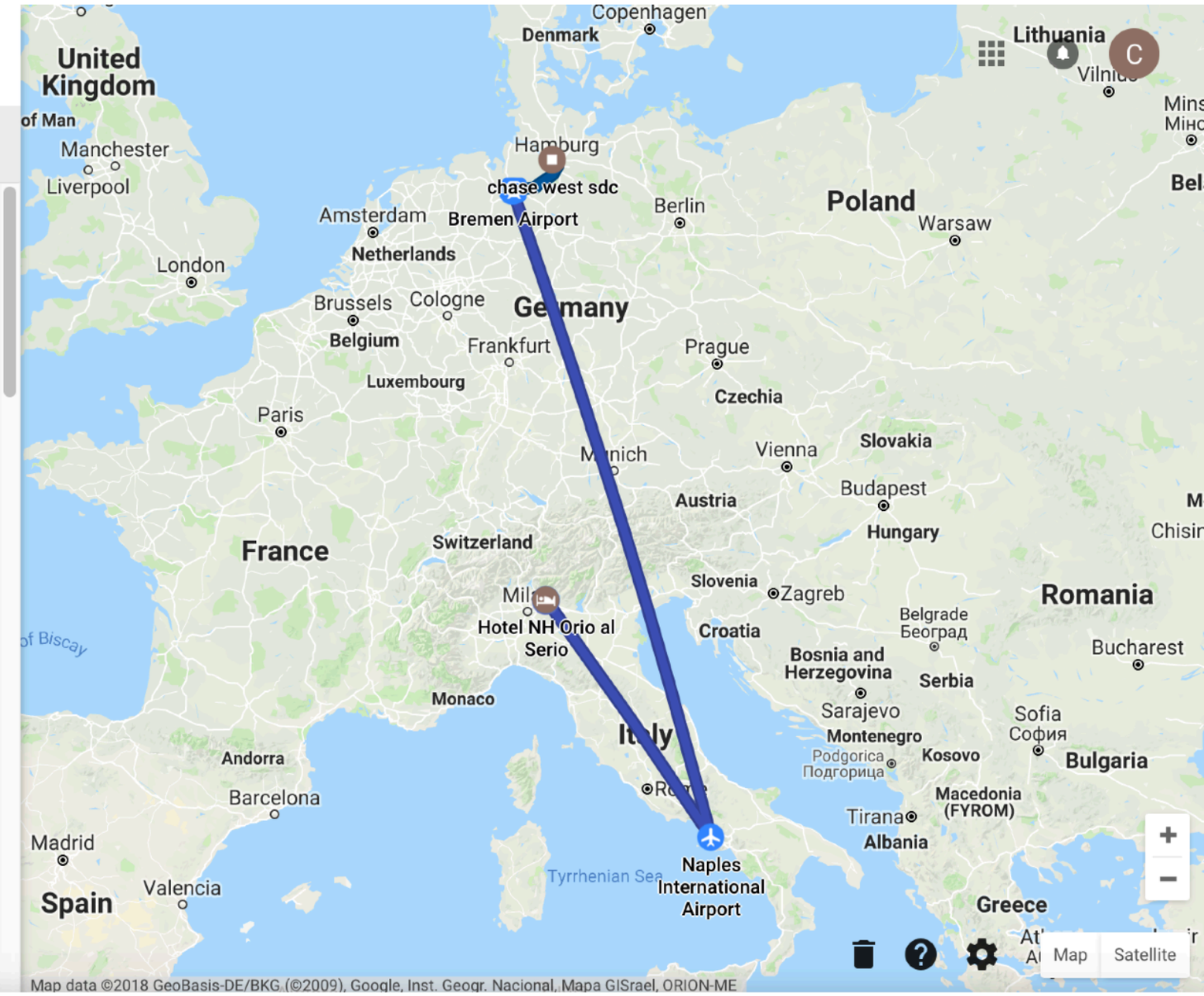
- Layout design of Linear_FE_V1 and Switched_FE_V1 front-ends have finished.
- Both analog and digital readout electronics will be integrated into the 50 μm × 50 μm pixel pitch.
- The comparator includes a current DAC for compensating offset variations.
- The digital readout circuits send out time stamps of the leading edge (LE) and trailing edge (TE) for linear discharge CSAs and ToT can be calculated as TE - LE off chip. For switched discharge CSAs, only the LE is sent out. The hit pixel address is also sent out for all types of front-ends.

Outlook

- After layouts of all front-end flavours are finished, the digital readout circuits will be designed.
- The Matrix will apply a column-drain readout architecture according to current plan.
- It is foreseen that RD50-ENGRUN1 will be submitted for fabrication after earlier chips with RD50 are characterised and well understood (late 2018).

My journey to DESY





- Trento -> Milan Bergamo airport -> Naples airport -> Bremen airport -> Bremen train station -> Hamburg train station -> DESY

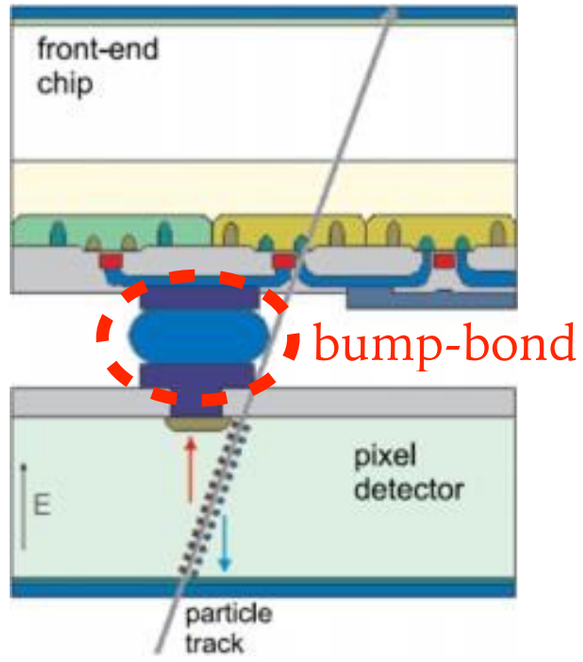
Backup

Introduction to HV-MAPS

➤ **Hybrid Detectors** assemble semiconductor planar sensors with readout chips using bump-bonds or glue.

Pros:
- freedom of choosing different technologies for the two parts:
  1. adjustable doping in the sensor —> **high radiation tolerance**
  2. suitable technology for the readout ASIC —> **fast readout**

Cons:
- large material thickness due to assembly causes **multiple scattering**
- the assembly process is **time-consuming** and **expensive**

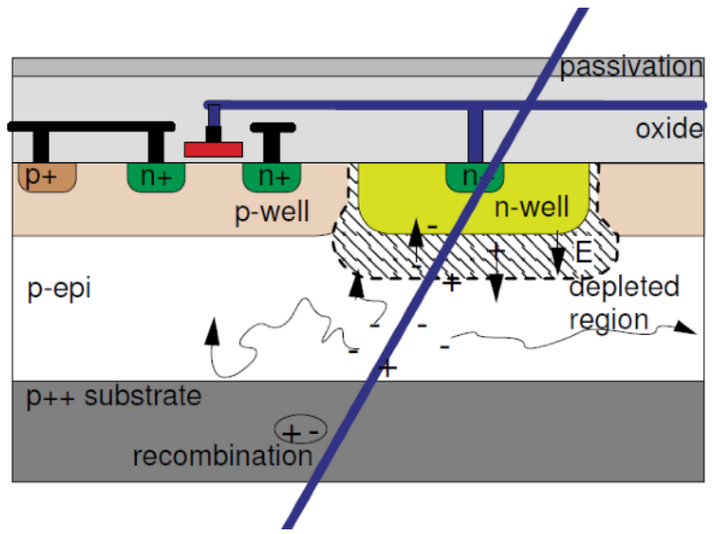


Hybrid Detector

➤ **Monolithic Active Pixel Sensor (MAPS)** allows embedding readout electronics within the pixel detector.

Pros:
- the monolithic structure gets rid of the assembly process —> **less material budget**, **less cost** and **shorter production time**

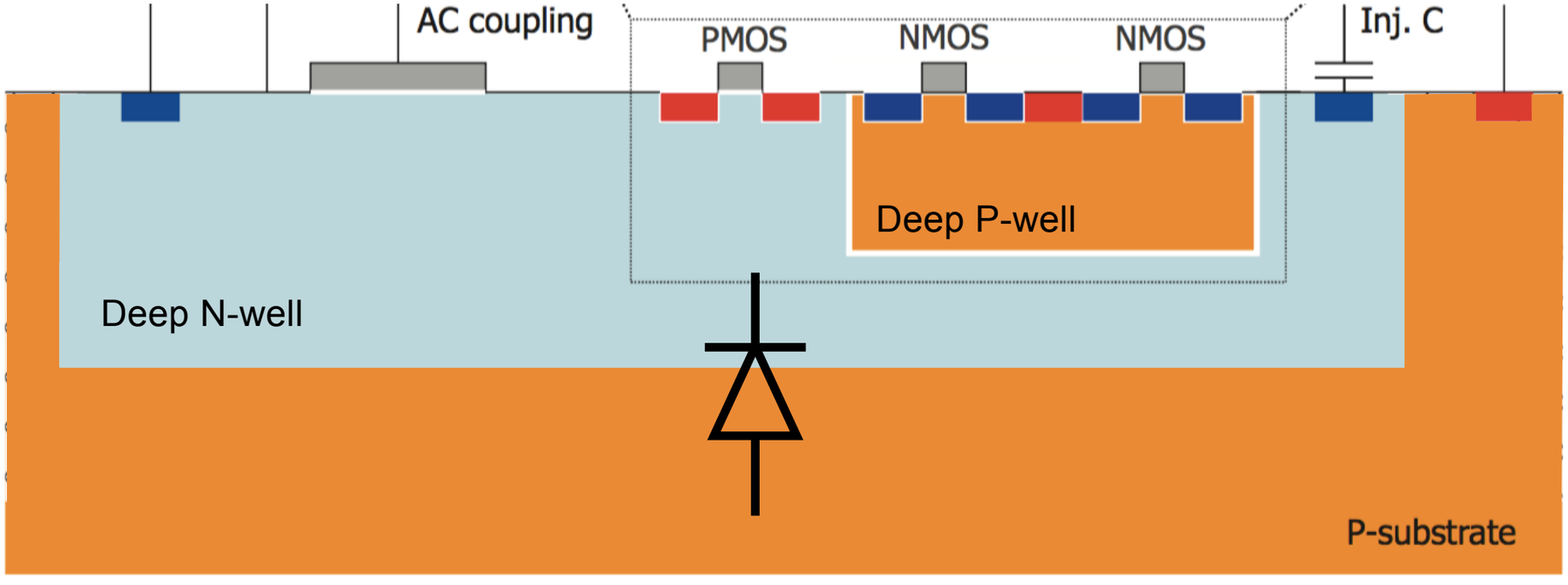
Cons:
- the sensor and readout circuits use the same technology —> **restricted radiation tolerance** ($< 10^{15}\ n_{eq}/cm^2$)



MAPS

Introduction to HV-MAPS

- **HV-CMOS** technology supports applying high bias voltage (<120V) onto the substrate of sensors, which can form a strong electric field in the depletion region and leads to:
  - **fast charge collection** via **drift** (~200 ps) instead of **diffusion** (~100 ns)
  - **good radiation tolerance**
- High bias voltage forms a **wide depletion region**
  - more charges are generated by a particle —> **high SNR**



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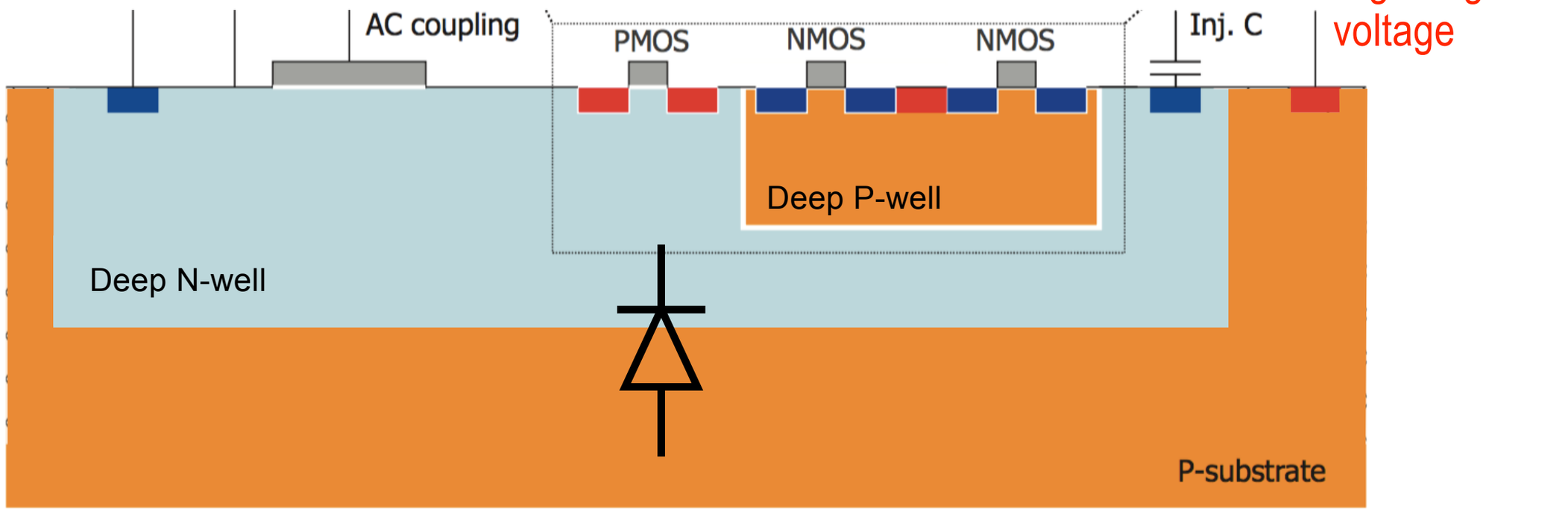

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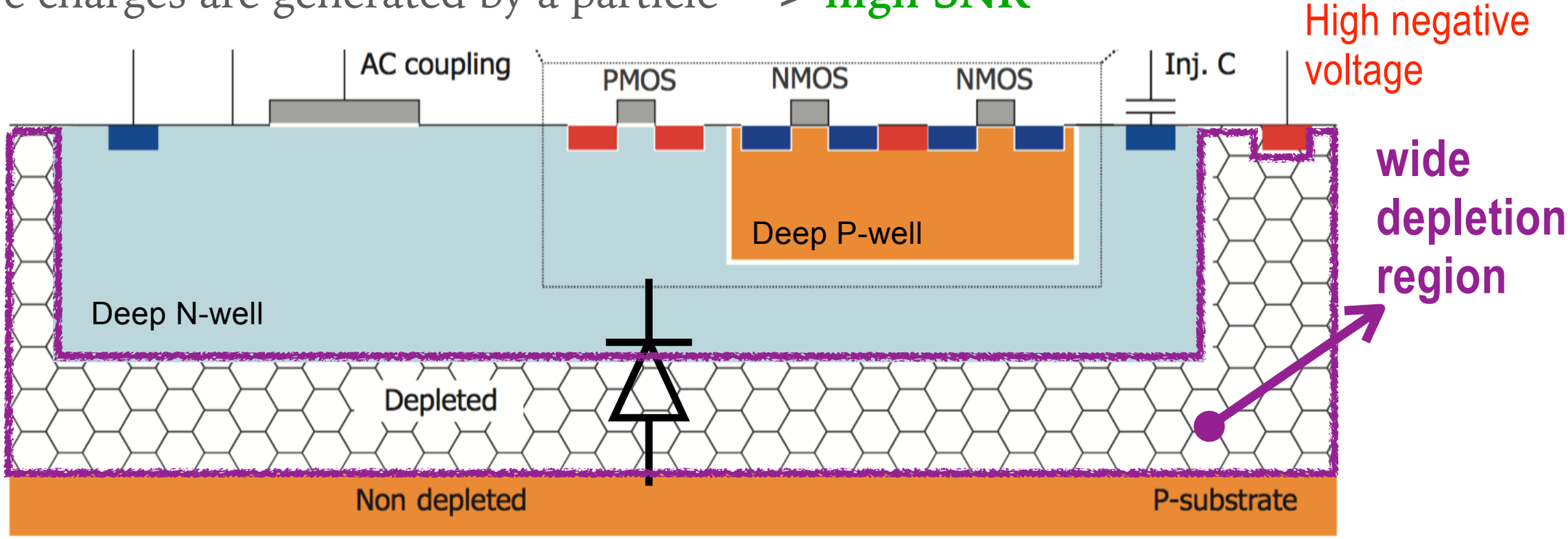

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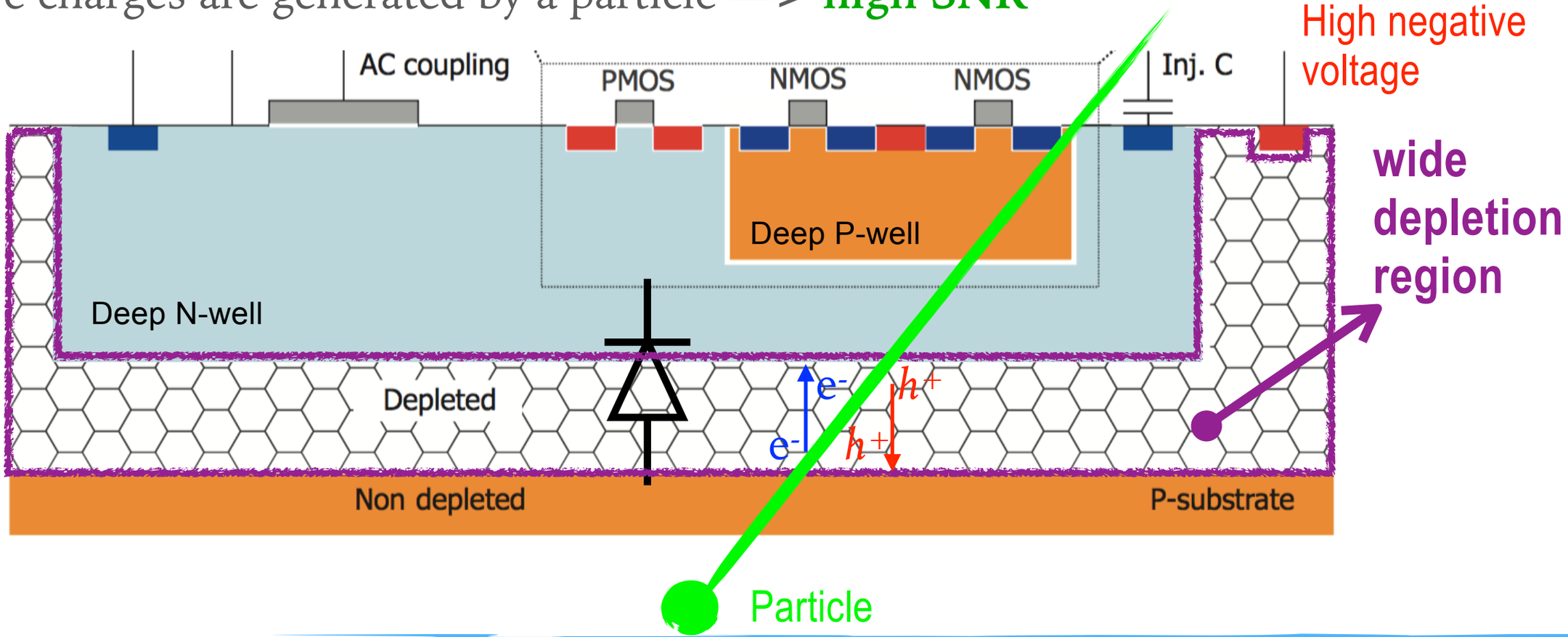

Pixel Readout Circuits – Standard CSA

- The CSA is composed of a pre-amplifier and a feedback branch.
- Charges generated by particle hits are integrated on the feedback capacitor C_f, its closed-loop gain is $G_{CSA} = 1/C_f$ ideally.
- C_f is implemented by C_{db} of the load transistor M_VPBIAS in this project.
- The Reset circuit discharges C_f to avoid saturation on CSA's output
- A current mirror as a constant current source placed in parallel with C_f takes the role of the reset circuit