Contribution ID: **6** Type: **not specified**

Design of high-speed front-ends for HV-MAPS within the CERN-RD50 collaboration

Tuesday 5 June 2018 09:45 (20 minutes)

The High Voltage-Monolithic Active Pixels Sensors (HV-MAPS) detector technology is a promising candidate for particle physics experiments. While standard hybrid sensors require bump-bonding or gluing to assemble the sensor and the readout electronics together, fully monolithic HV-MAPS allow integrating these parts onto one single chip, which makes them more cost-efficient especially for tracking applications that require large area silicon sensors. The high bias voltage that can be applied to the sensors forms a wide depletion region that improves the signal-to-noise ratio and a strong electrical field that drifts charges to the collecting node. Moreover, the radiation tolerance of HV-MAPS is also improved, which has been demonstrated to be up to a few $10^{15} n_{eq}/cm^2$.

As the HV-CMOS technology has many advantages, the RD50 collaboration is making efforts to study it in view of future particle physics experiments such as the High Luminosity-LHC (HL-LHC) and beyond. A large area demonstrator (RD50-ENGRUN1) with several matrices dedicated to improving the time resolution and speed of the sensor using different solutions at the readout circuit level amongst other matrices is being designed.

One of the pixel matrices will include four differently flavoured pixel types. These pixels are distinguished by two types of Charge Sensitive Amplifier (CSA) that use either a PMOS or an NMOS as the input transistor and two mechanisms of reset that are continuous or switched. The first two types use continuous current sources as their reset circuits resulting in the CSA's fall time being proportional to the number of input charges. The rise time of these two pixel types is less than 10 ns. Adjusting the reset current to a high value, it is possible to process a particle hit that generates 10K electrons in the sensing diode within 100 ns. The latter two use the discriminators'outputs to control the reset circuits that reset the CSAs with a switched large current while keeping the power consumption low. Such high current can discharge the feedback capacitors almost immediately and limits the fall time below 10 ns no matter how many input charges a particle generates. The total processing time is thus less than 25 ns. The continuously reset pixels will provide both rising and trailing edge time stamps to obtain Time over Threshold (ToT) information. In contrast, the switched reset pixels will only give the time stamp of the rising edge.

The timing information mentioned above is all obtained from simulations that use schematic models. All pixel flavours will integrate both analog and digital readout electronics into the 50 µm × 50 µm sensing area and be read out using a column-drain readout strategy. More details about the RD50-ENGRUN1 and the high-speed pixel matrix will be presented at the talk.

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Session Classification: CMOS Sensors