

# CNM Activities on LGADs for ATLAS/CMS Timing Layers

S. Hidalgo, M. Carulla, A. Doblas, D. Flores,  
A. Merlos, G. Pellegrini, D. Quirion

Centro Nacional de Microelectrónica, IMB-CNM-CSIC, Barcelona, Spain



Work done in the framework of the CERN RD50 Collaboration and AIDA 2020 Project

## Summary (1/2)

- **4'' Thin LGAD 4 AIDA2020 (35 and 50  $\mu\text{m}$  thick Si-Si)**
  - ✓ Mask Description (Version 18b)
  - ✓ Fabrication Process Basic Description. Run 11748
- **6'' LGAD (300  $\mu\text{m}$  thick, Run 9974)**
  - ✓ Electrical Characterization Results. I(V), C(V), Gain
- **6'' Thin LGAD (50-1-300  $\mu\text{m}$  SOI wafers). Run 11486**
  - ✓ Basic Description
- **6'' Thin LGAD 4 ATLAS/CMS (35-50  $\mu\text{m}$  thick Si-Si)**
  - ✓ Mask Description (Version 3)

## Summary (2/2)

- **4" Thin Gallium LGAD (50-300  $\mu\text{m}$  Si-Si wafers). Run 10924**

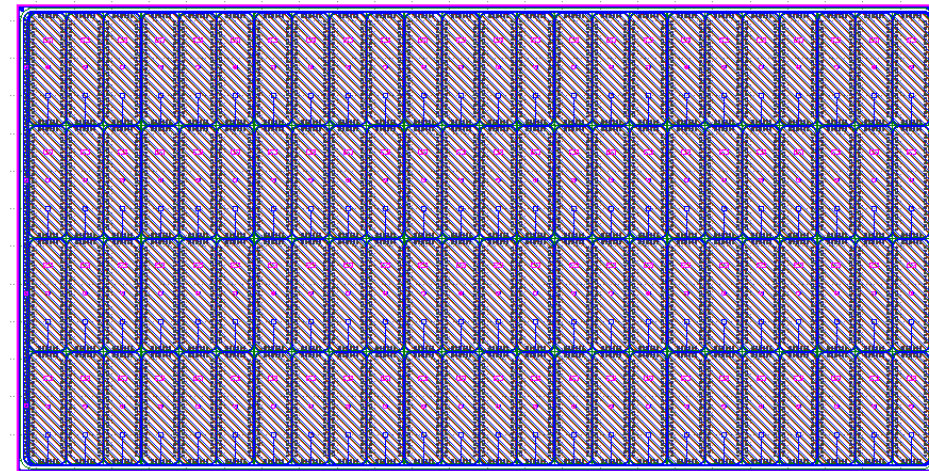
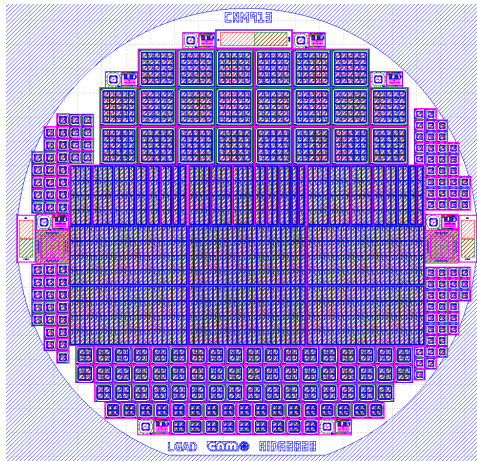
  - ✓ Basic Description
  - ✓ Electrical Characterization Results. I(V), C(V)

- **4" Run 10478. The Wafer 5 Affair**

  - ✓ Problem Description
  - ✓ Actions Performed
  - ✓ Electrical Characterization Results. I(V), C(V)
  - ✓ Proton & Neutron Irradiation Campaigns. Test Beams

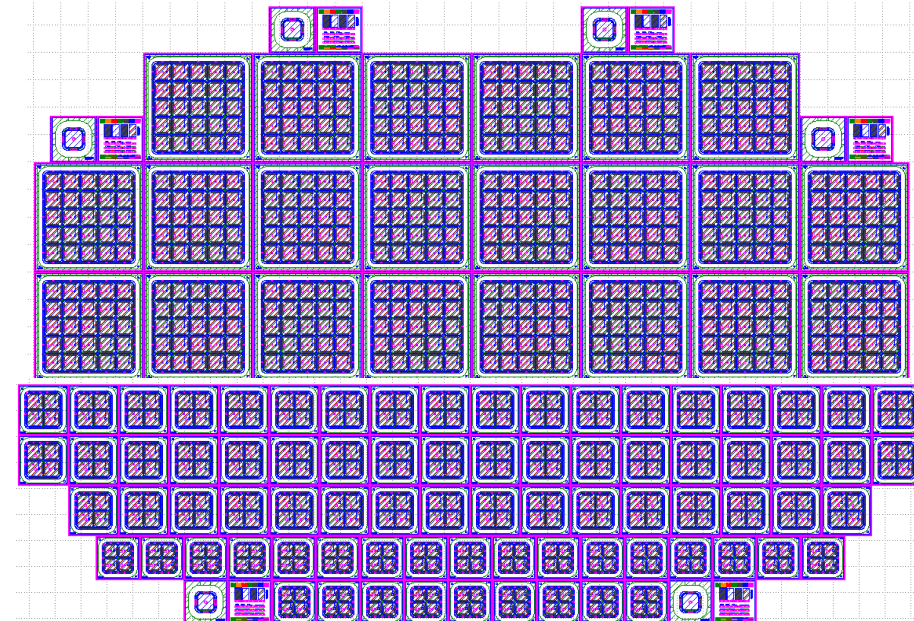
- **Future Work**

# 4" Thin LGAD 4 AIDA2020 (35-50 $\mu\text{m}$ thick Si-Si)



## Run AIDA2020

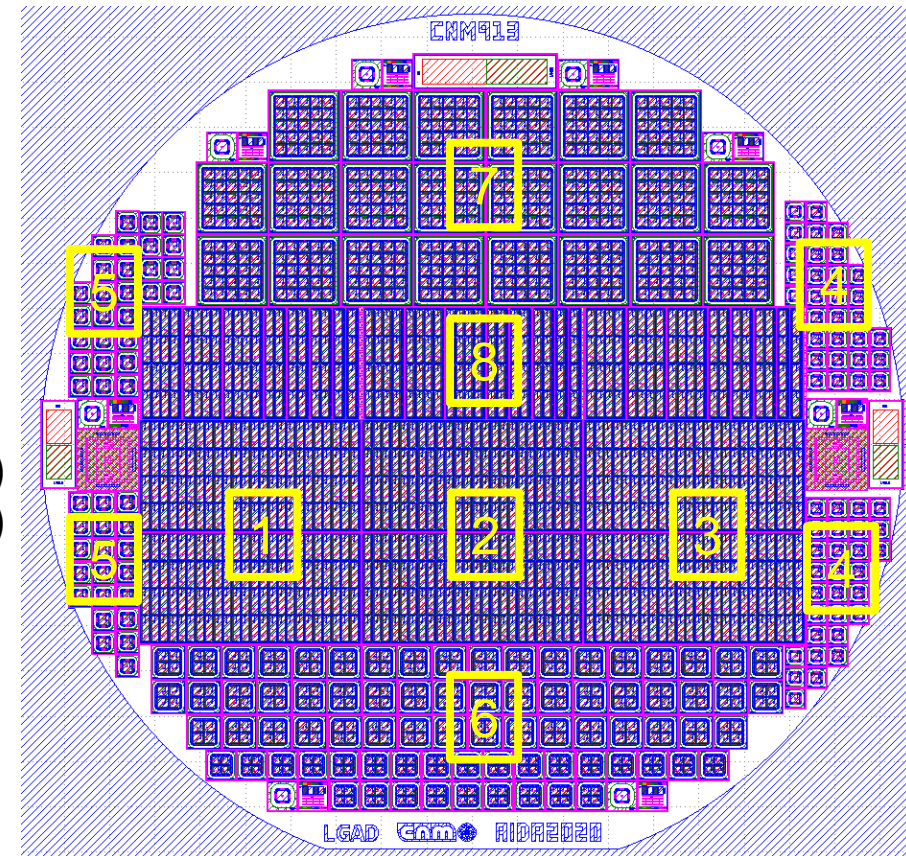
- ✓ Si-Si 4" wafers (35-50  $\mu\text{m}$  High-Res)
- ✓ JTE all structures (5, 10, 15  $\mu\text{m}$  width, 37, 47, 57  $\mu\text{m}$  Inter-Pad distance)
- ✓ 1.3 x 1.3 and 1.0 x 1.0  $\text{mm}^2$  pitch
- ✓ 6 CMS-LGAD sensors in 4x24 matrix design
- ✓ 3 CMS-LGAD sensors in 4x4, 4x2 and 4x1 matrix design
- ✓ 100 ATLAS-LGAD sensors in 5x5 and 2x2 matrix design
- ✓ 108 LGAD PAD sensors
- ✓ Run will be completed by Summer 2018





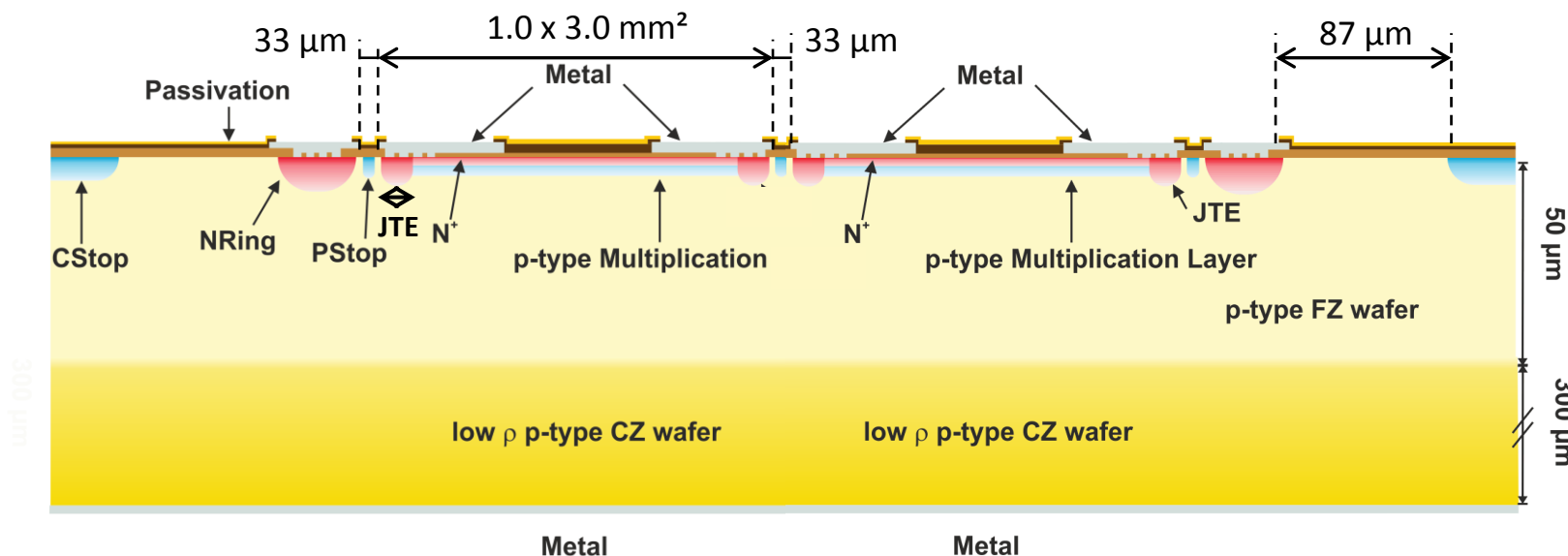
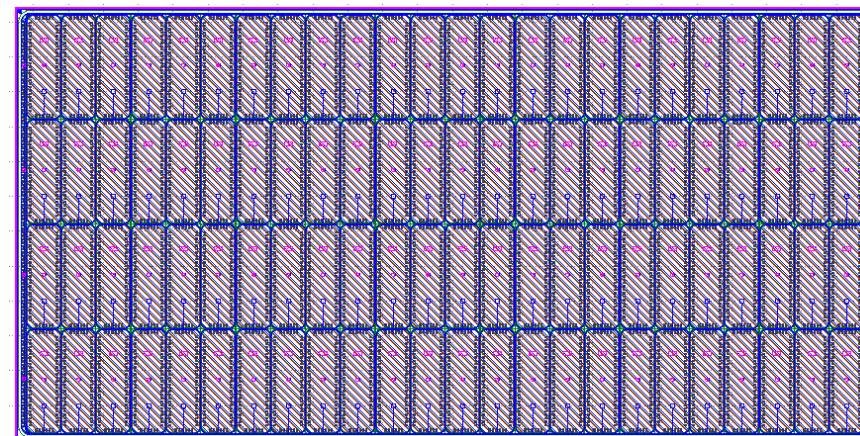
# 4" Thin LGAD 4 AIDA2020 (35-50 $\mu\text{m}$ thick Si-Si)

- **Run AIDA2020. Chips Distribution. Version 18b**
  - ✓ **JTE** all structures (5, **10**, 15  $\mu\text{m}$  width)
  - ✓ **Inter-Pad distance**: 37, **47**, 57  $\mu\text{m}$
  - ✓ **6x** CMS\_3x1\_4x24\_JTE (1) (2) (3)
  - ✓ **3x** CMS\_3x1\_4xY\_JTE (8)
    - **3x**: 4x4, **3x**: 4x2, **2x**: 4x1
  - ✓ **22x** HGTD\_S\_5x5\_BUMPADS (7)
    - ATLAS HGTD **Array 5x5** (1.3 x 1.3 mm<sup>2</sup>)
  - ✓ **78x** HGTD\_S\_2x2\_BUMPADS (6)
    - **52** ATLAS HGTD **Array 2x2** (1.3 x 1.3 mm<sup>2</sup>)
    - **26** ATLAS HGTD **Array 2x2** (1.0 x 1.0 mm<sup>2</sup>)
  - ✓ **48x** LGAD\_S\_1\_3x1\_3 (5)
    - Area 1.3 x 1.3 mm<sup>2</sup>
    - **10+2** PiN
  - ✓ **60x** LGAD\_S\_1x1 (4)
    - Area 1.0 x 1.0 mm<sup>2</sup>
    - **18+2** PiN
  - ✓ **2x** SPR\_QUAD, **1x** 4POINTS, **8x** CNM913\_TEST



# 4" Thin LGAD 4 AIDA2020 (35-50 μm thick Si-Si)

- Run AIDA2020. CNM913. Version 18b. CMS
  - ✓ 6x CMS\_CT\_PPS\_3x1\_4x24\_JTE
    - JTE = 5 μm, IP = 37 μm
    - JTE = 10 μm, IP = 47 μm
    - JTE = 15 μm, IP = 57 μm
    - **3x**: 4x4, **3x**: 4x2, **2x**: 4x1
    - P-type Multiplication Layer **Area Variation** with JTE (low JTE, high multiplication area)
    - **Fill Factor** will be increased

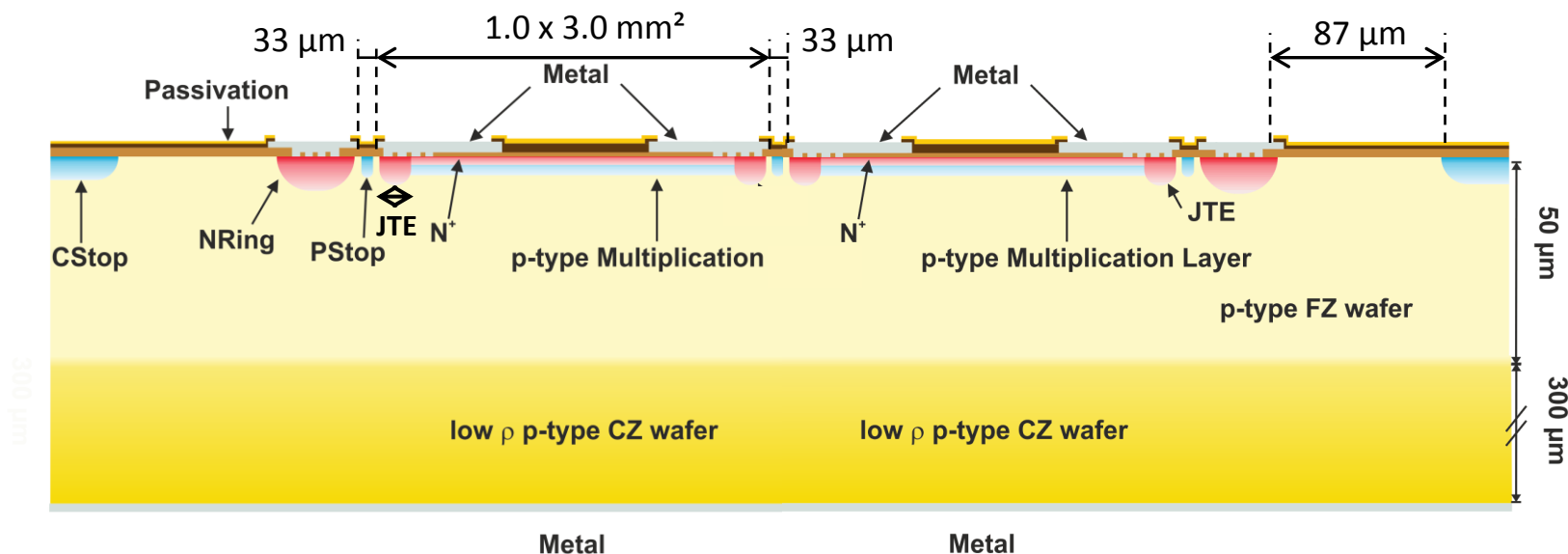
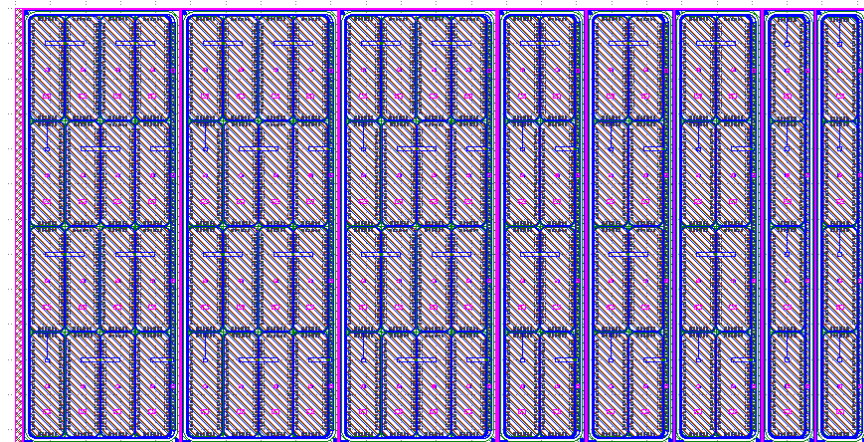


# 4" Thin LGAD 4 AIDA2020 (35-50 μm thick Si-Si)

○ Run AIDA2020. CNM913. Version 18b. CMS

✓ 6x CMS\_CT\_PPS\_3x1\_4x24\_JTE

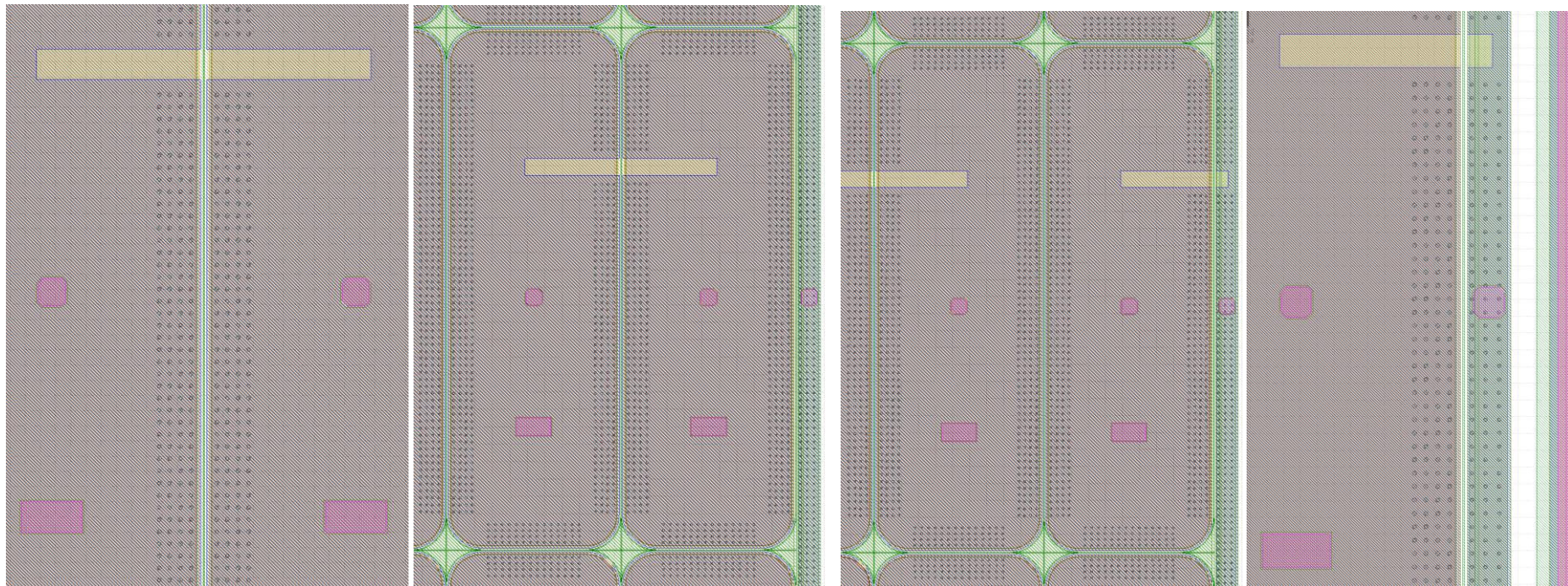
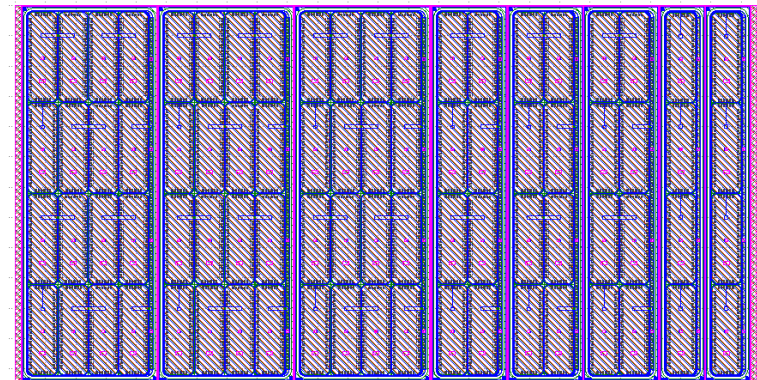
- JTE = 5 μm, IP = 37 μm
- JTE = 10 μm, IP = 47 μm
- JTE = 15 μm, IP = 57 μm
- **3x: 4x4, 3x: 4x2, 2x: 4x1**
- P-type Multiplication Layer **Area Variation** with JTE (low JTE, high multiplication area)
- **Fill Factor** will be increased





# 4" Thin LGAD 4 AIDA2020 (35-50 $\mu\text{m}$ thick Si-Si)

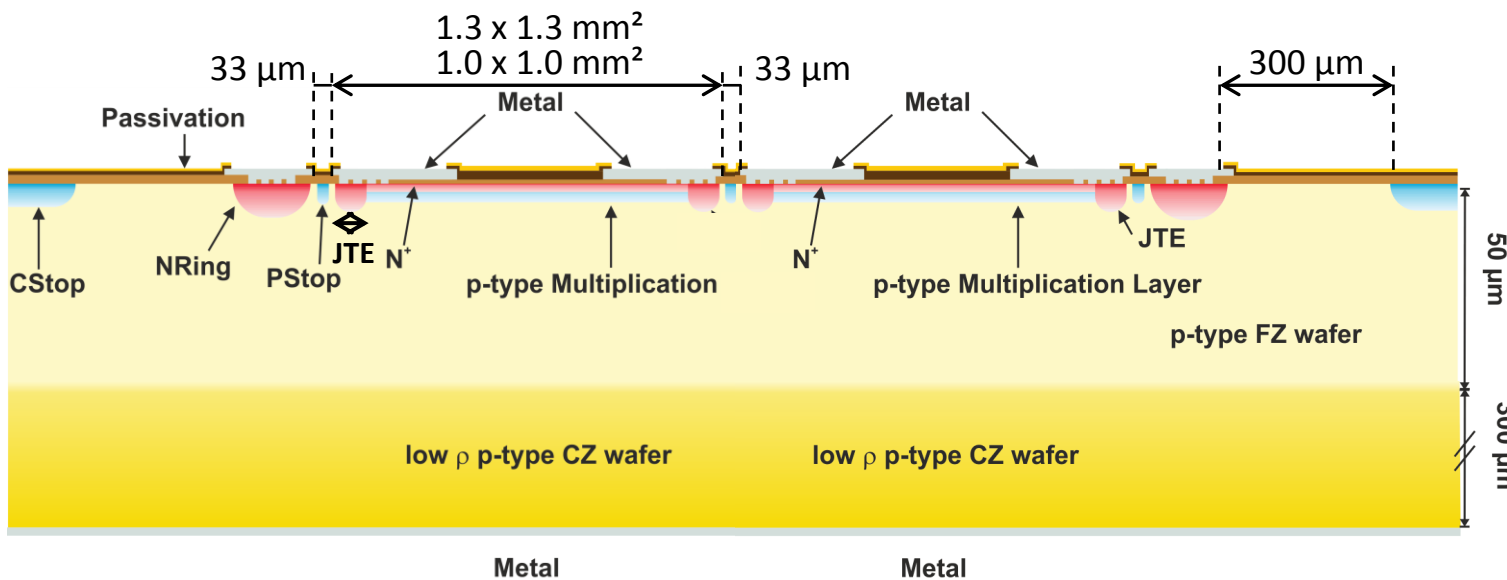
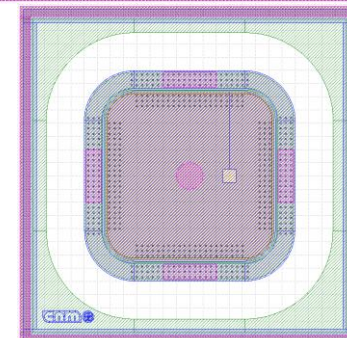
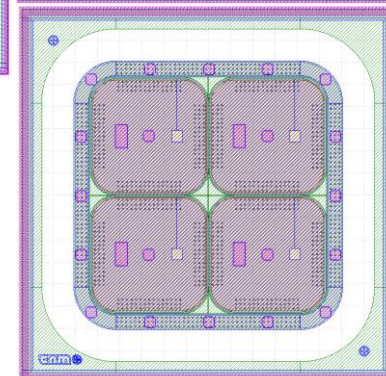
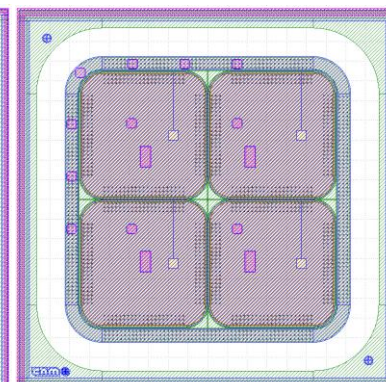
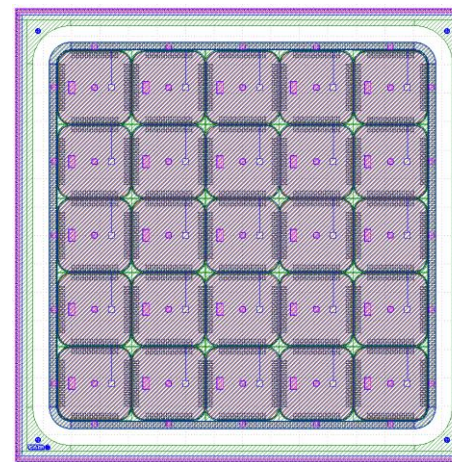
- Run AIDA2020. CNM913. Version 18b. CMS
  - ✓ 3x CMS\_CT\_PPS\_3x1\_4xY\_JTE
    - 3x: 4x4, 3x: 4x2, 2x: 4x1
    - Metal Layer Opening for Laser Measurements
      - Gain @ Adjacent Pixels
      - Gain @ Periphery





# 4" Thin LGAD 4 AIDA2020 (35-50 μm thick Si-Si)

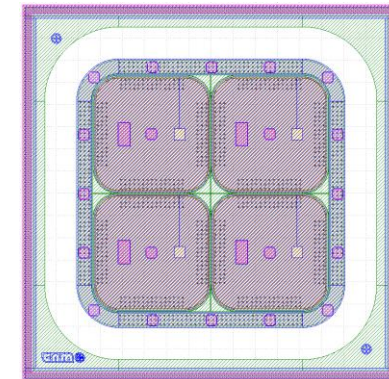
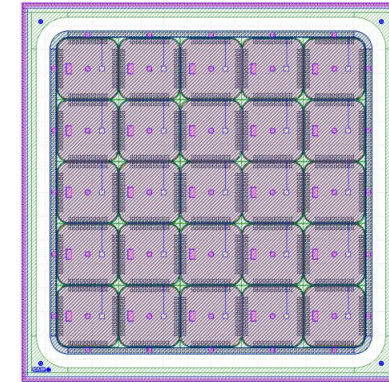
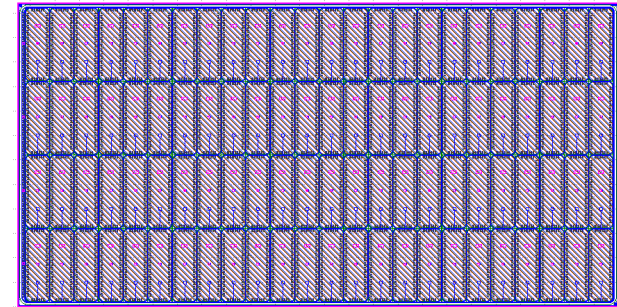
- Run AIDA2020. CNM913. Version 18b. ATLAS
  - ✓ HGTD 2x2 Arrays for first version of readout chip
    - ALTIROC1
  - ✓ UBM opening for bumps
    - Passivation opening of 90 μm
  - ✓ Large opening for wire-bond + probe
    - 200 x 100 μm<sup>2</sup>
  - ✓ An open window in the top metal layer for Laser characterization
    - 100 x 100 μm<sup>2</sup>



# 4" Thin LGAD 4 AIDA2020 (35-50 $\mu\text{m}$ thick Si-Si)

## ○ Run 11748. AIDA2020

- ✓ **14 Si-Si** 4" wafers (35-50  $\mu\text{m}$  High-Res)
- ✓ **9 Mask Levels** (CNM913)
- ✓ **JTE** all structures (5, **10**, 15  $\mu\text{m}$  width)
- ✓ **Boron** multiplication layer
- ✓ **100** Fabrication Steps
- ✓ An **open window** in the top metal layer for **Laser** characterization (100x100  $\mu\text{m}^2$ )
- ✓ **Temporary metal** layer for matrix devices electrical characterization (shorting all pixels)
- ✓ Run **has started** in April 12<sup>th</sup> 2018
- ✓ Run **will be completed** by August 2018

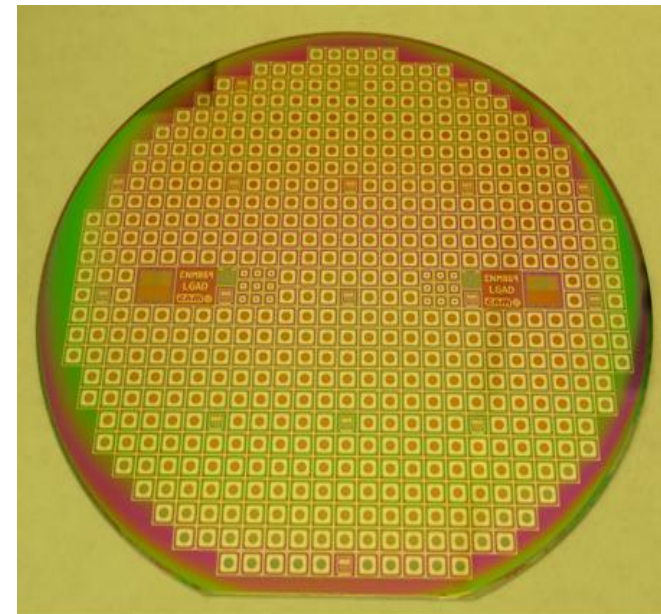




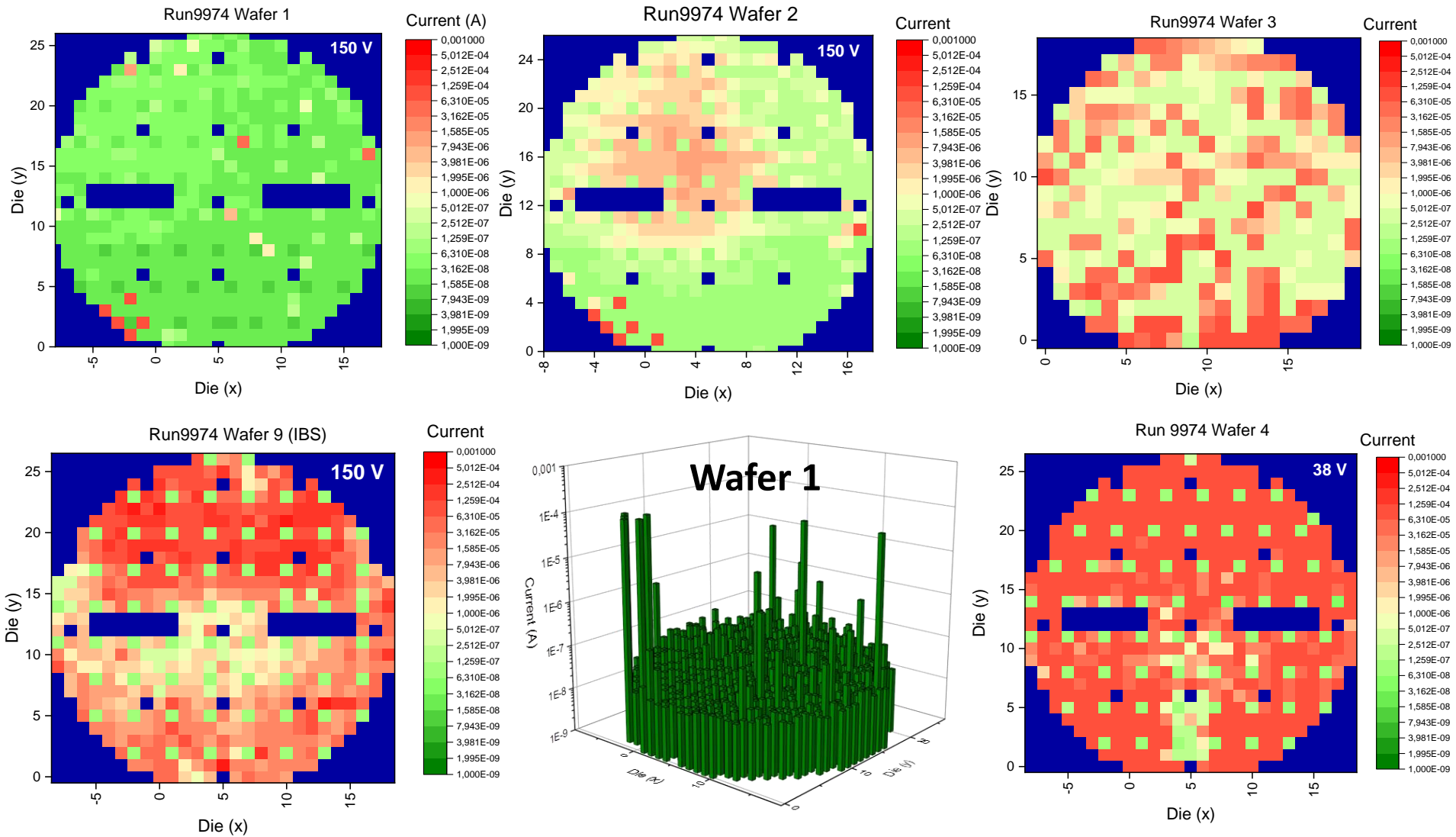
# First 6" LGAD (300 $\mu\text{m}$ thick, Run 9974)

- **New LGAD batch on 6" wafers. Run 9974**
  - ✓ **15 wafers**, **300  $\mu\text{m}$  thick**, high resistivity p-type FZ
  - ✓ Small diodes **5x5 mm<sup>2</sup>** (with **3.3x3.3 mm<sup>2</sup>** test structures)
  - ✓ Multiplication area **3x3 mm<sup>2</sup>** (**1x1 mm<sup>2</sup>**)
  - ✓ **6 different** multiplication layer implant doses
  - ✓ 6" wafers have to be processed in a **different ion implanter** (IBS and CNM) **and furnace**
  - ✓ Re-calibrated **Drive-in**
  - ✓ Re-calibrated **Implantation Energy and Dose**
  - ✓ Run started **November 2016**
  - ✓ Design optimized for **Automatic probe station** measurements
  - ✓ Run completed in **July 2017**
  - ✓ **Electrical characterization done**
  - ✓ **All wafers diced**

✓	<b>472</b>	LGAD 5x5 mm <sup>2</sup>
✓	<b>64</b>	PIN 5x5 mm <sup>2</sup>
✓	<b>16</b>	LGAD 3x3 mm <sup>2</sup>
✓	<b>2</b>	PIN 3x3 mm <sup>2</sup>
✓	<b>561</b>	Devices



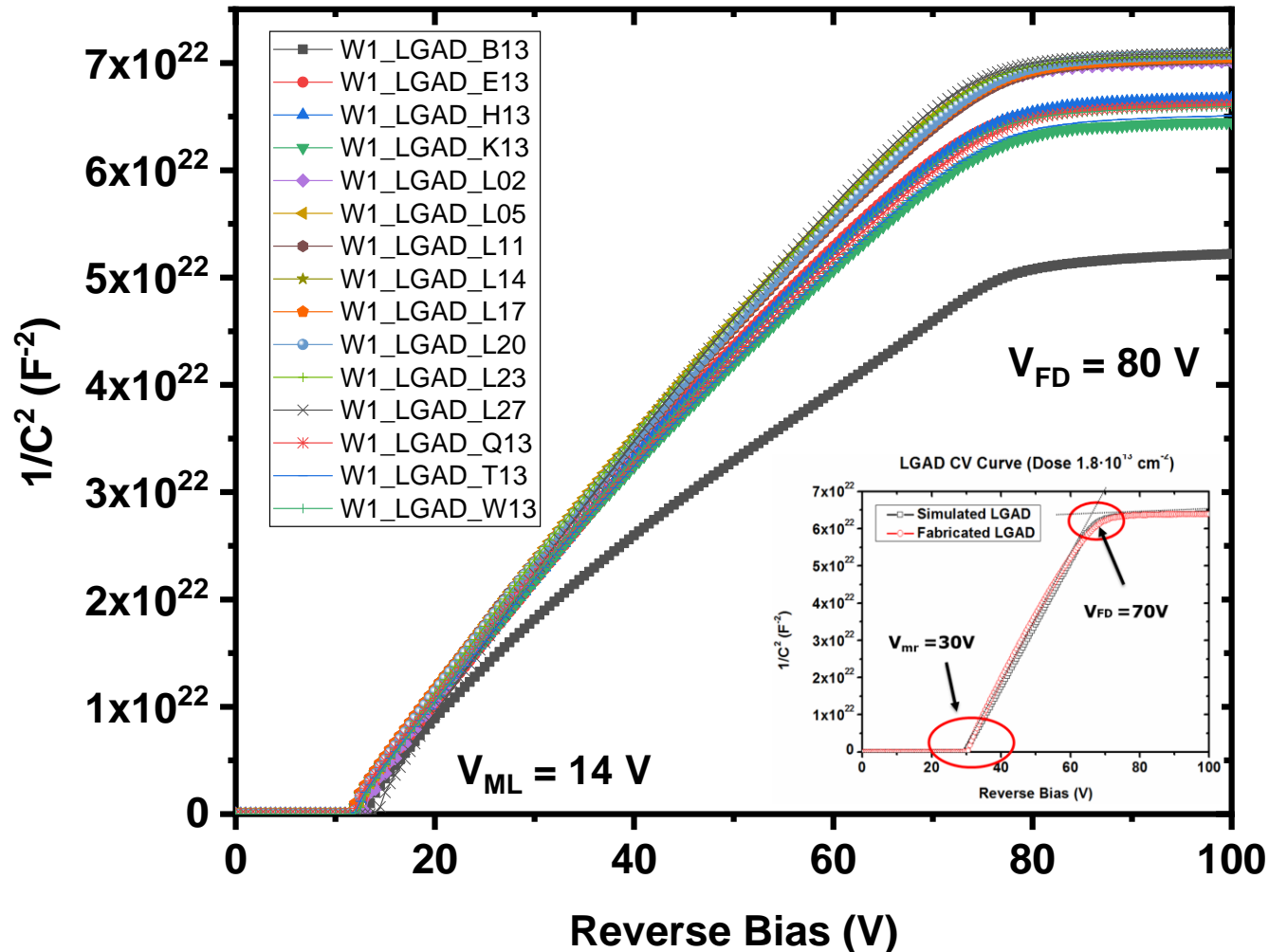
# First 6" LGAD (300 $\mu\text{m}$ thick, Run 9974, IV)





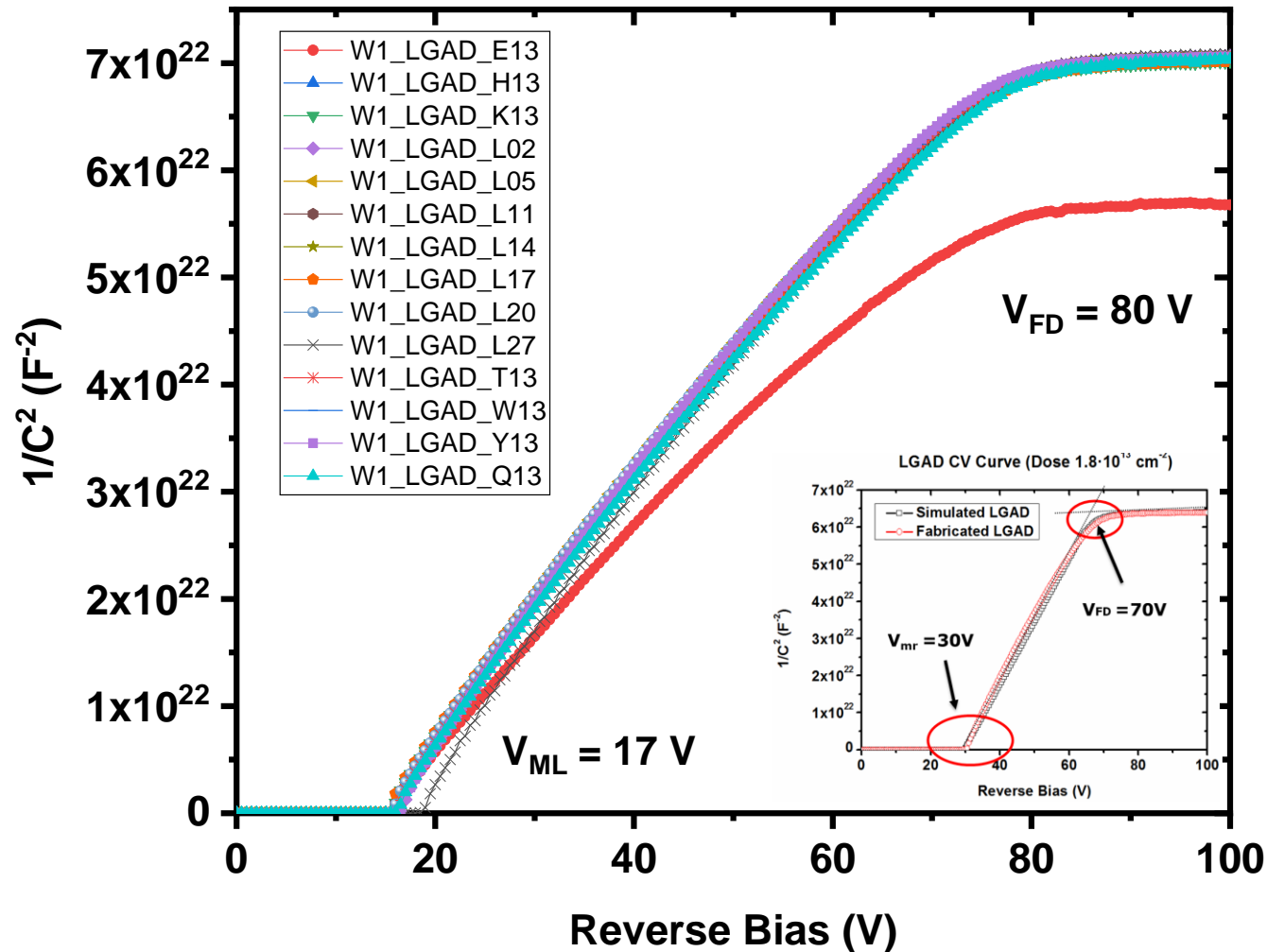
# First 6" LGAD (300 μm thick, Run 9974, CV)

## Run 9974 LGAD 6" Wafer 1



# First 6" LGAD (300 μm thick, Run 9974, CV)

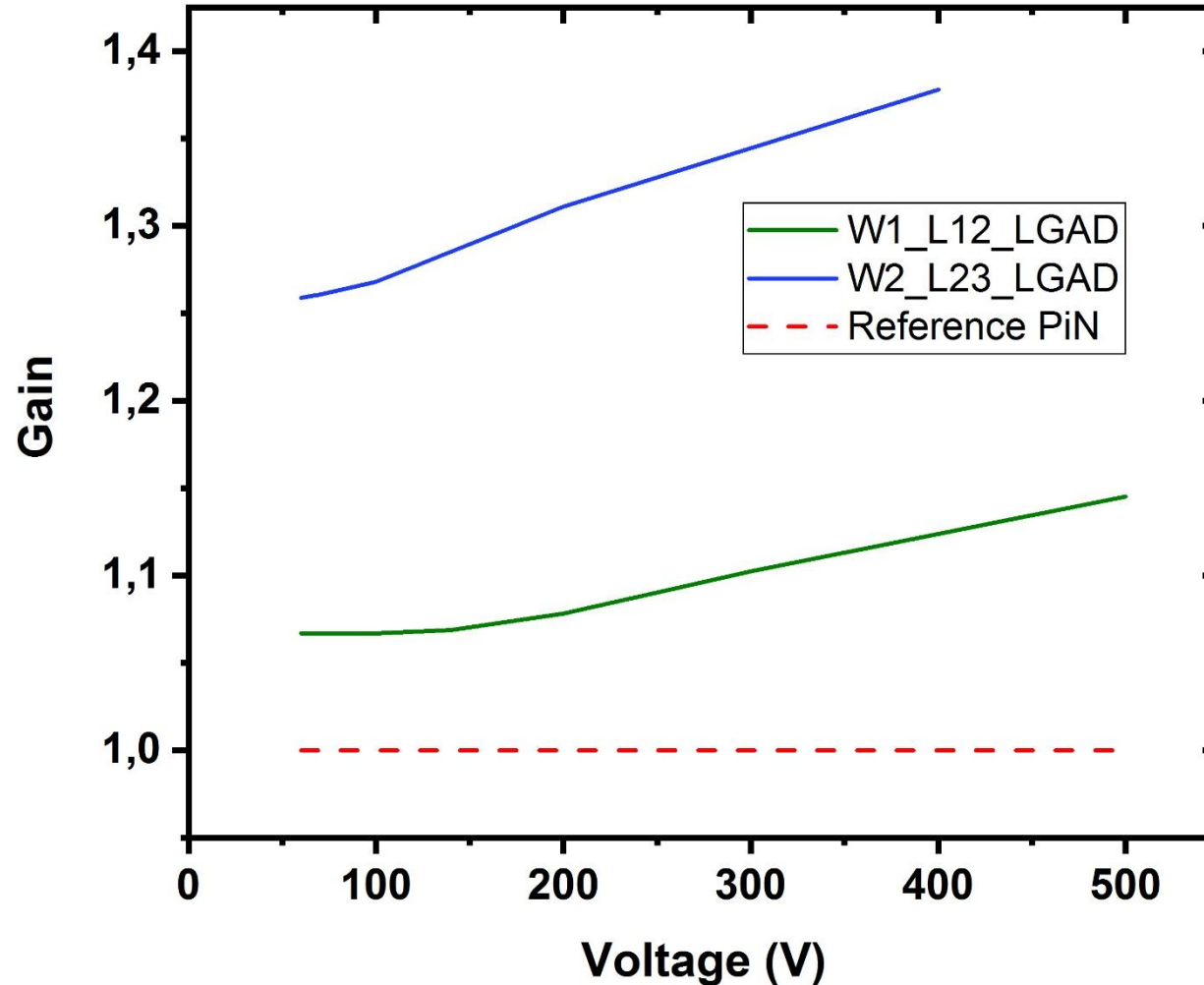
## Run 9974 LGAD 6" Wafer 2





# First 6" LGAD (300 $\mu\text{m}$ thick, Run 9974, TriAlfa)

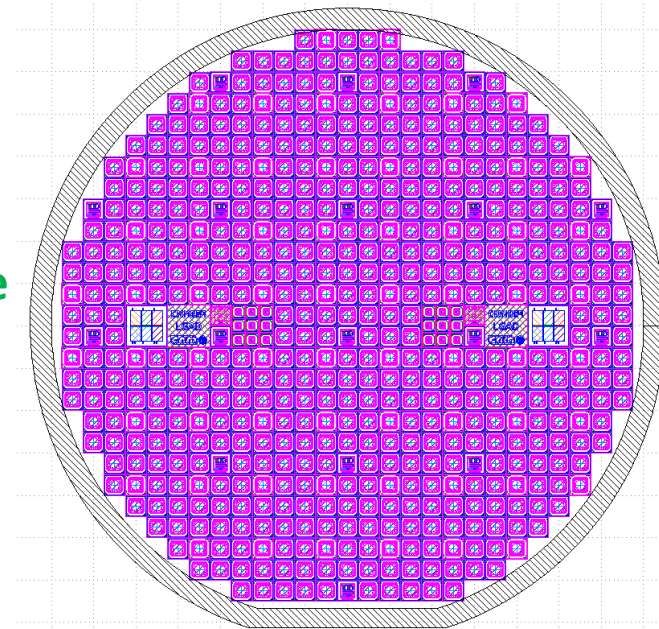
## Run9974 W1 and W2 Alpha Particle Irradiation



# First 6" Thin LGAD (50-1-300 $\mu\text{m}$ SOI wafers)

## ○ Run 11486

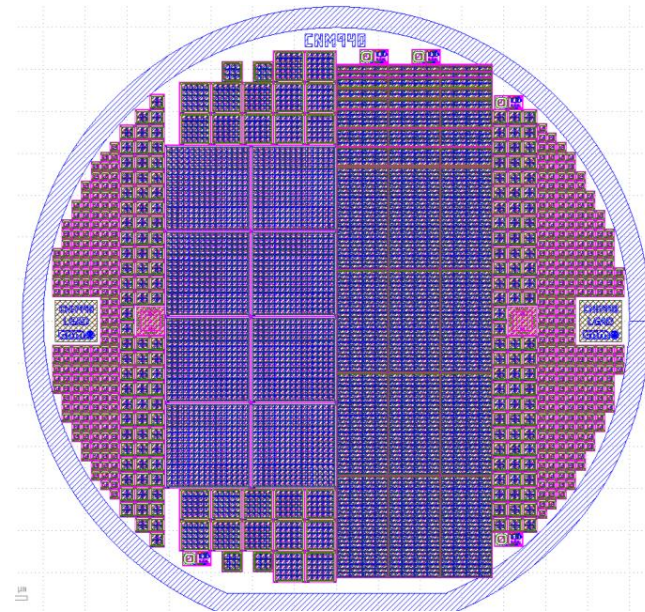
- ✓ Based on Run 9974 results
- ✓ 7 wafers high resistivity p-type FZ
- ✓ This is a calibration LGAD run in 6" SOI wafers
- ✓ Setting of the multiplication layer implantation process
  - Re-calibrated Implantation Energy and Dose
- ✓ CNM869 mask set
- ✓ Small PIN + LGADs 5x5 mm<sup>2</sup>
- ✓ Design optimized for Automatic probe station measurements
- ✓ 100 Fabrication steps. 30 Steps done
- ✓ Run started in February 2018
- ✓ Run will be completed by July 2018





# 6" Thin LGAD 4 ATLAS/CMS (35-50 $\mu\text{m}$ thick Si-Si)

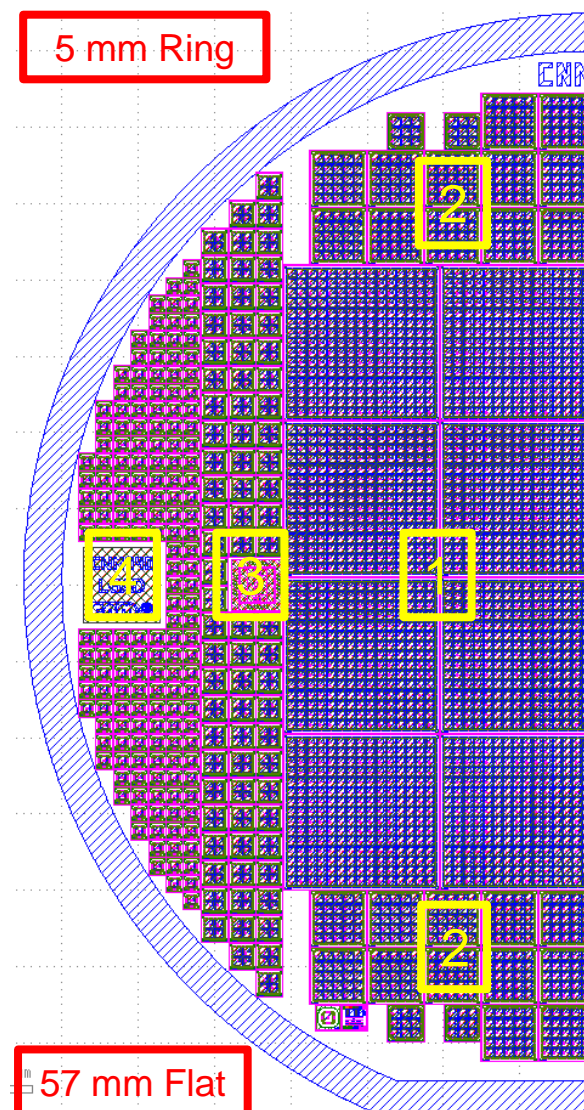
- **Common Run ATLAS/CMS. CNM940 v7**
  - ✓ 150 mm wafer
  - ✓ 35-50  $\mu\text{m}$  thick **Si-Si** (5+10 wafers)
  - ✓ Layout proposed by **ATLAS-HGTD** and **CMS-ETL**
  - ✓ Timing detectors with **Pad** and **Array** designs
  - ✓ Change **standard Slim Edge** to **500  $\mu\text{m}$**  (instead of 650  $\mu\text{m}$ )
  - ✓ **3 Slim Edge** variations: **500, 300, 200  $\mu\text{m}$**  (called **SE5, SE3, SE2**)
  - ✓ **3 Inter-Pad Gaps**: **37, 47, 57  $\mu\text{m}$**  (corresponding to JTE 5, 10, 15  $\mu\text{m}$ ), called **IP37, IP47, IP57**
  - ✓ **Same positions** of large probe pads for **common probe card** between HPK+CNM
  - ✓ Wafers were **purchased** in **January 2018** and will **arrive** in **August 2018**
  - ✓ Run **will be completed** in **Q4 2018**



# 6" Thin LGAD 4 ATLAS/CMS (35-50 $\mu\text{m}$ thick Si-Si)

- **Common Run ATLAS/CMS. CNM940 v7**  
**150 mm Wafer. ATLAS-HGTD Half Wafer**

- ✓ **8x ATLAS\_15x15 (1)**
- ✓ **24x ATLAS\_5x5 (2)**
- ✓ **4x ATLAS\_3x3 (Void)**
- ✓ **80x ATLAS\_1.3x1.3\_2x2 (3)**
- ✓ **170x ATLAS\_1.3x1.3\_1x1 (4)**
- ✓ **1x SPR\_QUAD, 1x 4POINTS**
- ✓ **4x CNM940\_TEST**
- ✓ **Some Metal vs. No-Metal type structures for comparison (a la HPK)**



# 6" Thin LGAD 4 ATLAS/CMS (35-50 $\mu\text{m}$ thick Si-Si)

## CNM Test Structures Table: ATLAS

- 33 Inter-pad gaps: IP57/ 47/ 37 = 57, 47, 37  $\mu\text{m}$
- Slim-edges: SE5/ 3/ 2 = 500, 300, 200  $\mu\text{m}$

Devices per wafer						
Type	Variation	Edge [um]	IP Gap [um]	Fraction [%] of devices/type	Total #/type	#devices
Single Pad	PIN1-SE5	500	-	10	?	?
	LG1-SE5	500	-	50		
	LG1-SE3	300	-	20		
	LG1-SE2	200	-	20		
2x2 arrays	PIN2x2-SE5	500	PIN	10	?	?
	LG2x2-SE5-IP47	500	47	30		
	LG2x2-SE3-IP47	300	47	10		
	LG2x2-SE2-IP47	200	47	10		
	LG2x2-SE5-IP37	500	37	10		
	LG2x2-SE5-IP57	500	57	10		
	LG2x2-SE3-IP37	300	37	10		
	LG2x2-SE2-IP37	200	37	10		
3x3 arrays	LG3x3-SE5-IP47	500	47	100	4	4
5x5 arrays	PIN5x5-SE5	500	PIN	17	24	4
	LG5x5-SE5-IP47	500	47	83		20
15x15 arrays	LG15x15-SE5-IP47	500	47	100	8	8

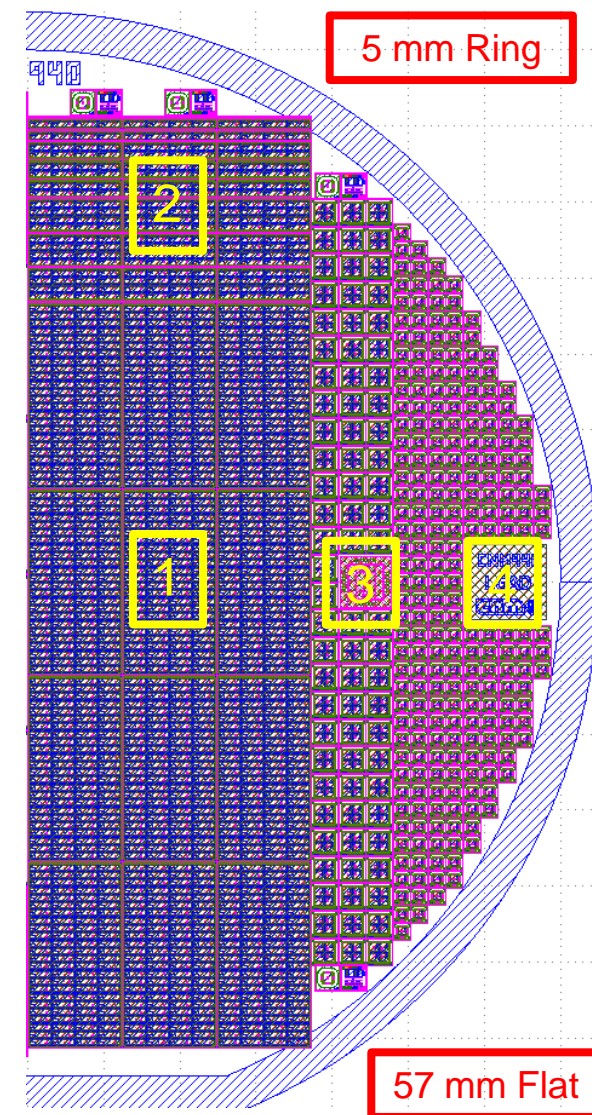
From Joern Lange



# 6" Thin LGAD 4 ATLAS/CMS (35-50 $\mu\text{m}$ thick Si-Si)

- **Common Run ATLAS/CMS. CNM940 v7.**  
**150 mm Wafer. CMS-ETL Half Wafer**

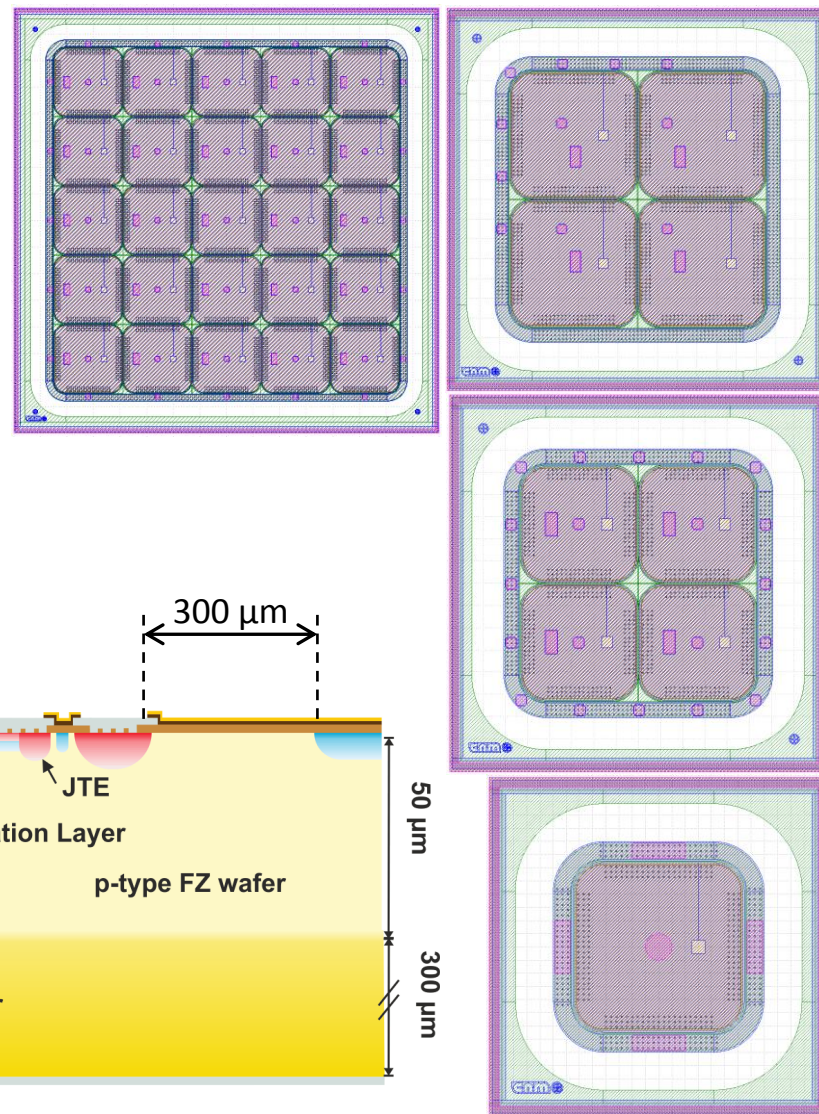
- ✓ **12x** CMS\_3x1\_4x24\_JTE (1)
- ✓ **3x** CMS\_3x1\_4xY\_JTE (2)
  - **3x**: 4x4, **3x**: 4x2, **2x**: 4x1
- ✓ **104x** CMS\_1.3x1.3\_2x2 (3)
- ✓ **100x** CMS\_1.3x1.3\_1x1 (4)
- ✓ Paired **Pin+LGAD** structures
- ✓ **1x** SPR\_QUAD, **1x** 4POINTS
- ✓ **4x** CNM940\_TEST



# 6" Thin LGAD 4 ATLAS/CMS (35-50 $\mu\text{m}$ thick Si-Si)

## Run ATLAS/CMS. CNM940. Version 7. ATLAS

- ✓ HGTD 5x5, 2x2 Arrays first version of readout chip
  - ALTIROC1
- ✓ UBM opening for bumps
  - Passivation opening of 90  $\mu\text{m}$
- ✓ Large opening for wire-bond + probe
  - 200 x 100  $\mu\text{m}^2$
- ✓ An open window in the top metal layer for Laser characterization
  - 100 x 100  $\mu\text{m}^2$

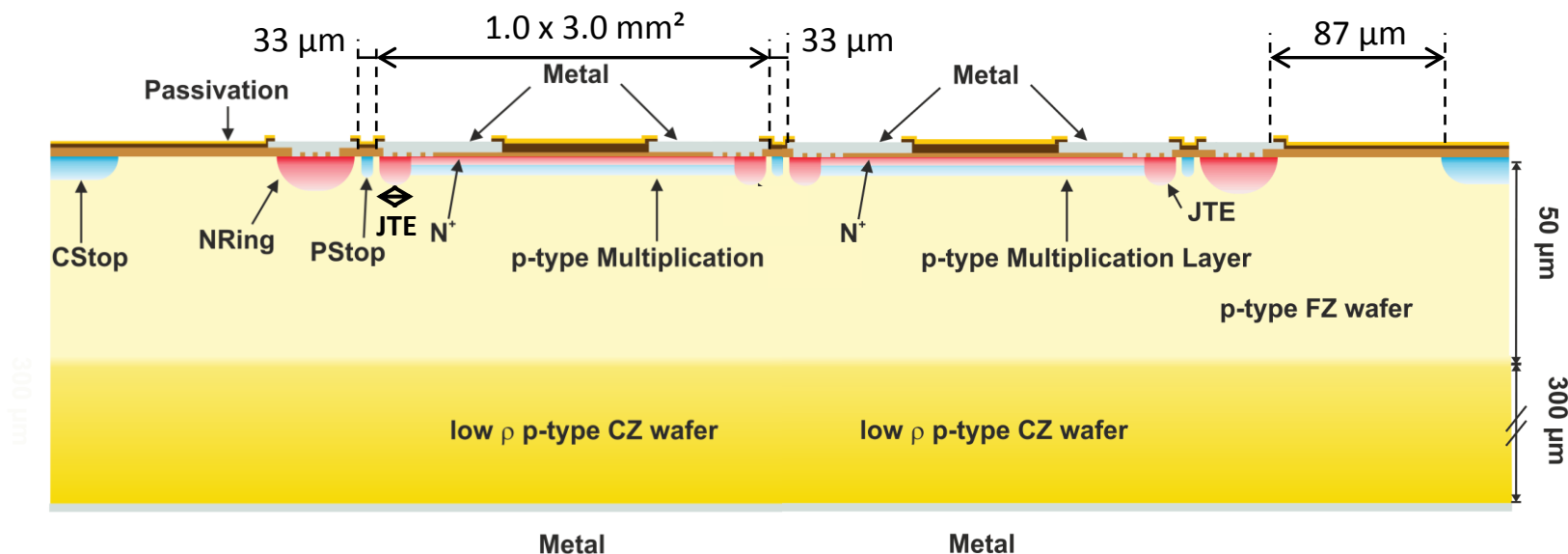
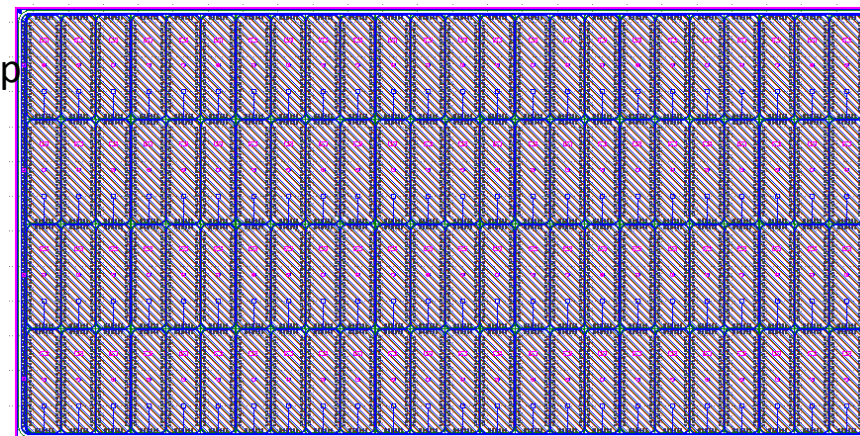




# 6" Thin LGAD 4 ATLAS/CMS (35-50 μm thick Si-Si)

## Run ATLAS/CMS. CNM940. Version 7. CMS

- ✓ HGTD 5x5, 2x2 Arrays first version of readout chips
  - ALTIROC1
- ✓ UBM opening for bumps
  - Passivation opening of 90 μm
- ✓ Large opening for wire-bond + probe
  - 200 x 100 μm<sup>2</sup>
- ✓ An open window in the top metal layer for Laser characterization
  - 100 x 100 μm<sup>2</sup>



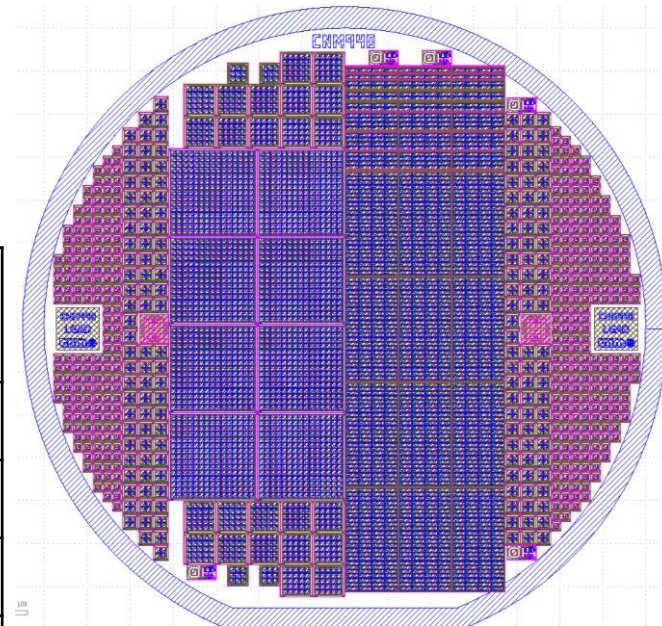


# 6" Thin LGAD 4 ATLAS/CMS (35-50 $\mu\text{m}$ thick Si-Si)

## Common Run ATLAS/CMS. CNM940

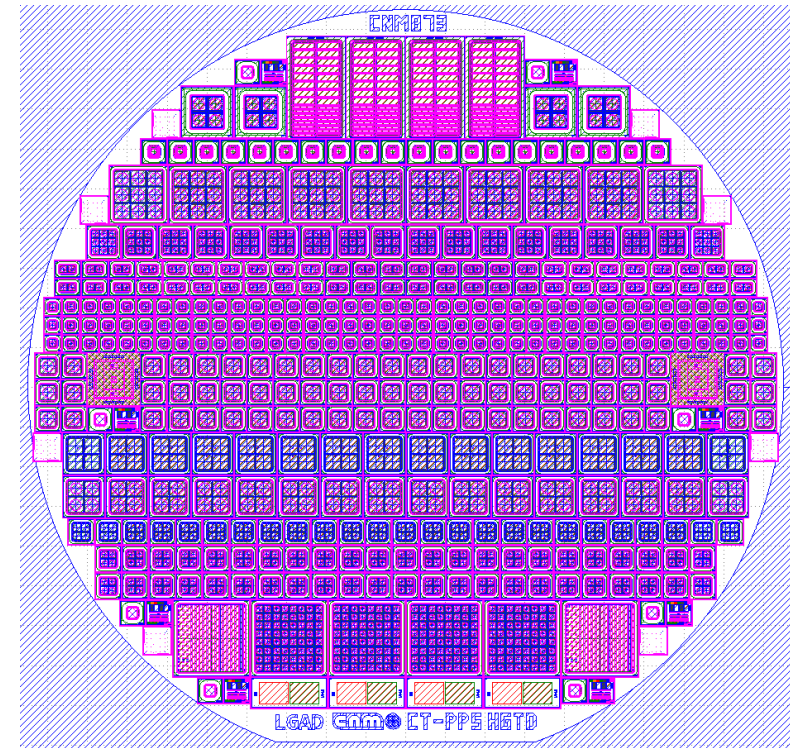
- ✓ 150 mm wafer
- ✓ 35-50  $\mu\text{m}$  thick Si-Si (5+10 wafers)
- ✓ Run 9088 (low dose) is roughly equivalent to HPK 50D ( $V_{\text{BD}} \sim 300 \text{ V}$ )
- ✓ Take this run as baseline

# of Wafers	Thickness [ $\mu\text{m}$ ]	Doping Profile	Carbon?
3	50	"9088 (med)"	no
3	50	"9088 (low)"	no
2	50	Lower than "(low)"	no
2	50	"9088 (low)"	yes
3	35	"9088 (low)"	no
2	35	"9088 (low)"	yes

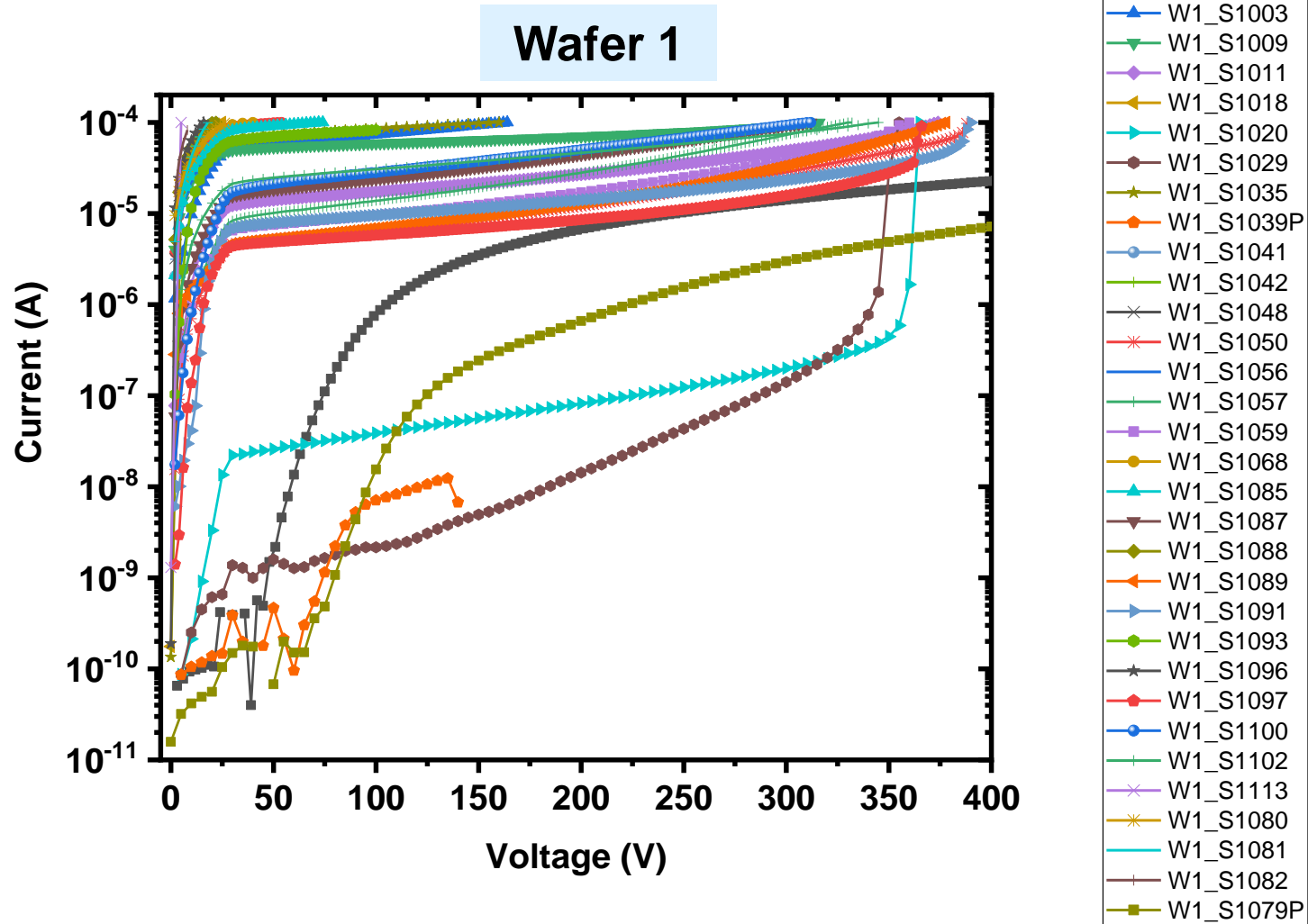


# 4" Thin Gallium LGAD (50-300 $\mu\text{m}$ Si-Si wafers)

- **Run 10924**
  - ✓ Based on **Run 10478** results
  - ✓ **CNM873** mask set
  - ✓ **14 wafers** high resistivity p-type FZ
  - ✓ **Gallium** multiplication layer
    - Re-calibrated **Implantation Energy and Dose**
  - ✓ **80** Fabrication steps. **70** Steps done
  - ✓ Run completed in **May 2018**
  - ✓ **Electrical characterization on going**
  - ✓ **All wafers will be diced**



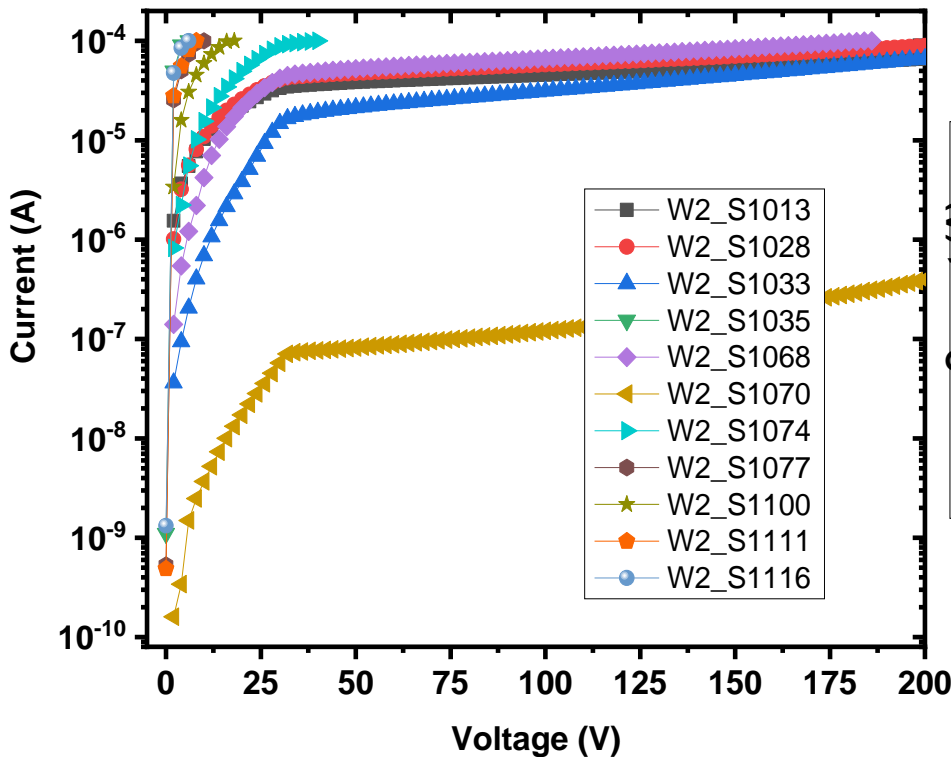
# 4" Thin Gallium LGAD (50-300 μm Si-Si wafers)



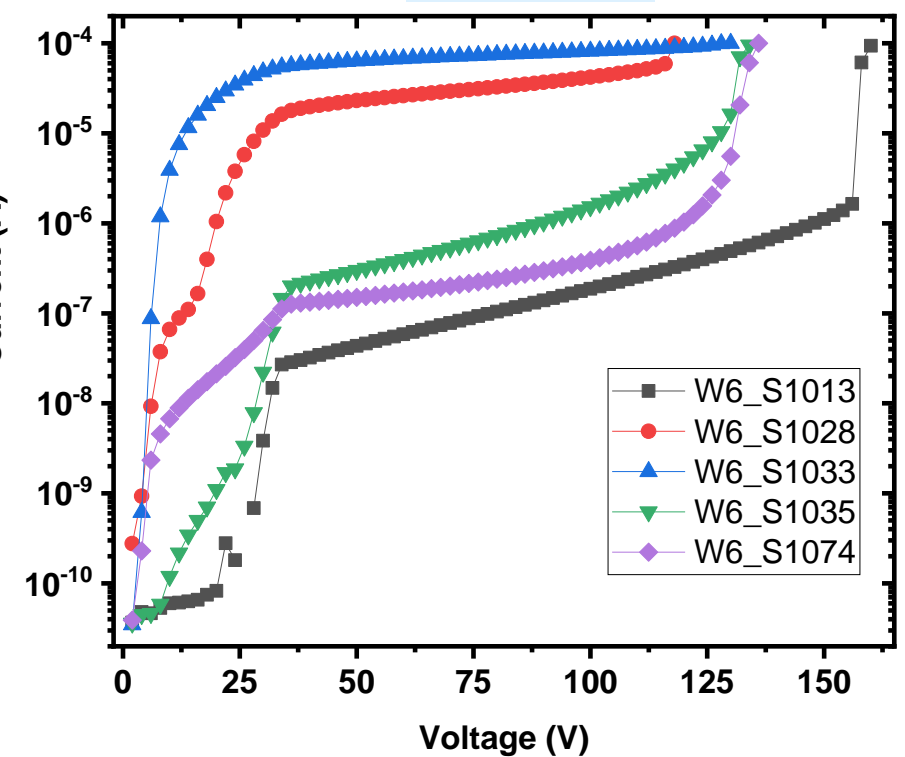


# 4" Thin Gallium LGAD (50-300 μm Si-Si wafers)

Wafer 2



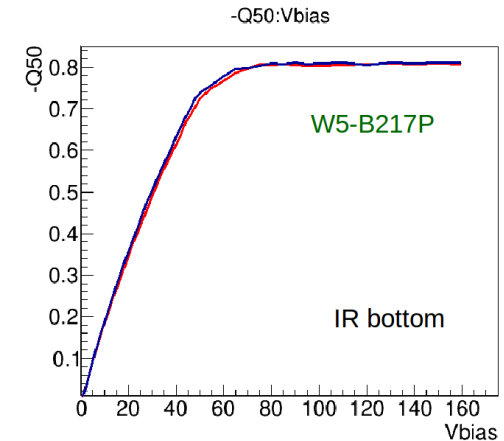
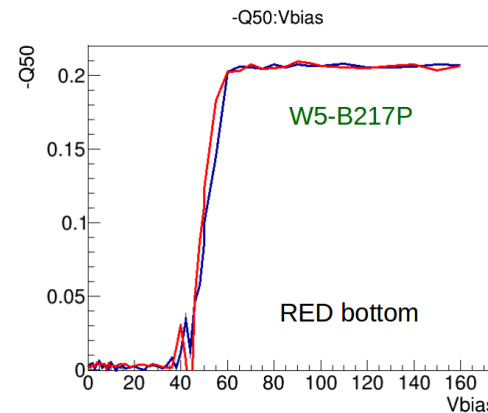
Wafer 6



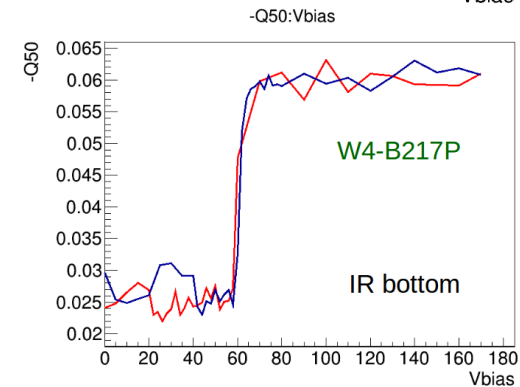
# Run 10478. The Wafer 5 Affair

## ○ TCT Measurements

- ✓ **W4** and **W5** were fabricated using the same fabrication process. W5 has an additional **carbon spray layer** on top
- ✓ **W5-B217P** PiN diode shows **different performances** than **W4-B217P** using RED and IR bottom illumination
- ✓ Optical measurements shows that **W5-B217P** is **285 μm** thick and **W4-B217P** is **350 μm** thick
- ✓ **Si-Si** wafers are **350 μm** thick, **Si** wafers are **285 μm** thick



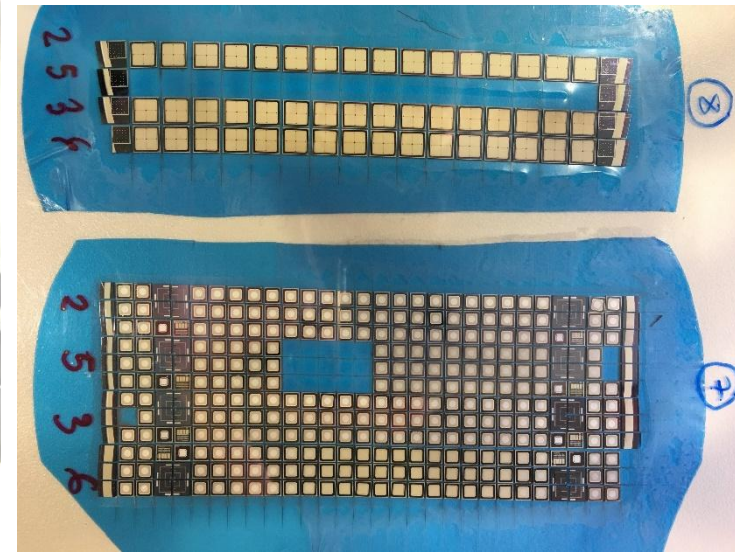
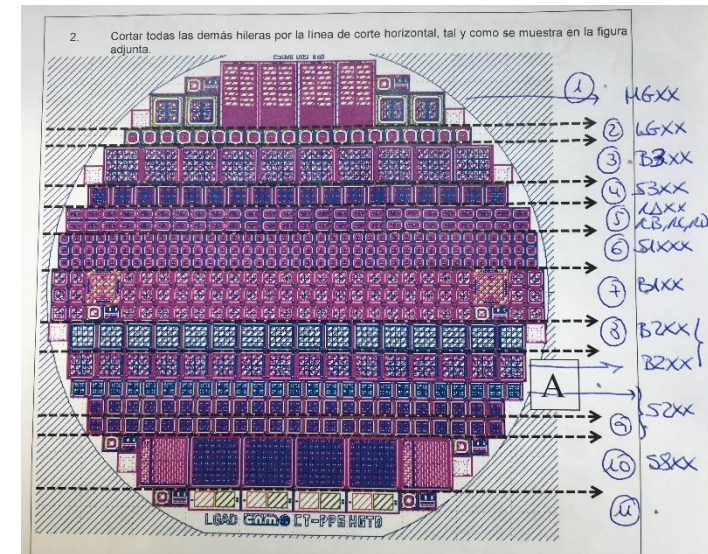
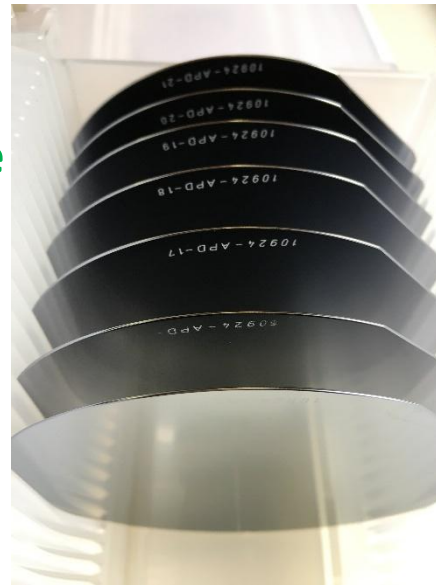
W4-B217P  
RED bottom  
No signal !!



W5-B217P, W4-B217P. TCT Measurements by Esteban Curras (IFCA) at CERN

# Run 10478. The Wafer 5 Affair

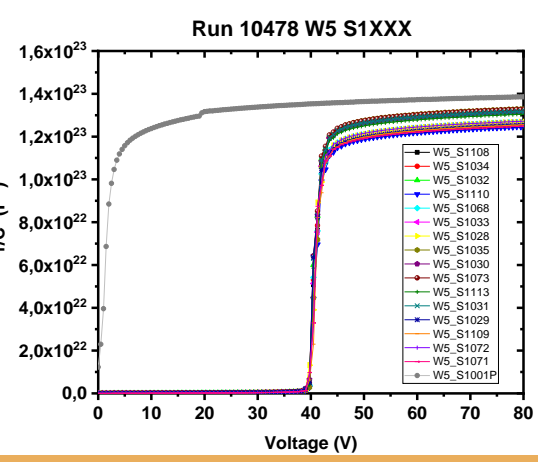
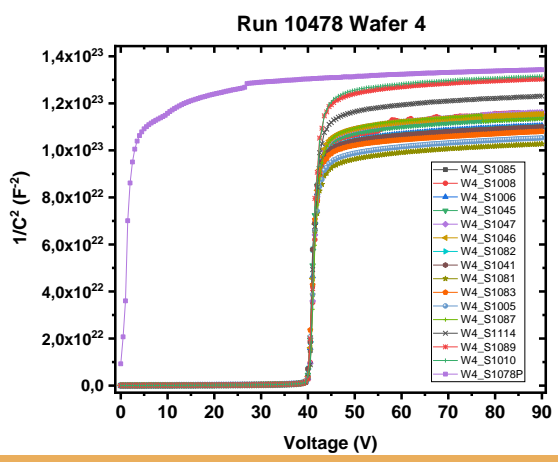
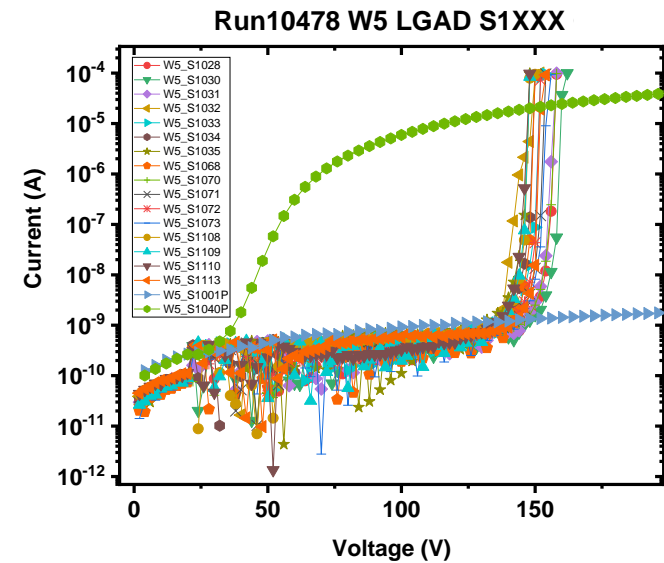
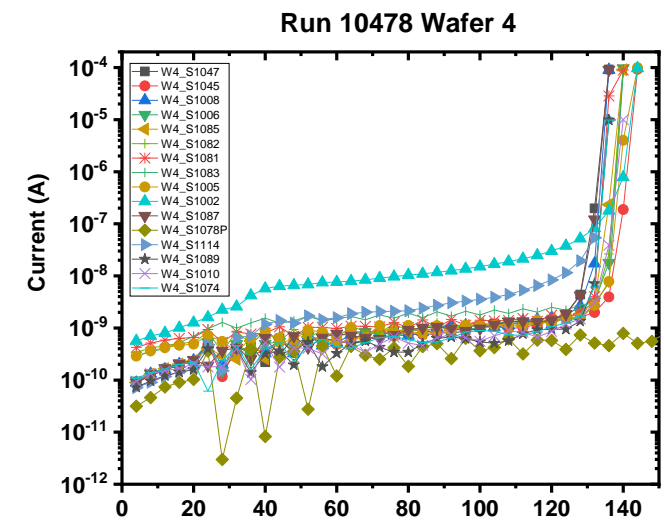
- ✓ During the **fabrication process** all wafers **are clearly identified** using a code defined by a **laser writing machine**
- ✓ **W4** and **W5** were measured **on wafer** by Mar Carulla showing **similar performances** for same devices on each wafer
- ✓ **12 different sets** of devices are integrated **on each wafer**
- ✓ **Several sets** of equivalent devices were **diced at same time**
- ✓ Their **identification** were **done by hand**
- ✓ In this process **W5 was changed with W1**
- ✓ **W5** is already been diced





# Run 10478. Wafer 5 Irradiation Campaigns

- **Proton & Neutron Irradiation Campaigns. Test Beams**
  - ✓ **IFCA: W4** and **W5** samples have been sent to **CERN** to irradiate with protons
  - ✓ **Test Beam:** During the first week of June **W5** samples will be measured at **FERMILAB**
  - ✓ **IFAE: W5** samples will be send to **IJS Ljubljana** to irradiate with neutrons
  - ✓ **W4** and **W5** samples will be send to **KIT** and **SCIPP** to characterize them



## Future work

### ○ Future

- ✓ New run with AC coupled (**AC-LGAD-RD50**). **Mask design**
- ✓ Run 9974. 6" LGAD. Dicing of the wafers and **measurement of gain** in the different **multiplication profiles**
- ✓ Fabrication of **thin LGAD 4 AIDA2020**. Run 11748
- ✓ Fabrication of **50  $\mu\text{m}$  thick LGAD** on **6"** wafers. Run 11486
- ✓ Design and Fabrication of **6" LGAD 4 ATLAS/CMS**
- ✓ Run 10924. **4" Thin Ga-LGAD**. Electrical Characterization



Virtuoso® Layout Editing: CHM2017 thanks layout (on opter12)

X: -1.6 Y: 22.1 (F) Select: 0 DRD: OFF dX: -103.1 dY: -4.8 Dist: 103.21 Cnd: Ruler 2

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Migrate Help

LSW - + x

Sort Edit Help

ME6 drw

UMC\_18\_CMOS

Show Objects

Inst Pin

AV NV AS NS

VINHL drw

NPOLY drw

ESD drw

PESD drw

SAB drw

TG drw

HR drw

CONT drw

P01 drw

P00 drw

VARACT drw

ME1 drw

VI1 drw

ME2 drw

VI2 drw

ME3 drw

VI3 drw

ME4 drw

VI4 drw

ME5 drw

VI5 drw

ME6 drw

MMC drw

0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100.00

CHM Thanks  
for your attention!

mouse L: M: R:

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