Status of HV-CMOS developments within the RD50 collaboration

E. Vilella[a*], O. Alonso[b], R. Casanova[d], G. Casse[a,e], L. Gonella[f], A. Dieguez[b], M. Franks[a], S. Grinstein[b], N. Massari[e], L. Meng[a], F. Muñoz[c], R. Palomo[c], J. Vossebeld[a], C. Zhang[a,e]

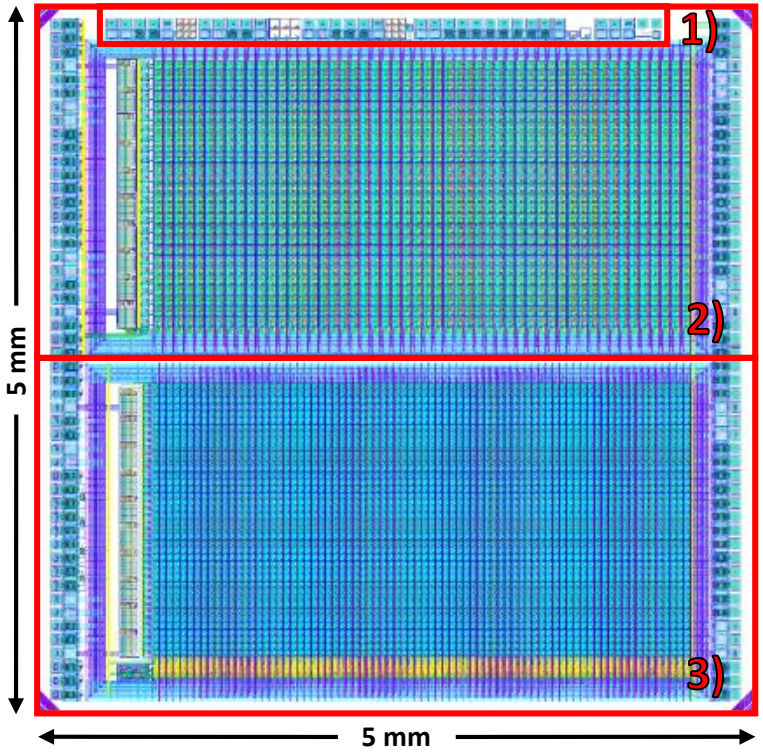
[a]University of Liverpool
[b]Universitat de Barcelona
[c]Universidad de Sevilla
[d]IFAE
[e]FBK
[f]University of Birmingham

[*]vilella@hep.ph.liv.ac.uk

RD50-MPW1

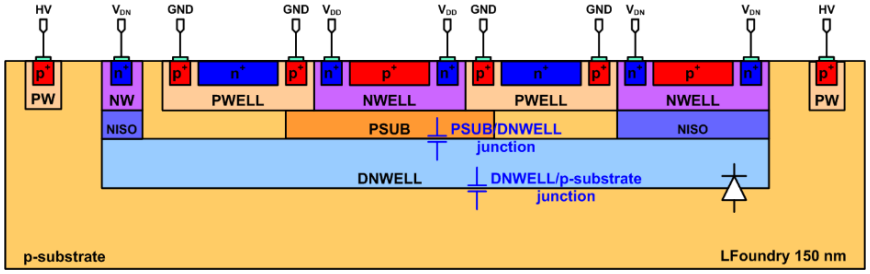
Overview

- MPW in 150 nm HV-CMOS from LFoundry
- Submitted in November 2017, samples just distributed last week
- Designed with PDK LF15A V1.2.0
  - → Models to simulate the sensing diodes
  - → Proper verification
- Manufactured on wafers with different substrate resistivities:
  - → 500 Ω·cm (40 samples) and 1.9k Ω·cm (80 samples)
- Motivation: Test the design aspects of the technology and also implement novel concepts
- Contents:
  1) Test structures for TCT/e-TCT
  2) Matrix of HV-MAPS pixels with 16-bits counter
     26 x 52 pixels
     75 µm x 75 µm pixel area
  3) Matrix of 40 x 78 HV-MAPS pixels with FE-I3 style RO
     40 x 78 pixels
     50 µm x 50 µm pixel area
  - → In both matrices, the analog and digital RO are embedded inside the sensing area
  - → The two matrices are completely independent between them
- DAQ development → See presentation "DAQ development for the characterization of the RD50 HV-CMOS devices" by Ricardo Marco for RD50 development, also IFAE DAQ



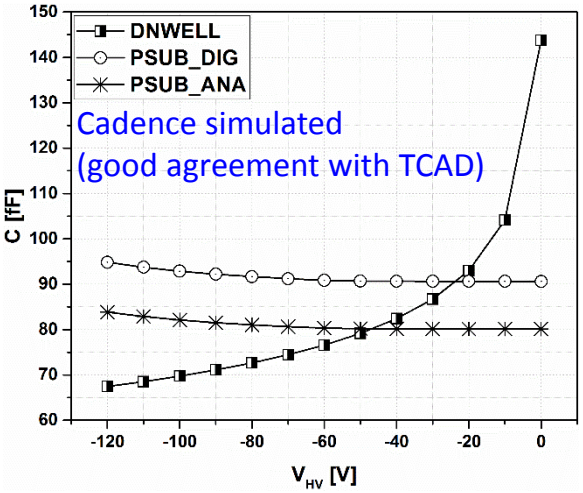
RD50-MPW1 – Sensor

Cross-section



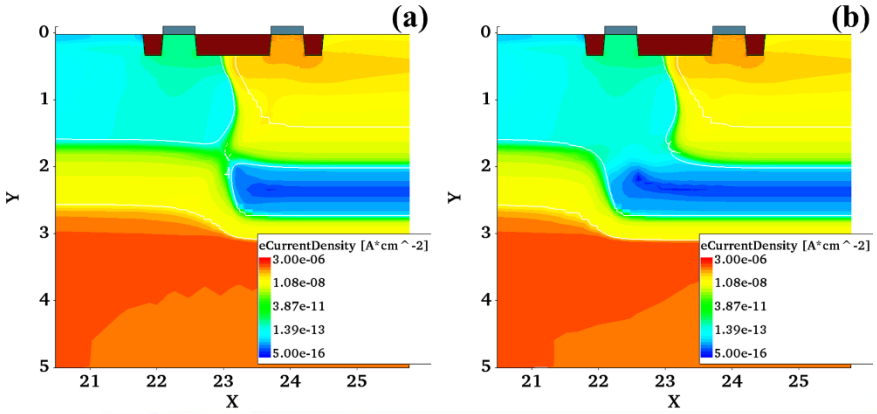
- PSUB → Deep p-well layer to isolate RO electronics from DNWELL
- The PSUB/DNWELL junction has a large contribution to the total capacitance of the sensor (capacitance/area ↑)
- PSUB only covers NWELLs with RO electronics + small (safe) overlap with neighbouring PWELLs to avoid unwanted currents from DNWELL

50 µm x 50 µm pixel capacitance



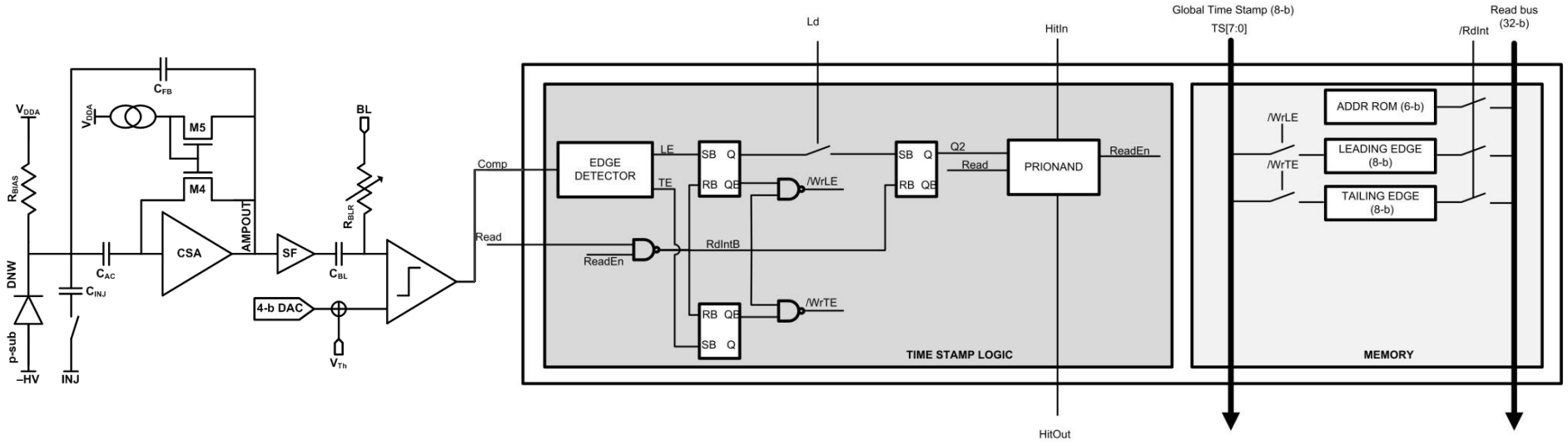
TCAD simulations

(a)
PWELL/PSUB overlap is 0 µm → DNWELL/NWELL current flow (the depletion regions merge)



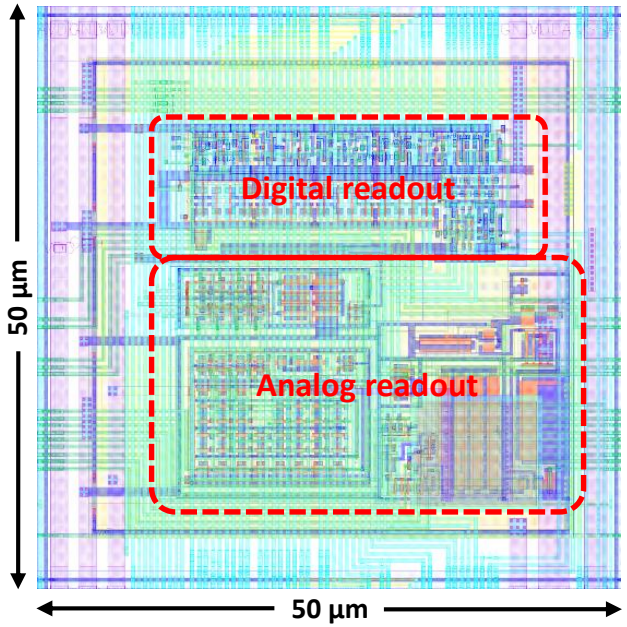
(b)
PWELL/PSUB overlap is 1 µm → DNWELL/NWELL no current flow (the depletion regions don't merge)

RD50-MPW1 – Pixel schematic

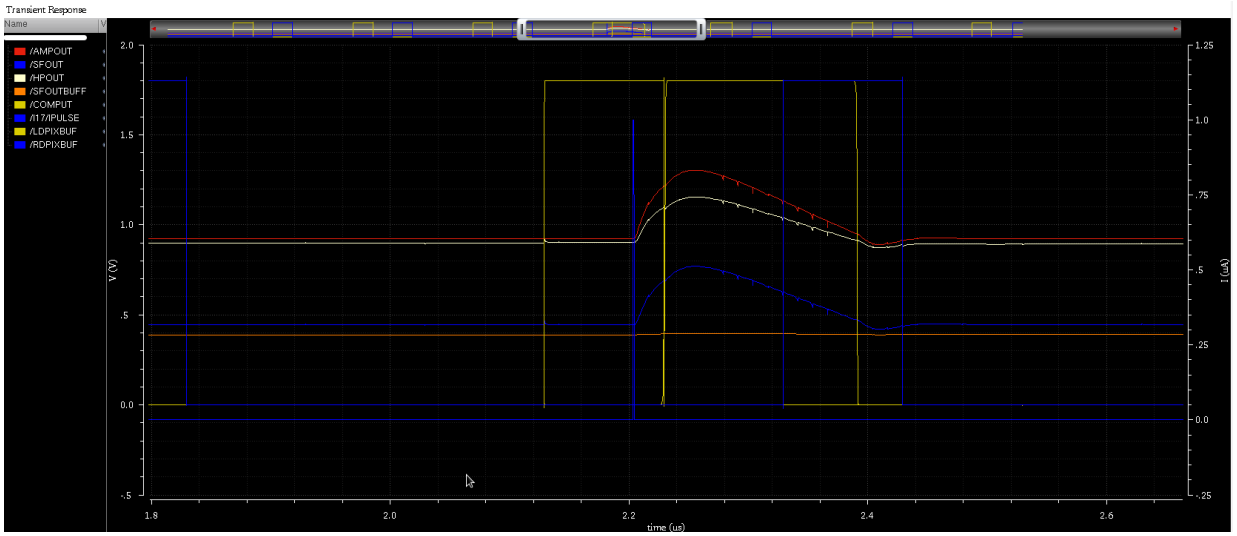


- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - The discriminator has a local 4-bit DAC to compensate for offset variations
- The **digital readout** is based on the FE-I3:
  - **Two 8-bit DRAM memories** that continuously store two time stamps (Leading Edge, Trailing Edge)
  - ToT = TE – LE (off-chip)
  - **One 8-bit ROM memory** to store the pixel address
  - **Electronics (edge detector)** to process the output of the discriminator and tell when the LE and TE have to be stored
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz

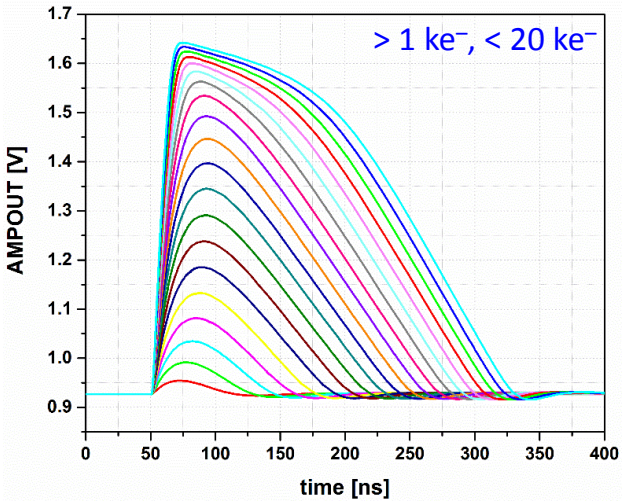
RD50-MPW1 – Layout

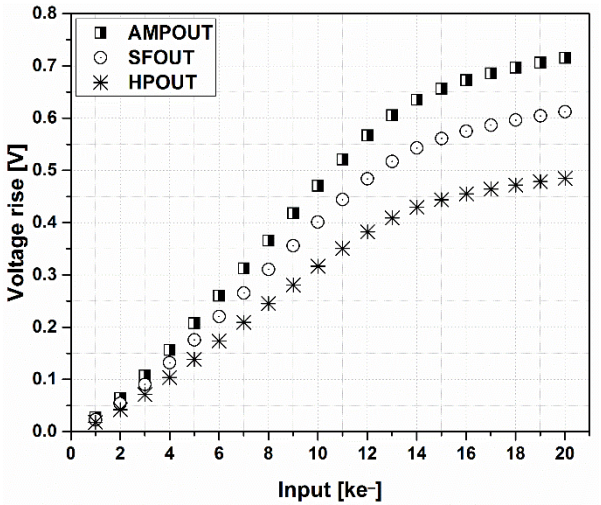


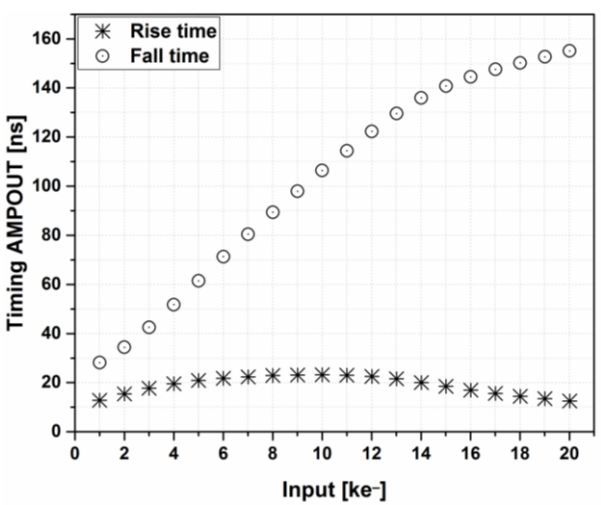
Post-layout simulation of analog and digital readout

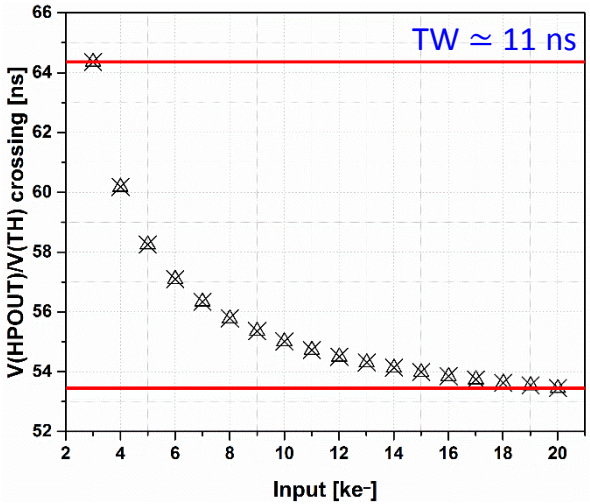


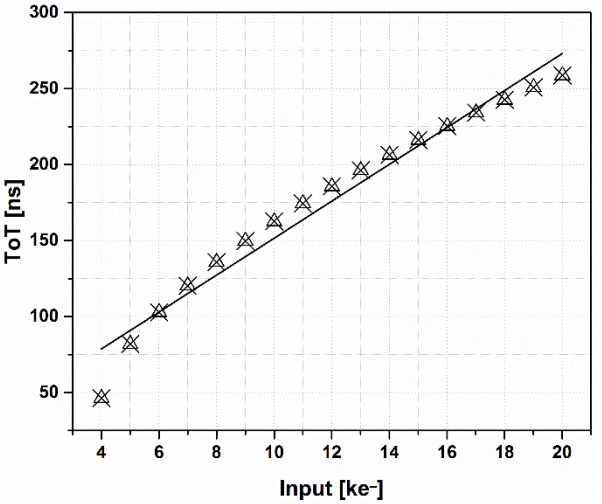
RD50-MPW1 – Post-layout simulations

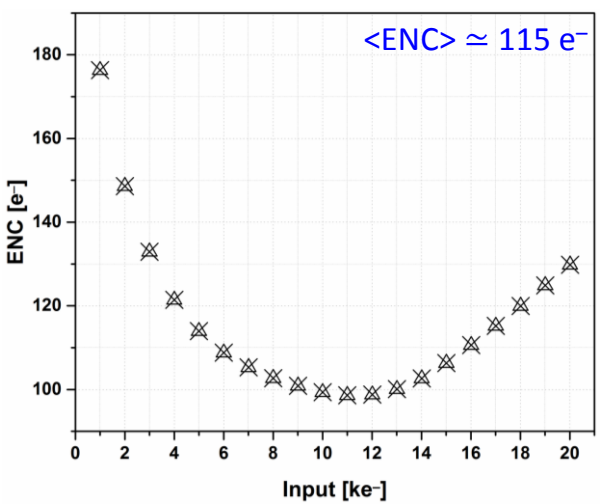




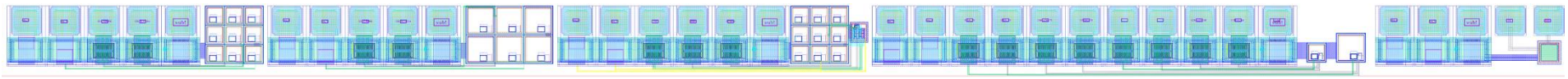








RD50-MPW1 – Test structures



A) TCT/e-TCT/TPA

- 3 x 3 matrix of 50 µm x 50 µm
- HV-CMOS pixels without electronics

B) TCT/e-TCT

- 2 x 3 matrix of 75 µm x 75 µm
- HV-CMOS pixels without electronics

C) Fast measurements (with a laser)

- 3 x 3 matrix of 50 µm x 50 µm
- HV-CMOS pixels

D) Sensor capacitance measurement

- 1 single pixel with 50 µm x 50 µm
- 1 single pixel with 75 µm x 75 µm

E) 1 avalanche photodiode for I-V measurements

RD50-ENGRUN1

Aims

- Improve the current time resolution of HV-CMOS sensors (by a factor 10)
- Implement different sensor cross-sections
- Study options to increase the device area beyond the reticle size limitation
- Measure the sensors performance after a wide range of fluences

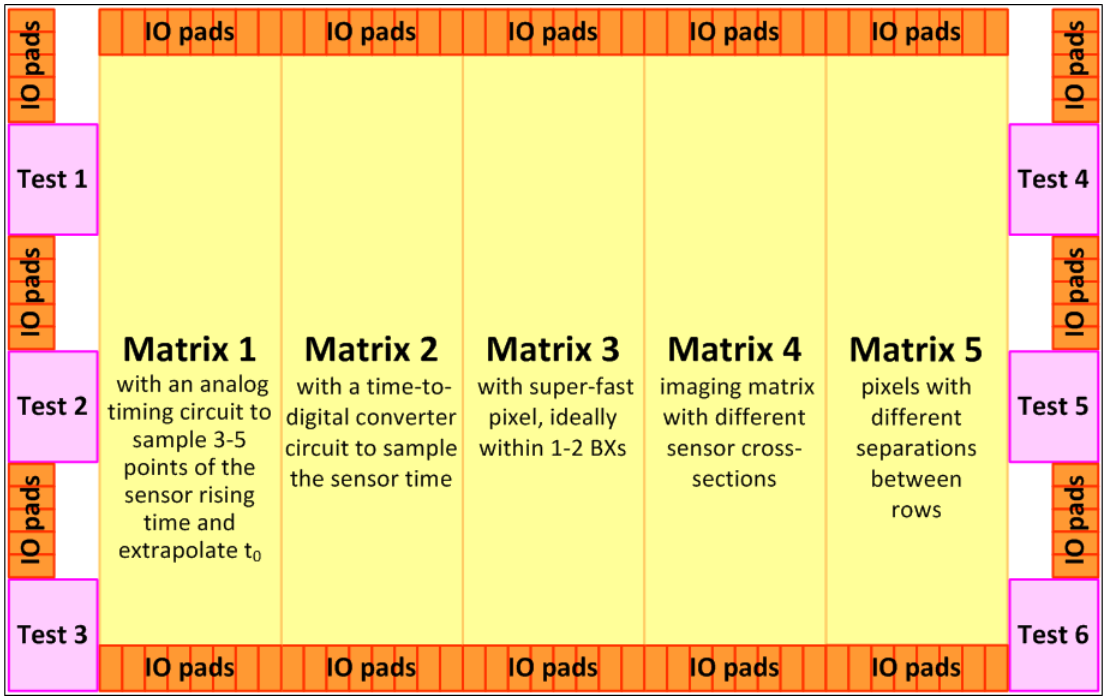
Technology

- 150 nm HV-CMOS from LFoundry
- Large area submission (2 cm x 2 cm, engineering run)

Design effort

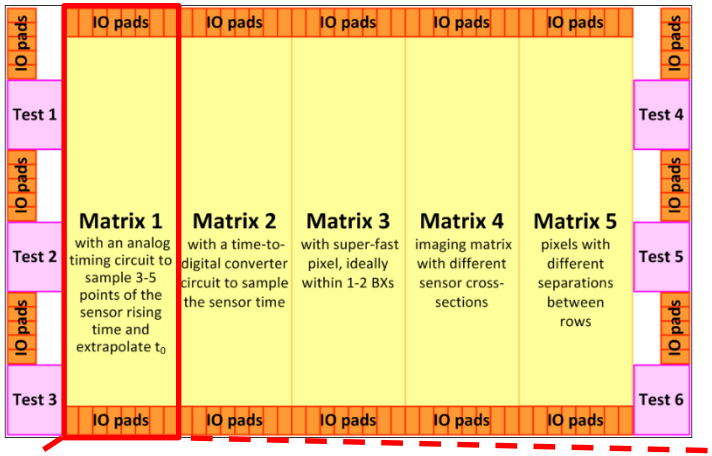
- FBK (N. Massari, M. Perenzoni and C. Zhang)
- IFAE (R. Casanova)
- Uni. Barcelona (O. Alonso, +1)
- Uni. Liverpool (S. Powell, E. Vilella and C. Zhang)
- Uni. Seville (F. Muñoz and R. Palomo)

TCAD simulations + DAQ development



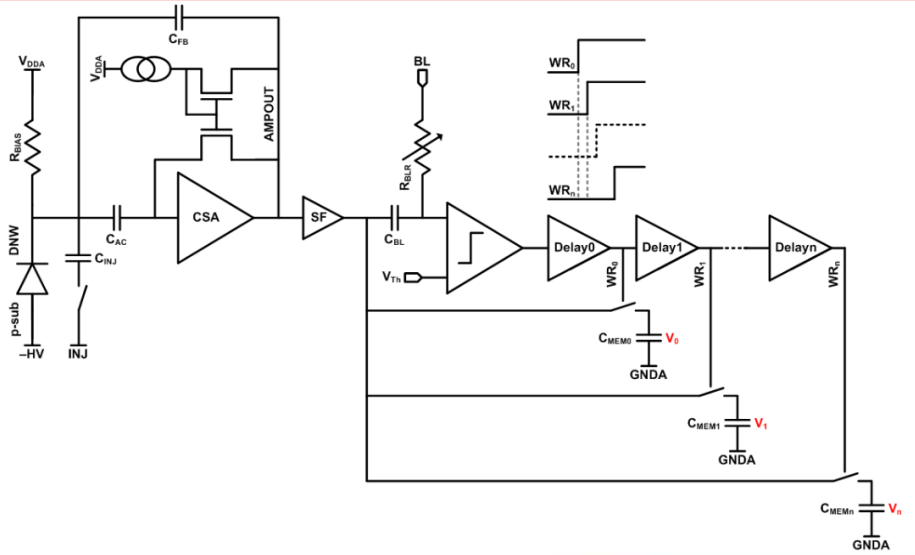
Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive RO
Test structure 3	10 x 10 matrix of very small pixels with 3T-like RO
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	…

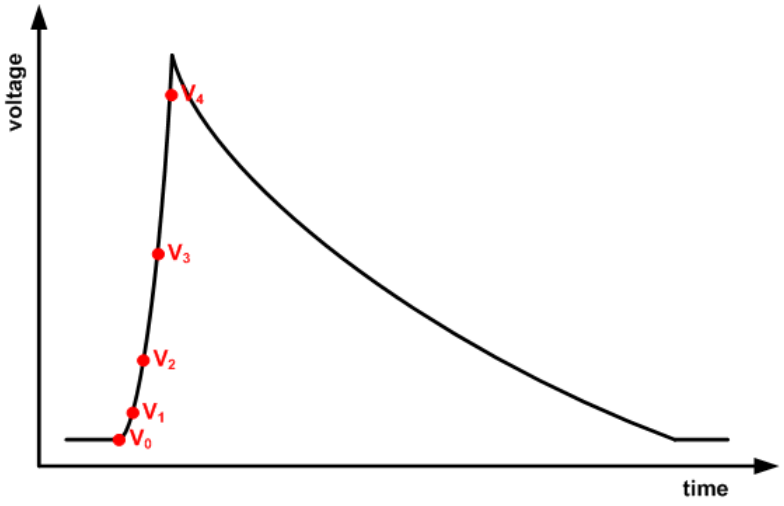
RD50-ENGRUN1 – Matrix 1



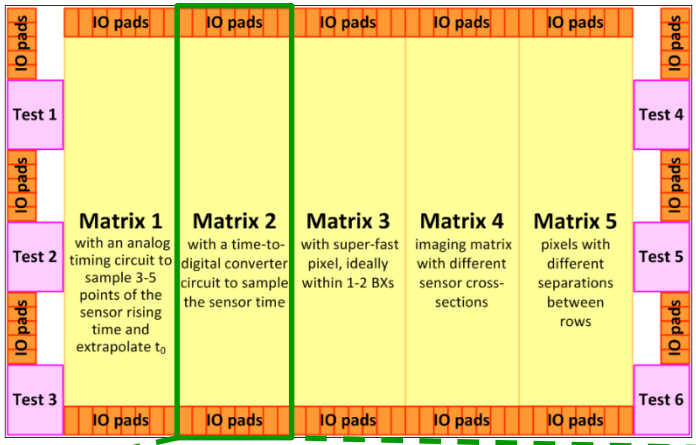
Matrix with analog sampling circuit

- It includes 'n' sample & hold circuits that sample the output voltage of the shaper and store the analog voltages.
- The 'n' hold signals (WR_0, WR_1, …, WR_n) are generated with a chain of delay elements.
- The delay between the 'n' hold signals can be tuned externally (i.e., 1.04 ns@1 V, 1.94 ns@ 1.1V).
- The sample & hold circuits enter the hold mode when there is an event in the pixel.
- The 'n' analog voltages are stored in 'n' analog memories based on MIM capacitances.



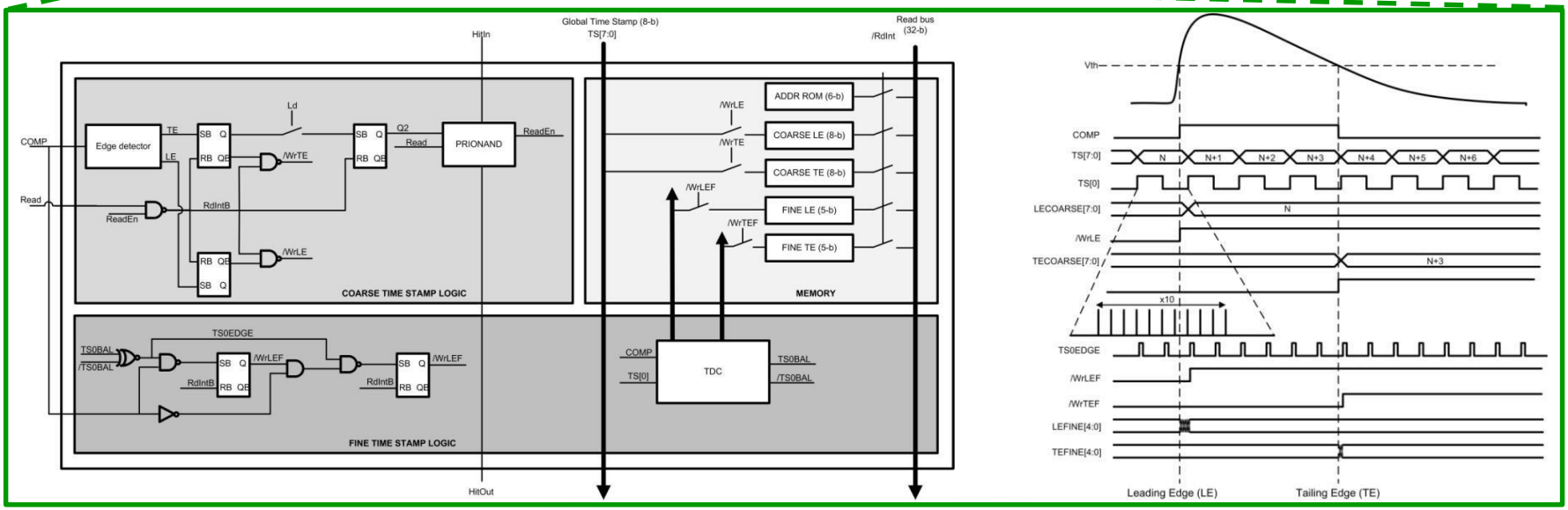


RD50-ENGRUN1 – Matrix 2

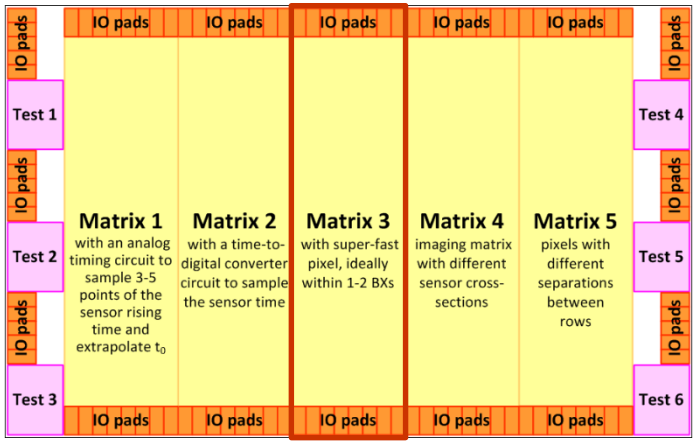


Matrix with Time-to-Digital Converter (TDC)

- Leading Edge and Trailing Edge time stamp capture
- TS measured with 2.5 ns accuracy:
  - Coarse time measurement (25 ns accuracy) → global time stamp
  - Fine time measurement (2.5 ns accuracy) → TDC



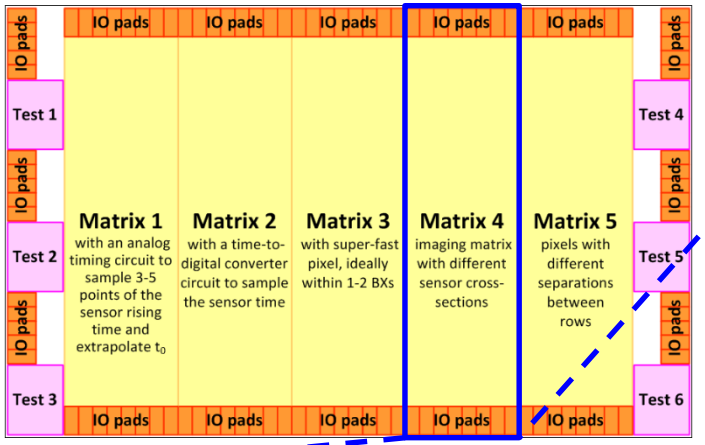
RD50-ENGRUN1 – Matrix 3



Matrix with fast pixels

- See presentation “Design of High-speed Front-ends for HV-MAPS” by Chenfan Zhang.

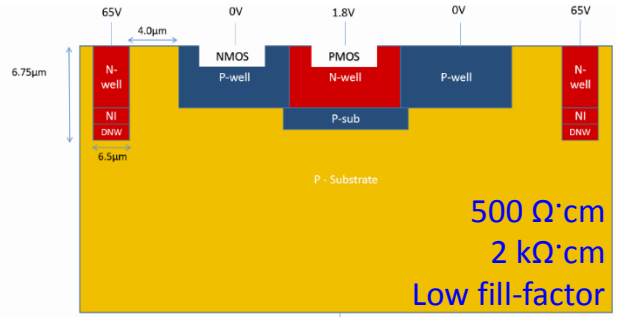
RD50-ENGRUN1 – Matrix 4

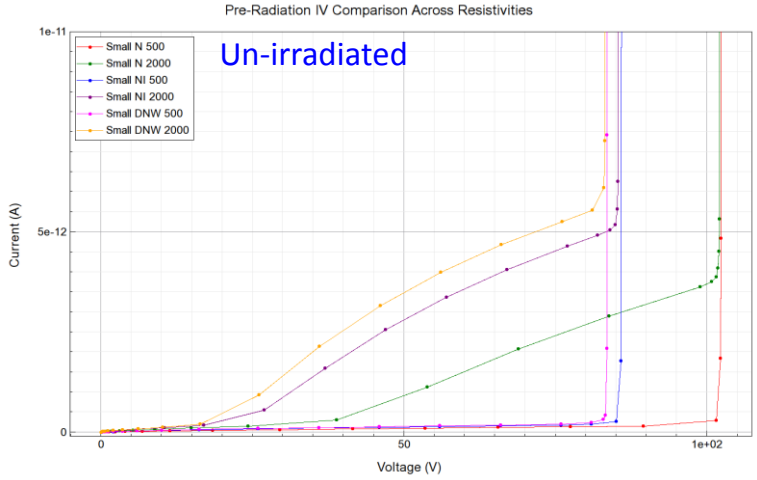


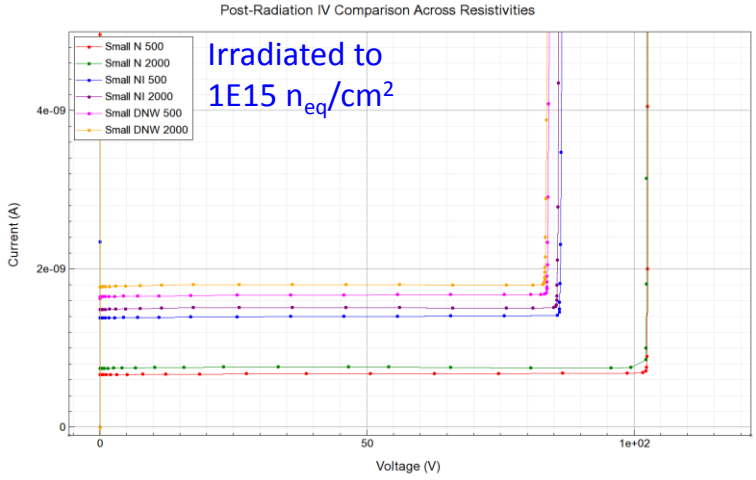
Matrix with different sensor cross-sections

- Study and compare pixels with different cross-sections fabricated on the same HV chip (i.e., low fill-factor vs. high fill-factor).
- TCAD simulations to study sensor performance before fabrication (plots by B. Doyle, R. Leigh and L. Gonella at Uni. Birmingham).

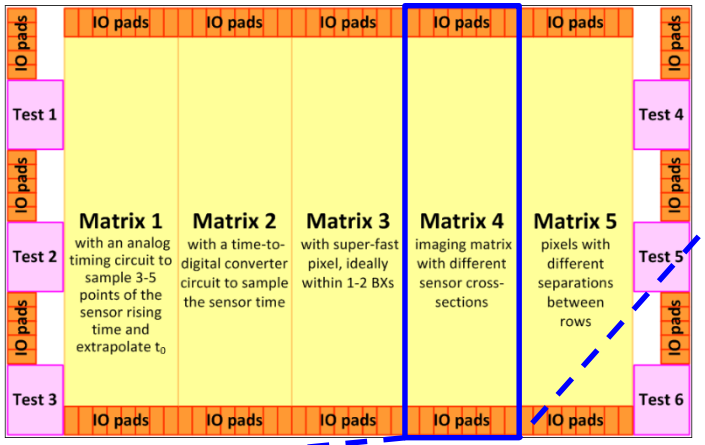
Preliminary







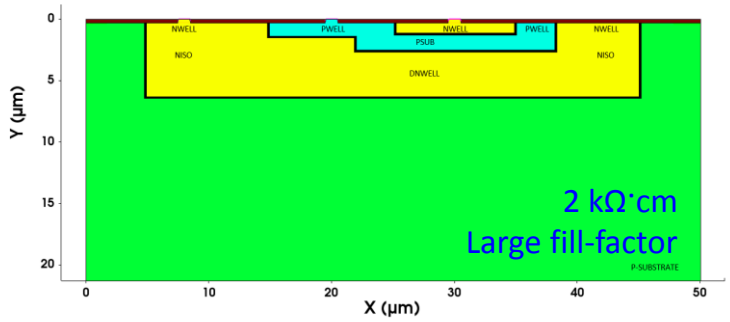
RD50-ENGRUN1 – Matrix 4

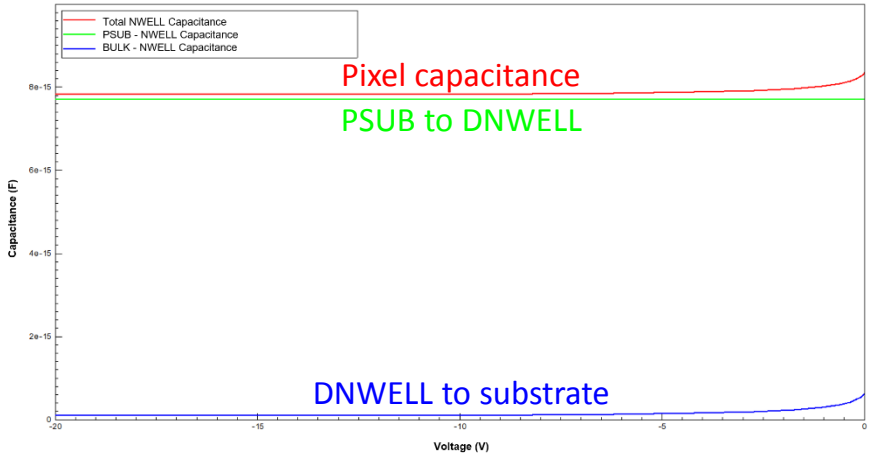


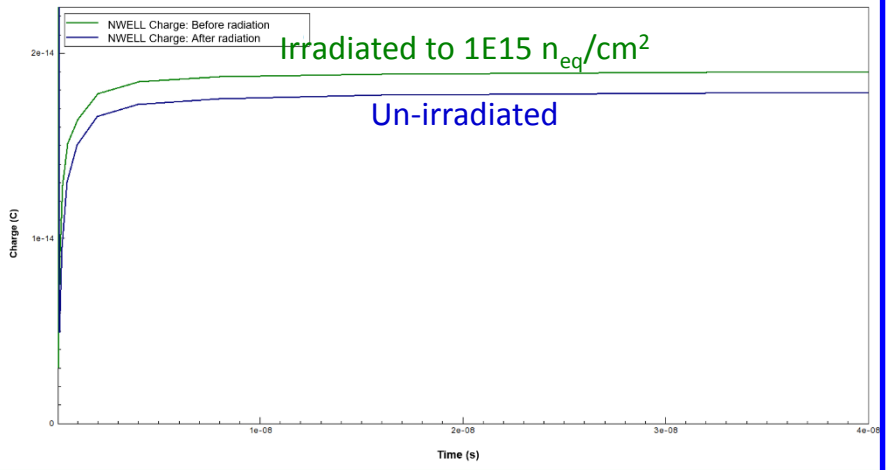
Matrix with different sensor cross-sections

- Study and compare pixels with different cross-sections fabricated on the same HV chip (i.e., low fill-factor vs. high fill-factor).
- TCAD simulations to study sensor performance before fabrication (plots by B. Doyle, R. Leigh and L. Gonella at Uni. Birmingham).

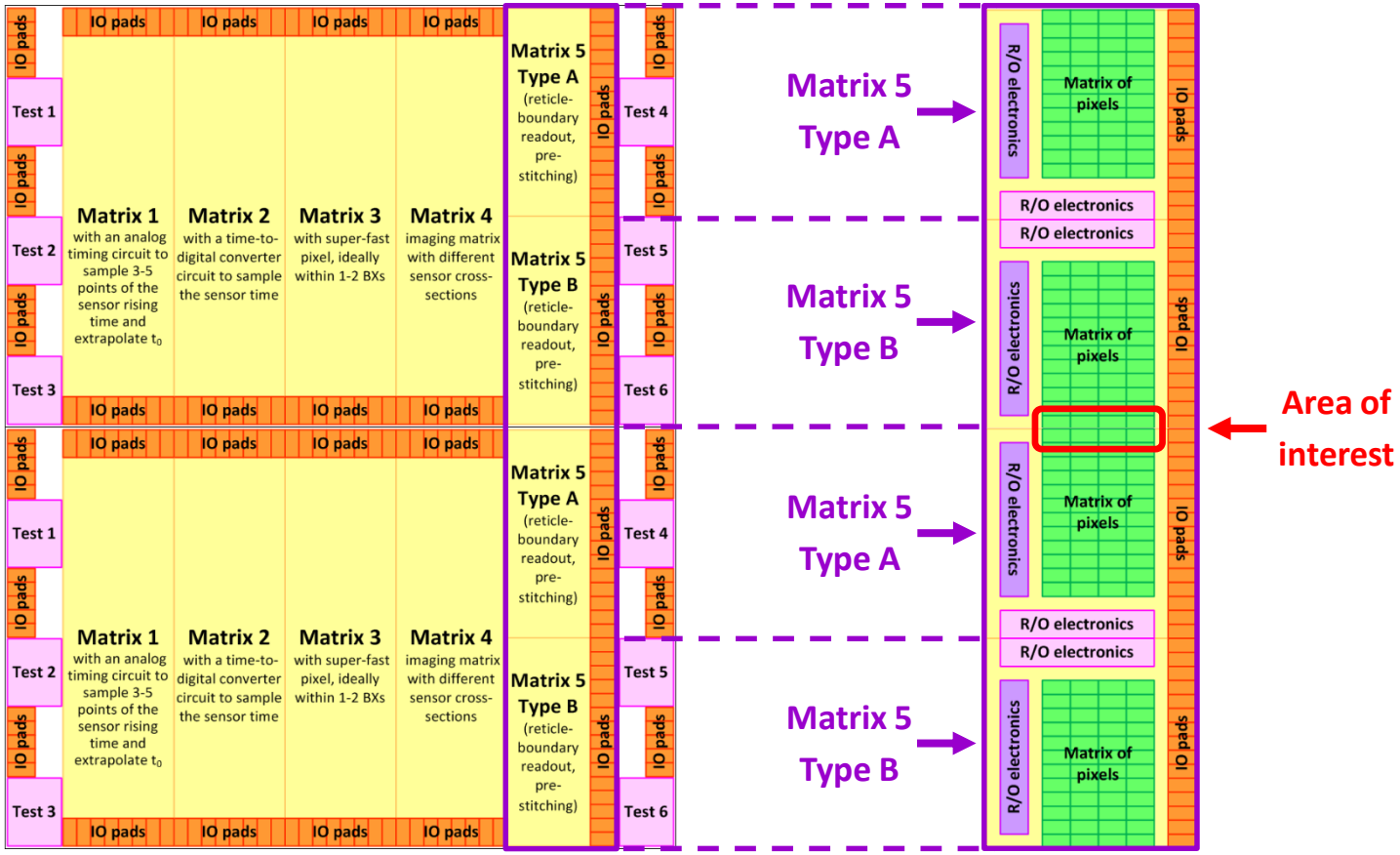
Preliminary







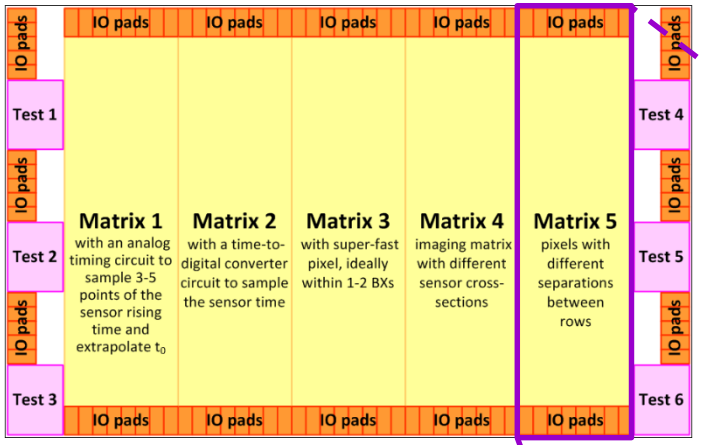
RD50-ENGRUN1 – Matrix 5 original idea



Motivation

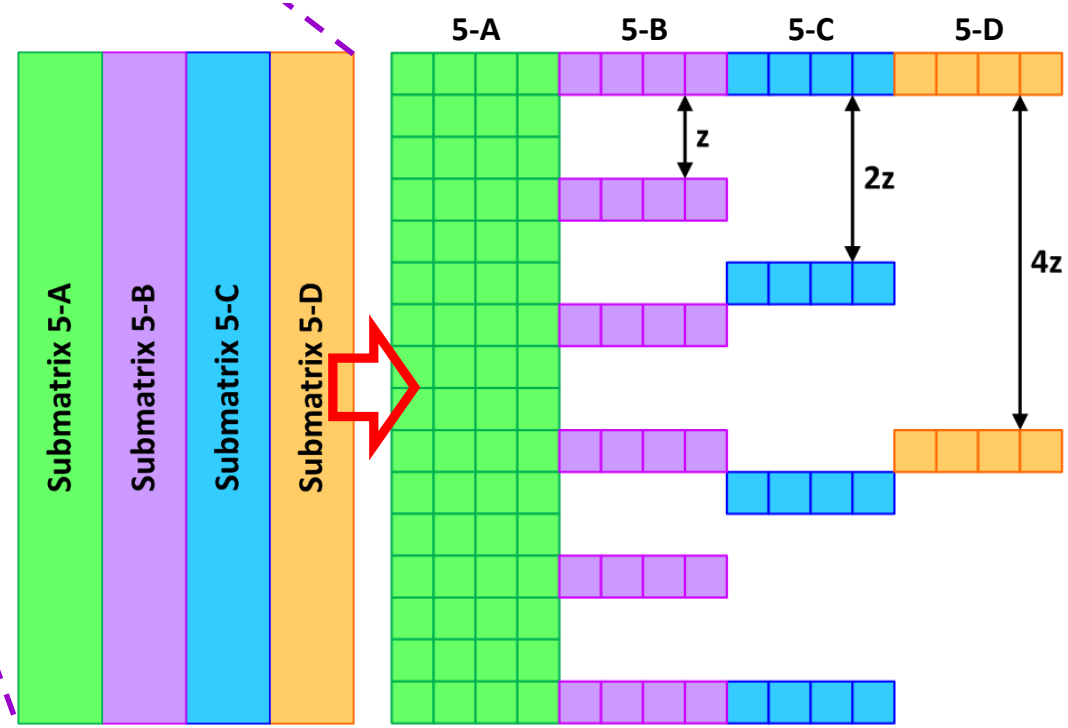
- Increase the device area beyond the reticle size limitation
- We want to know if it is possible to merge the depletion regions of pixels from 2 different samples

RD50-ENGRUN1 – Matrix 5 new approach



Matrix with different separations between rows

- Study the effects of dead areas between pixels on the charge collection efficiency of the sensor
- This matrix includes a few sub-matrices with different separations between rows of pixels
- The separations range between a few µm to some hundreds of µm
- Doing TCAD simulations at the moment



Conclusion

- Generic R&D work to push forward some of the features of HV-CMOS sensors is being done within the RD50 collaboration.
- An MPW in the 150 nm HV-CMOS technology from LFoundry S.r.l. (RD50-MPW1) has been designed and fabricated to test the design aspects of the technology and also implement novel concepts.
  - This chip integrates 2 fully monolithic matrices of HV-MAPS pixels + test structures.
  - A DAQ is being developed and measurements will start soon.
- The knowledge gained with RD50-MPW1 is being used to design a large area demonstrator (RD50-ENGRUN1) in the same technology.
  - TCAD simulations are being performed.
  - A DAQ is being developed.
- RD50-ENGRUN1 integrates novel detector concepts to improve the time resolution and speed of the detector, amongst other features.
- The prototypes will be extensively measured.

Many thanks for your attention!