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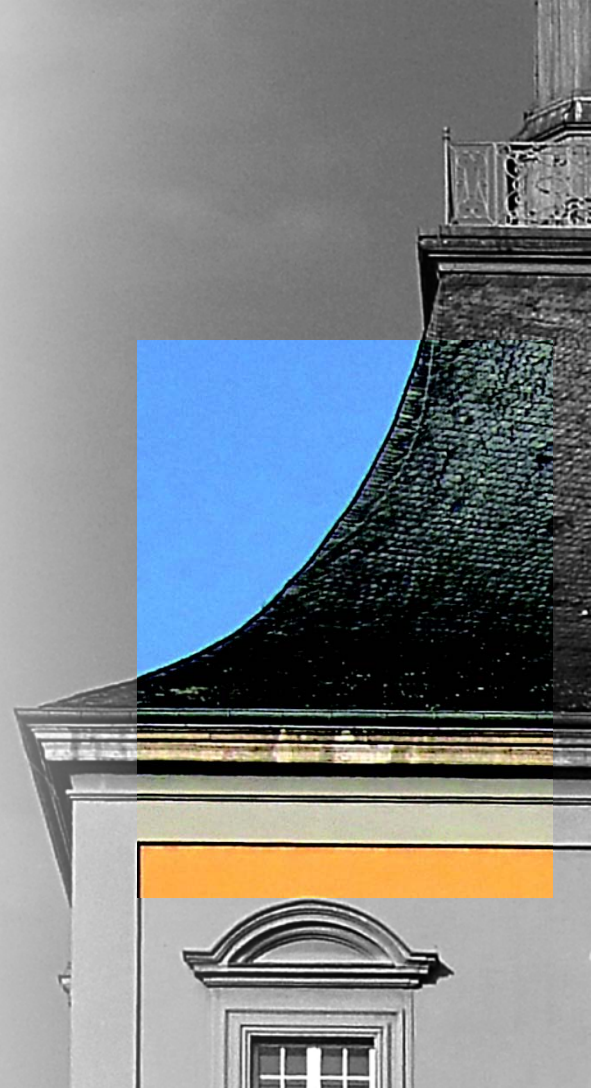
SI LAB Silizium Labor Bonn

CMOS PIXEL SENSORS/DETECTORS OVERVIEW

NORBERT WERMES (UNIVERSITY OF BONN)

RD50 Meeting, Hamburg, 5.6.2018



INTRODUCTION DMAPS

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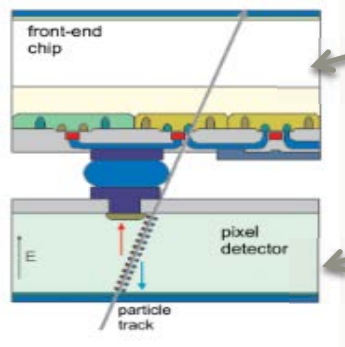
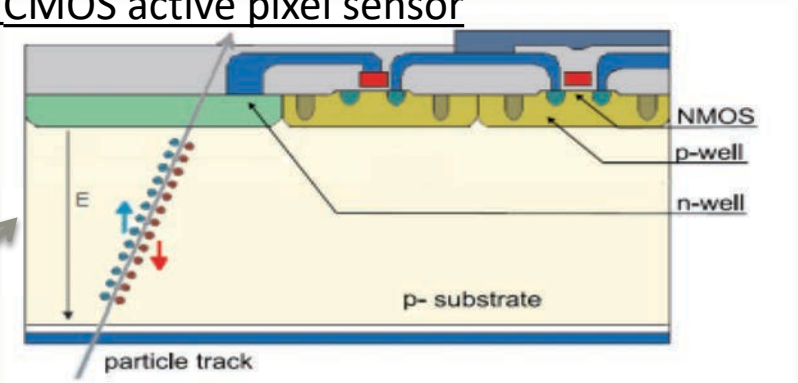
Hybrid detector



Depleted CMOS active pixel sensor



No need for fine pitch bump bonding between sensor and readout circuitry.

→ **Easier to produce**

→ Large cost reduction (sensor + R/O chip + BB → 1 x chip)

→ Plus all advantages that large CMOS Fabs may offer, including fast turn around

CMOS PIXEL DETECTORS

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Hybrid pixel detectors (L0 – L3)

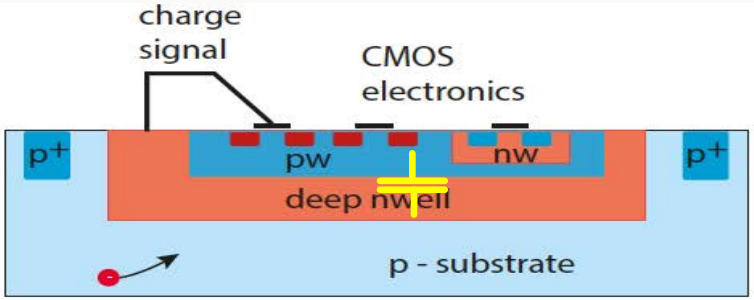
	STAR	ALICE-LHC	ILC	ATLAS-HL-LHC	
				Outer	Inner
Time resolution [ns]	110	20 000	350	25	25
Particle Rate [kHz / mm^2]	4	10	250	1000	10 000
Fluence [n_{eq} / cm^2]	> 10^{12}	> 10^{13}	10^{12}	10^{15}	2 x 10^{16}
Ion. Dose [MRad]	0.2	0.7	0.4	50	> 1000

MAPS (ALPIDE)

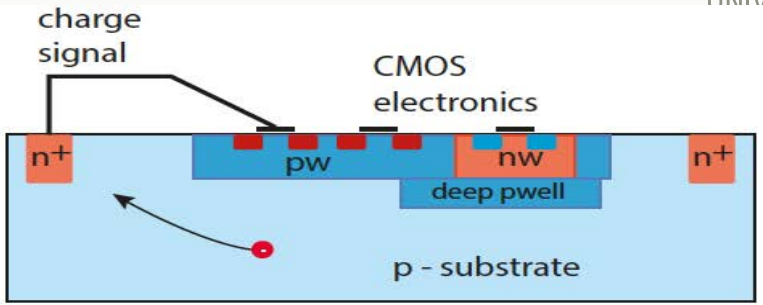
Radiation-hard DMAPS or hybrid (L4)

need: radhard (TID & NIEL) + fast response time + fast readout => Q coll. by drift & full R/O architecture

LARGE VERSUS SMALL COLLECTION ELECTRODE (FILL FACTOR)



(a) Large fill-factor



(b) Small fill-factor

Electronics **inside** charge collection well

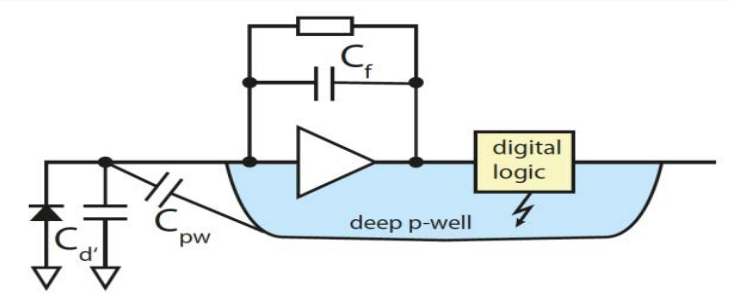
- **large fill factor**
  → no low field regions
  → on average **short(er) drift** distances
  → less trapping -> **radiation hard**
- **Larger (100 fF)** sensor **capacitance**
- **additional well-well capacitance** (~100 fF)
  → noise & speed/power penalties
  → x-talk easier (from digital to sensor)

Electronics **outside** charge collection well

- **small fill factor**
  -> very small sensor capacitance (<5 fF)
  → noise low, speed high, power low
- on average longer drift distances and low field regions
  → radhard hardness more difficult ?

CONSEQUENCES OF THE ADDITIONAL INTER-WELL CAPACITANCE

- larger total detector capacitance: $\mathbf{C_d} = C_{d'} + C_{pw}$

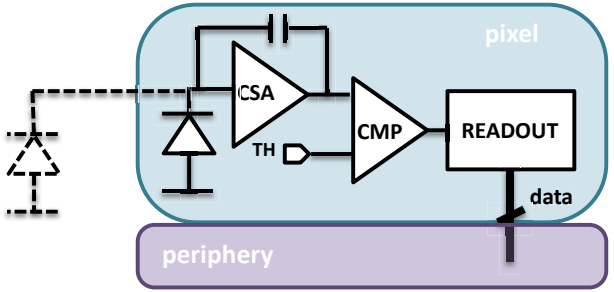


- noise $ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$
- timing $\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$

need to increase g_m to compensate
=> increased power ($g_m \propto I_d$)

- cross talk into sensor
  The PW/DNW capacitance C_{pw} couples into the sensor (the CSA input node).
  Needs special attention e.g. current steered logic.

READOUT VARIANTS



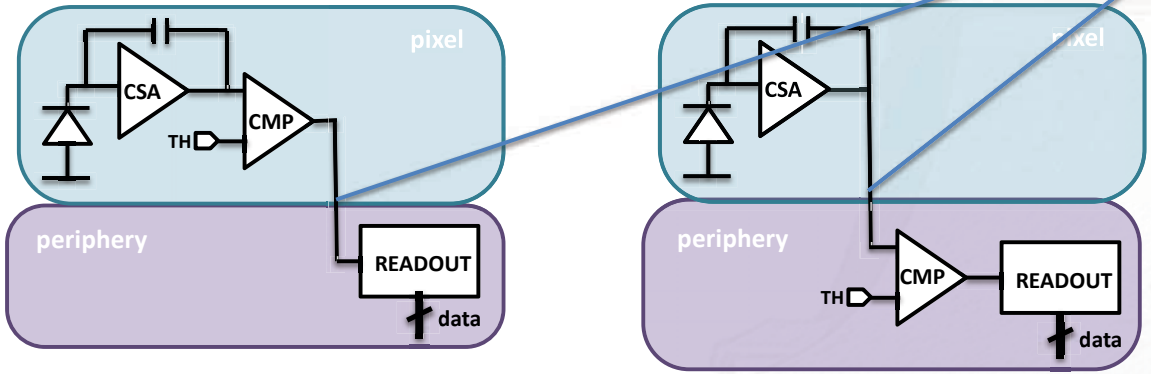
R/O address and time stamp in pixel

Move data to periphery

Example: column drain architecture

Move data from every pixel immidiately to periphery (example: PPtB architecture)

You can also hybridize here



Optimize for highest integration level, lowest cross coupling, and speed.

WHAT IS NEEDED TO REALIZE (RADHARD) DEPLETED CMOS PIXELS?

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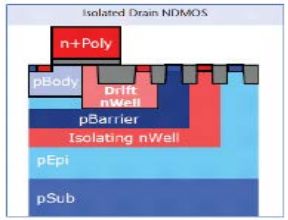
$$d \sim \sqrt{\rho \cdot V}$$

1 **"High" Voltage add-ons to apply 50 – 200 V bias**

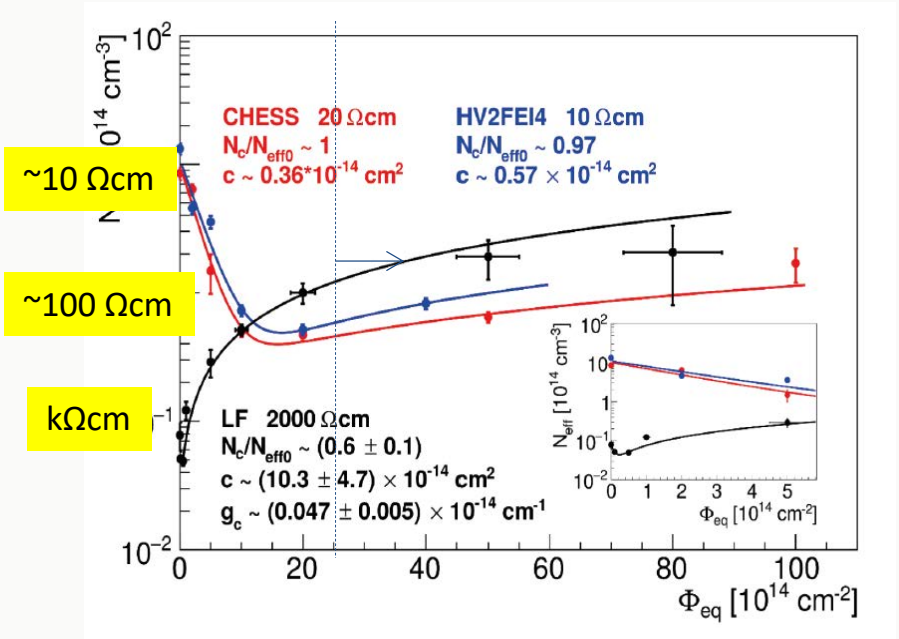
2 **"High" Resistivity Substrate Wafers (100 Ωcm – kΩ cm)**



from: www.xfab.com

3 **Multiple (3-4) nested wells (for shielding and full CMOS)**

4 **Backside Processing (for thinning and back bias contact)**



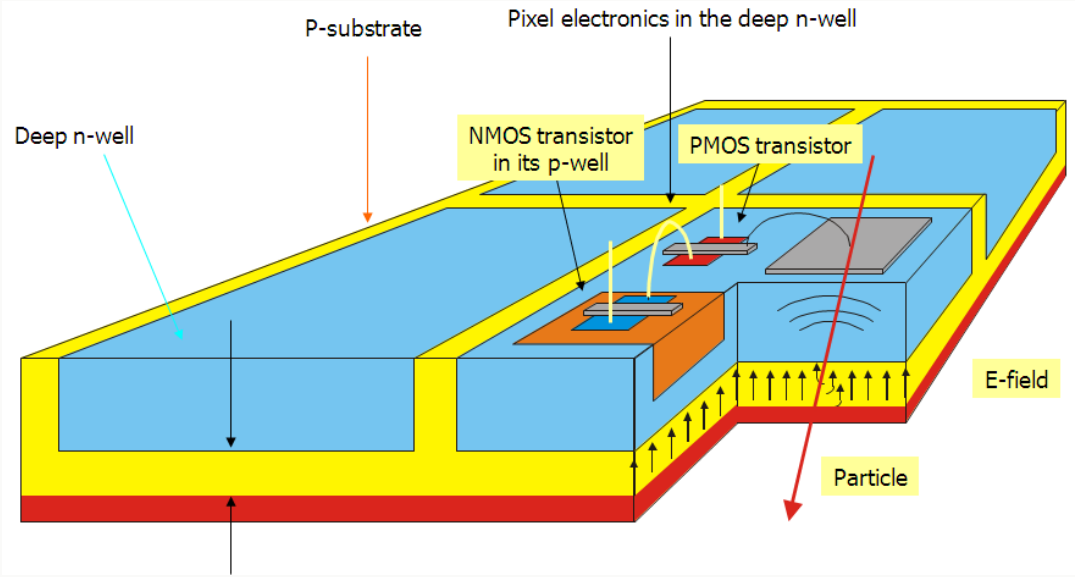
I. Mandic et al., JINST 12 (2017) no.02, P02021

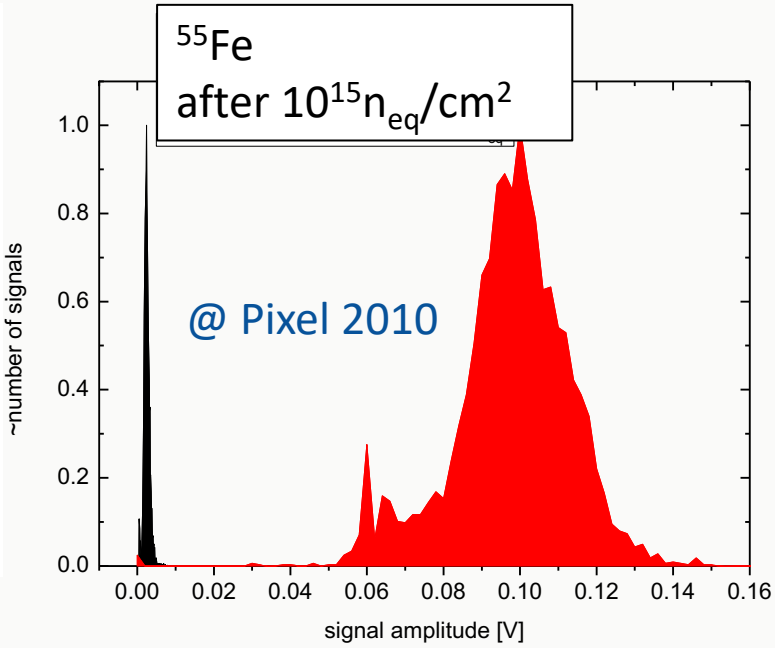
DMAPS IDEA (CALLED “HVCMOS”)

I. Peric, NIM A582 (2007) 876-885

HV add-on (AMS)

Medium resistivity





FOUNDRIES

feature sizes ≥ 130 nm

ATLAS CMOS PIXEL COLLABORATION

> 20 groups

DEVELOPMENT LINES LARGE ELECTRODE

This talk (with bias)

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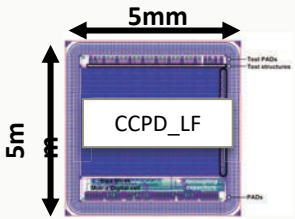
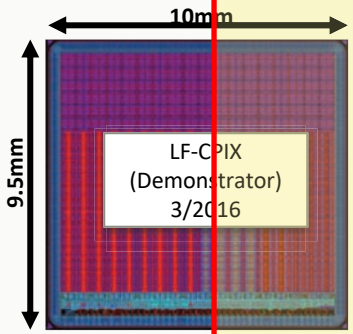
LFoundry

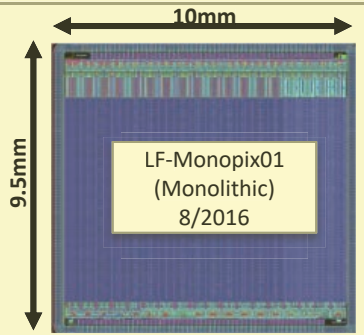


small **prototypes**



full size **demonstrator** bondable to FE-I4

big step

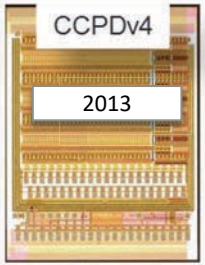


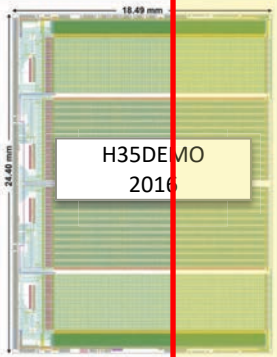
fully monolithic version with R/O architecture

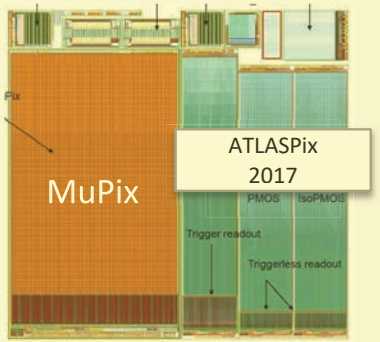
Full RD53B

compatible system chip

AMS







LARGE (~1 CM^2) FULL CMOS CHIPS (=MODULES) W/ READOUT

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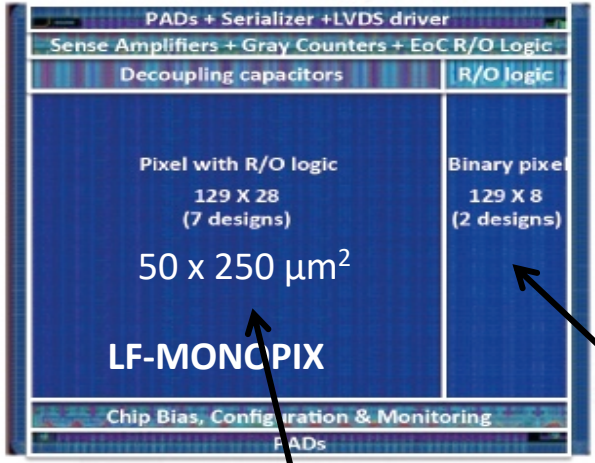
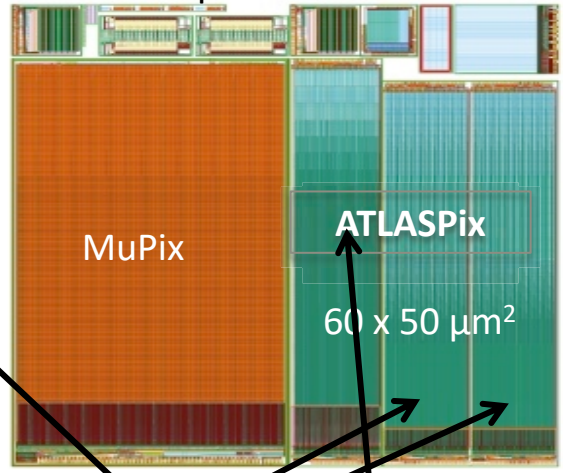
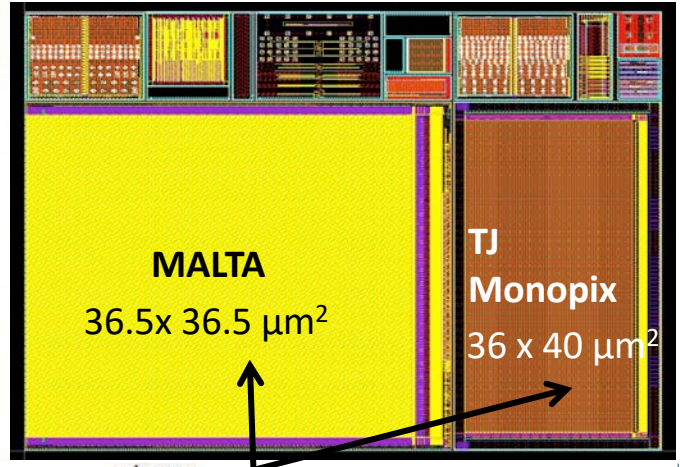
LFoundry 150 nm
substrate ρ > 2 kΩcm

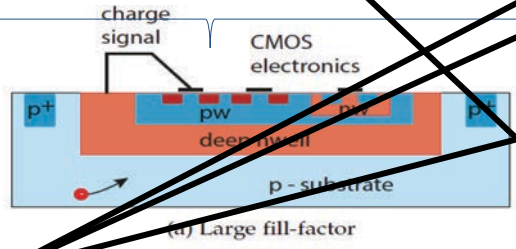
ams 180 nm
substrate ρ ~ 0.08 - 1 kΩcm

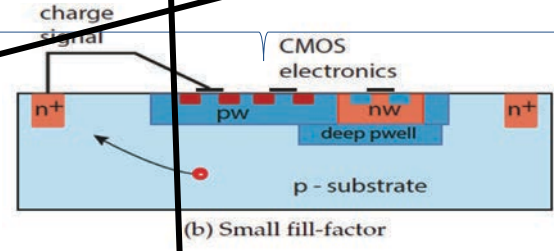
TowerJazz 180 nm epitaxial (25 µm)
substrate ρ > kΩ cm





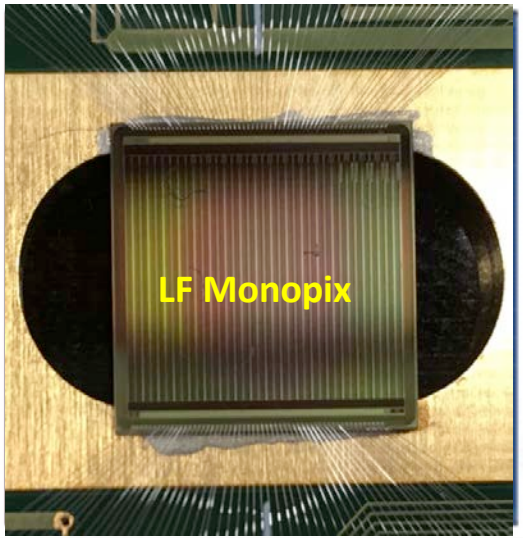




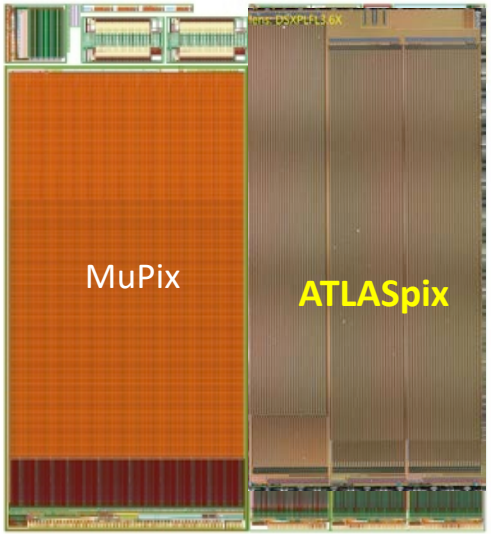


column drain (conservative) - parallel pixel to buffer - asynchronous

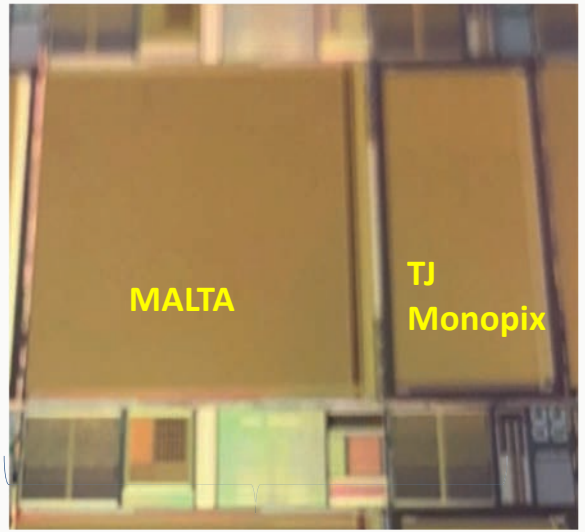
LARGE (~1 CM^2) FULL CMOS CHIPS (=MODULES) W/ READOUT



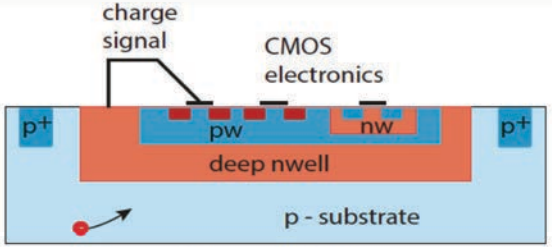
LFoundry 150 nm
substrate ρ > 2 kΩcm



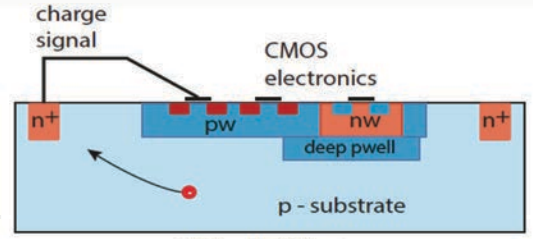
ams 180 nm
substrate ρ ~ 0.08 - 1 kΩcm



TowerJazz 180 nm epitaxial (25 µm)
substrate ρ > kΩ cm

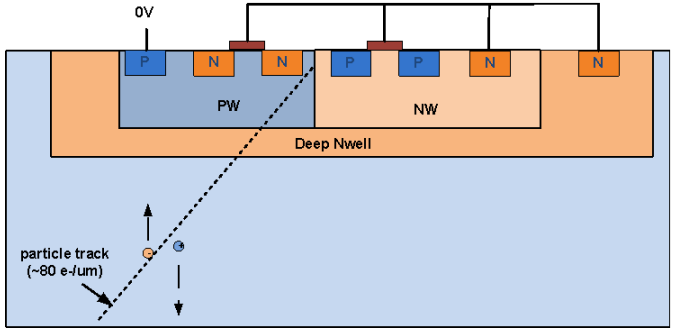


(a) Large fill-factor



(b) Small fill-factor

AMS 350 NM -> 180 NM LARGE ELECTRODE



- Substrate: **10 (initially) – 2k Ohm-cm**
- Bias: >60 – 100 V
- 180nm/350nm
- 3-6 metal layers
- **No PMOS isolation**

I. Peric et al.
Nucl.Instrum.Meth. A582 (2007) 876-885
Nucl.Instrum.Meth. A765 (2014) 172-176

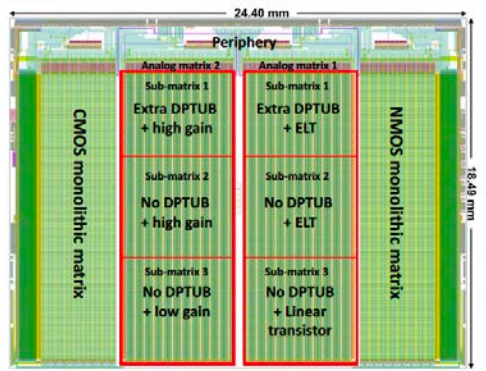
Designs: KIT, Liverpool, Geneva, Heidelberg, IFAE

Collaboration: KIT, Geneva, ANL, Hefei, Liverpool, Bern, BNL, IFAE, Lancaster, CERN, Illinois, Oklahoma, Tsukuba

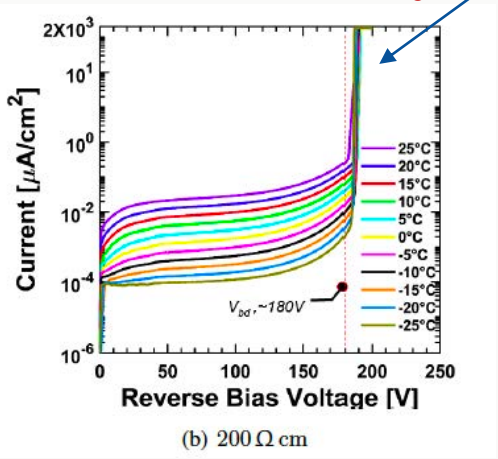
AMS 350 DEMONSTRATOR (H35DEMO)

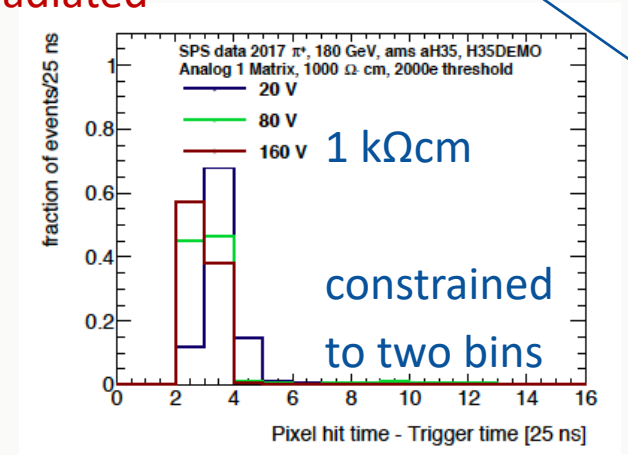
4 resistivities : 20 Ωcm (standard), 80 Ωcm, 200 Ωcm, 1 kΩcm

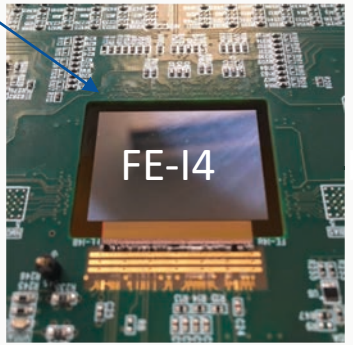
- Standalone matric w/ in-pixel nMOS discriminator
- Analog matrix for coupling to FE-I4
- Standalone matrix w/ off-pixel CMOS discriminator
- Demonstrated Bias up to 180V

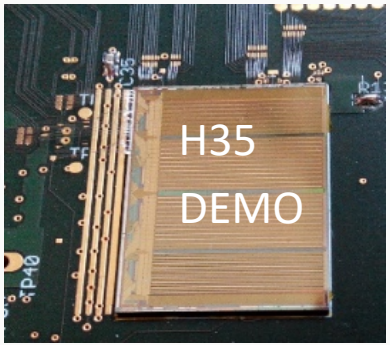


unirradiated









M. Benoit et al. : arXiv 1712.08338v1

AMS 350NM - H35DEMO

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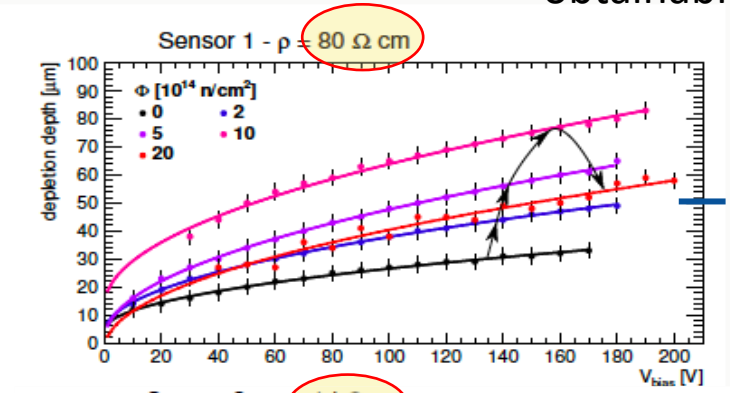
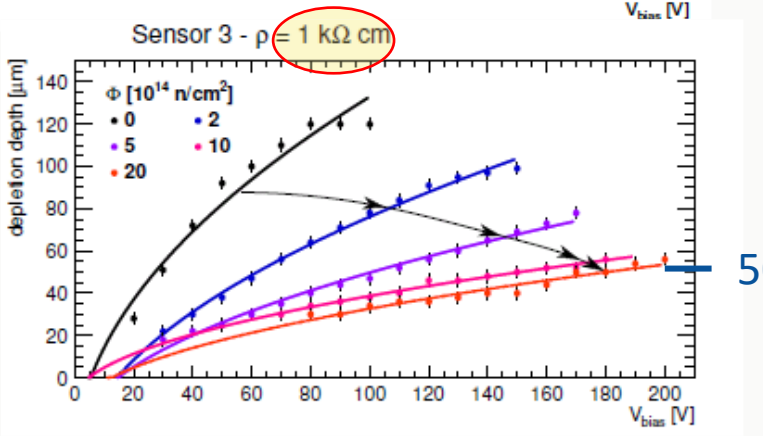
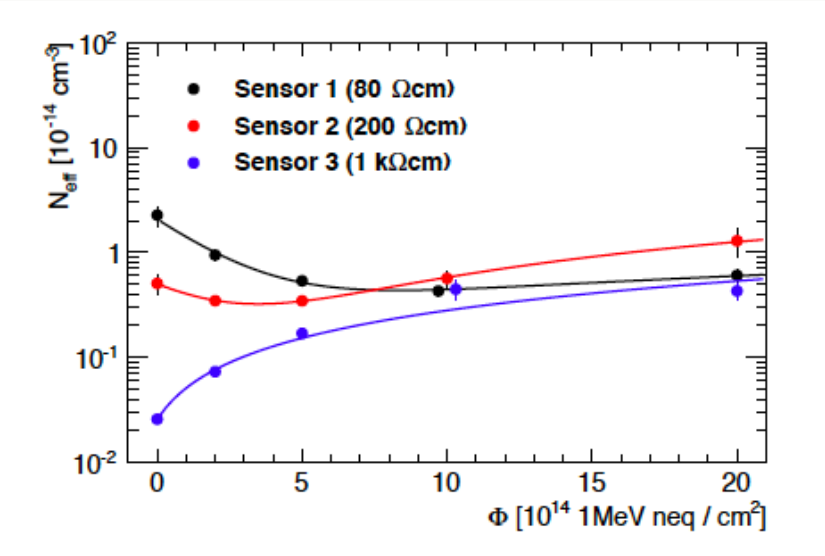
obtainable depletion depth



50 µm



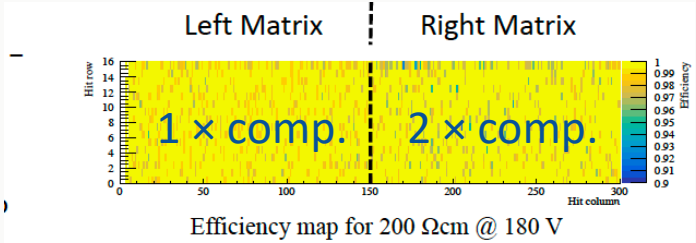
50 µm

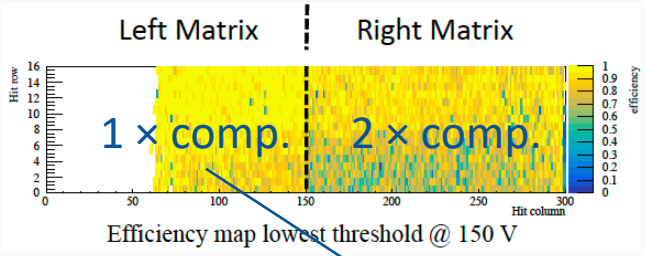


E.Cavallaro et al., JINST 12 (2017) no.01, C01074

AMS 350NM - H35DEMO

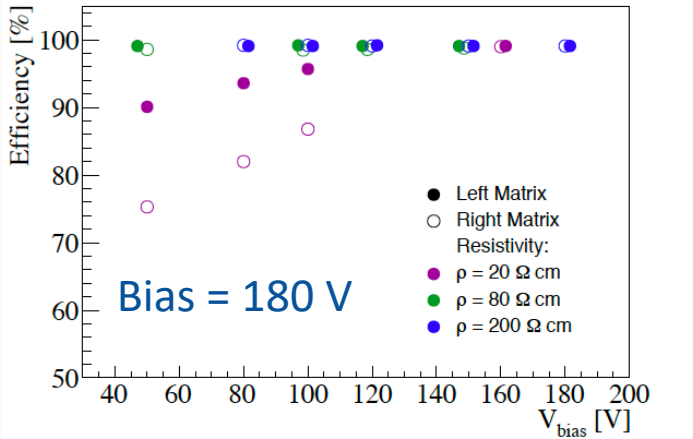
off-pixel comparator





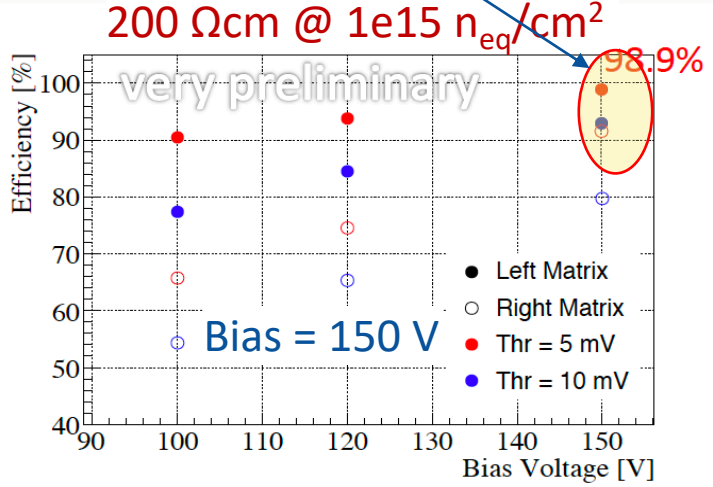
50 × 250 µm² pixels

unirradiated

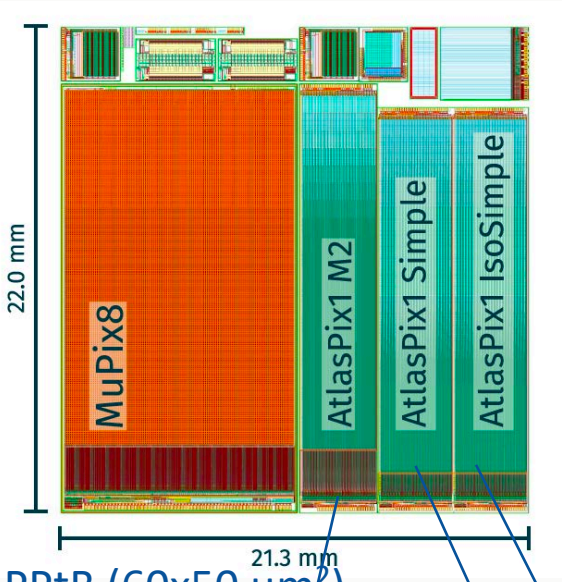


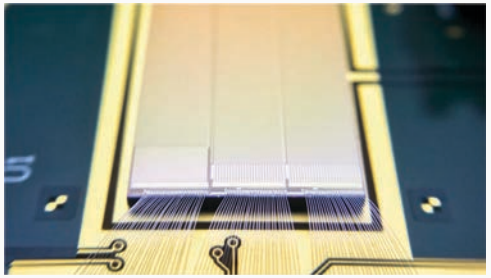
200 Ωcm @ 1e15 n_{eq}/cm^2

98.9%



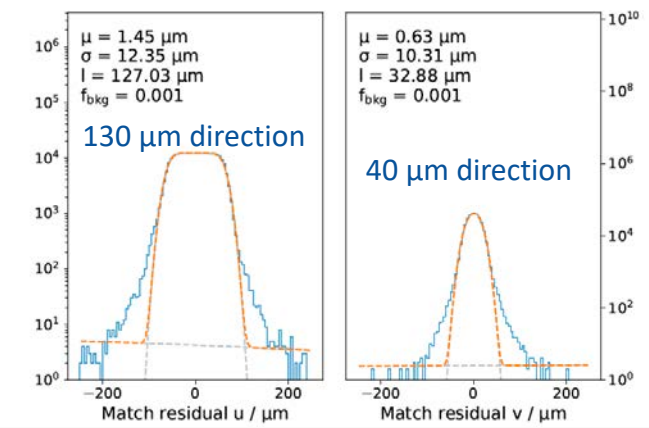
ATLASPIX1 (180 NM)





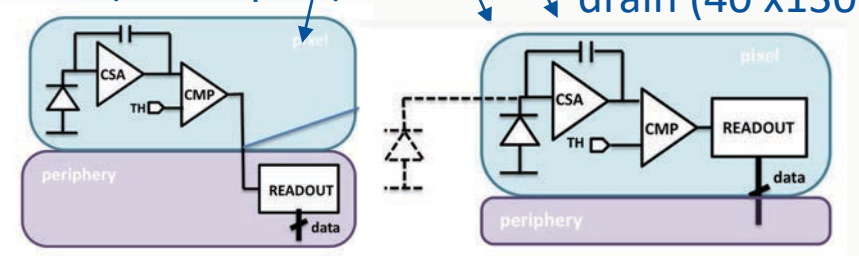
unirradiated

Resistivity 80 Ωcm & 200 Ωcm



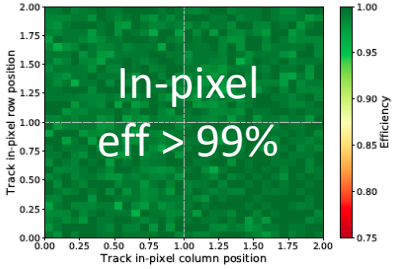
PPtB (60x50 μm²)

Column drain (40 x130 μm²)

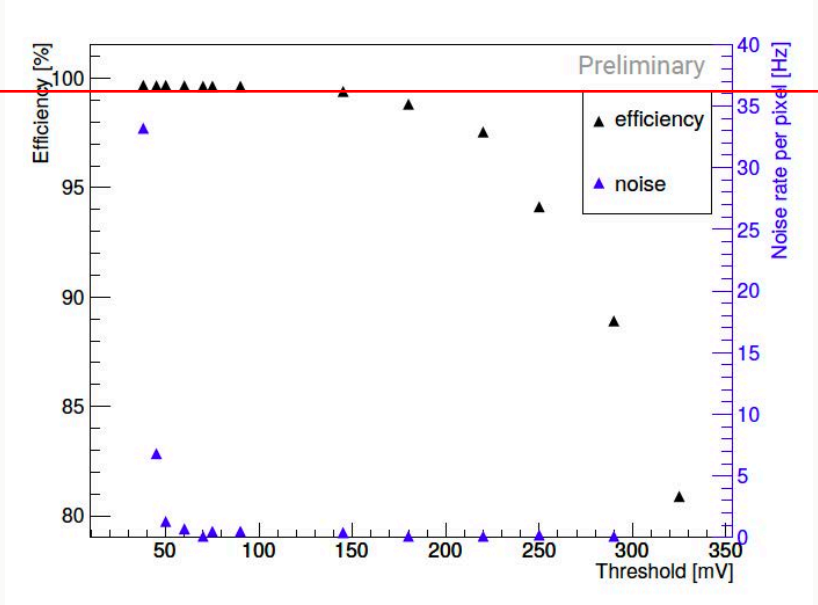


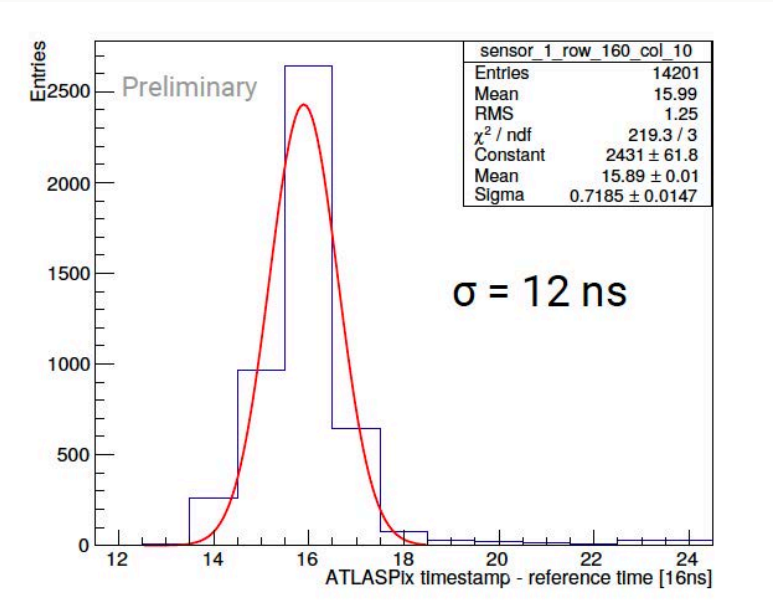
M. Kiehn
ATLAS UW 4/18

65V HV bias
Threshold 840 mV



unirradiated



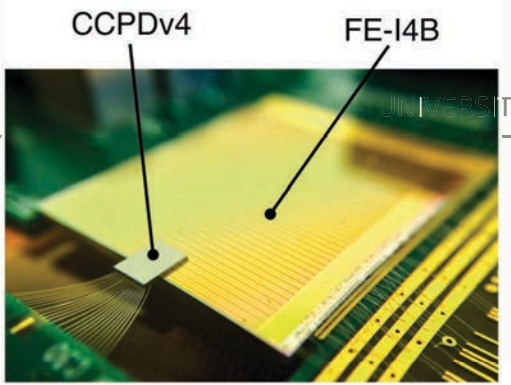


Overall efficiency ✓

Timing …

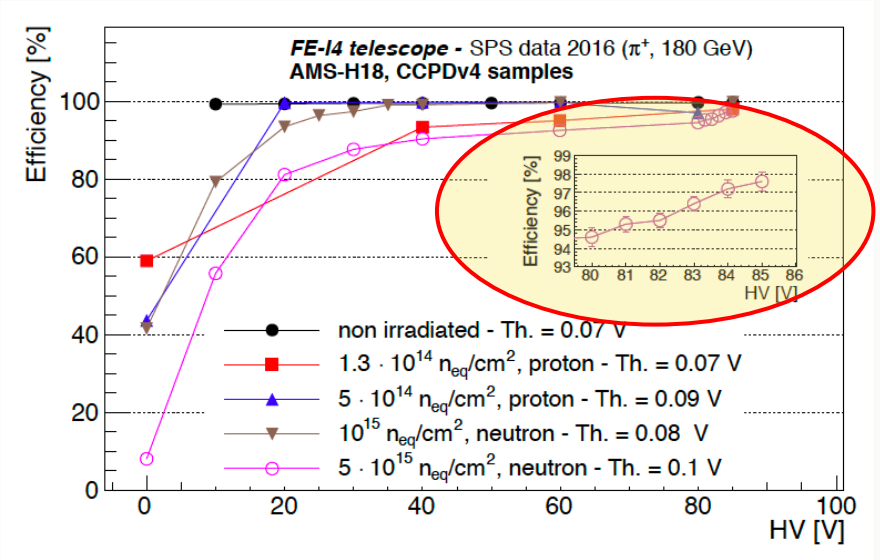
ATLAS specs: noise rate < 10^{-6} ≙ 40 Hz

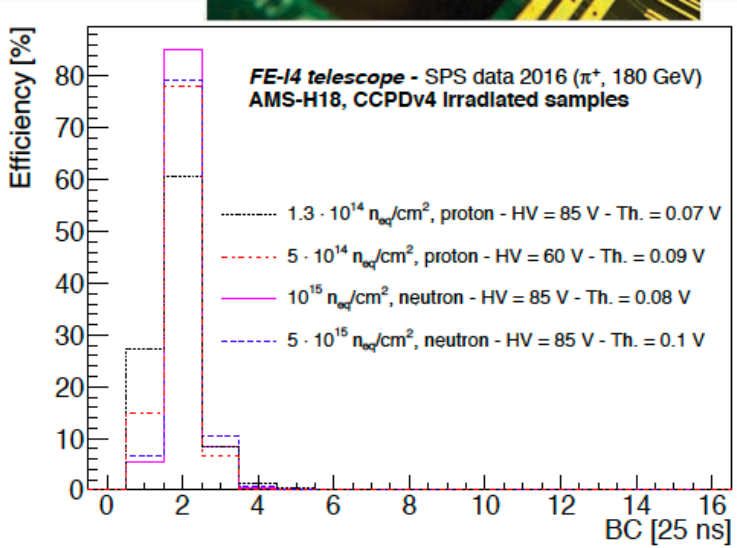
IRRADIATED AMS SAMPLES



Irradiated to > 10^{15} n_{eq}/cm^2

180 nm, but CCPD device w/ FE-I4B

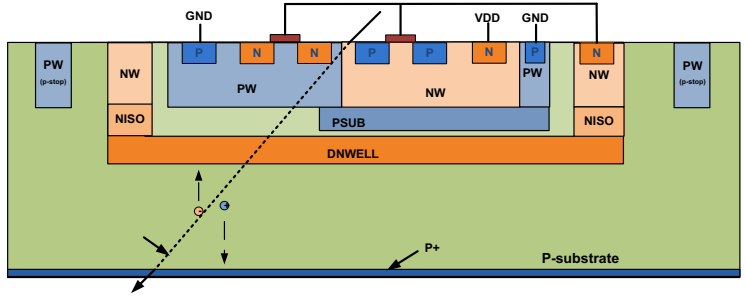




Overall efficiency ✓

Timing …

LFOUNDRY 150 NM LARGE ELECTRODE



LFA150:

- LFoundry **150 nm** process (deep N-well/P-well)
- **Quadrupel** well
- Up to 7 metal layers
- Resistivity of wafer: > 2 kΩ·cm
- Small implant customization possible
- Backside processing
- Voltages up to **280 V**

Designs: Bonn, CPPM, IRFU

Collaboration: Bonn, CPPM, IRFU, CERN, Ljubiljana, Milano, Bologna, Oxford, Glasgow, Birmingham

DEVELOPMENT SERIES

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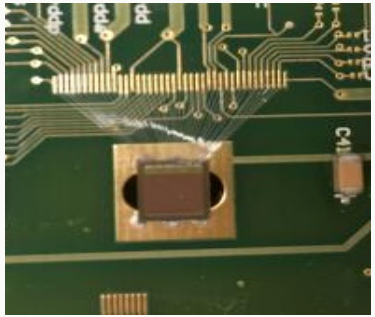
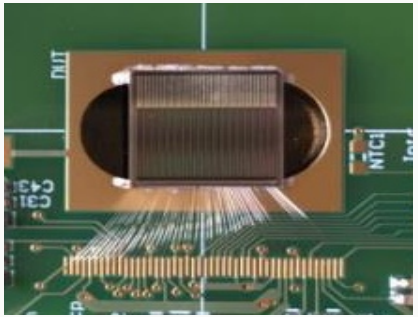
❑ CCPD_LF



Sensor + Analog (Disc.)

- Pixel size: 33 µm x 125 µm
- Chip size: 5 mm x 5 mm
- Fast R/O with FE-I4
- Thickness: 750, 300, 100 µm
- Bonn/CPPM/KIT

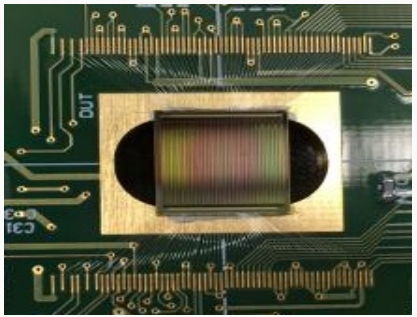
❑ LF-CPIX



Sensor + Analog

- Pixel size: 50 µm x 250 µm
- Chip size: 10 mm x 10 mm
- Fast R/O with FE-I4
- Thickness: 750, 200, 100 µm
- Bonn/CPPM/IRFU

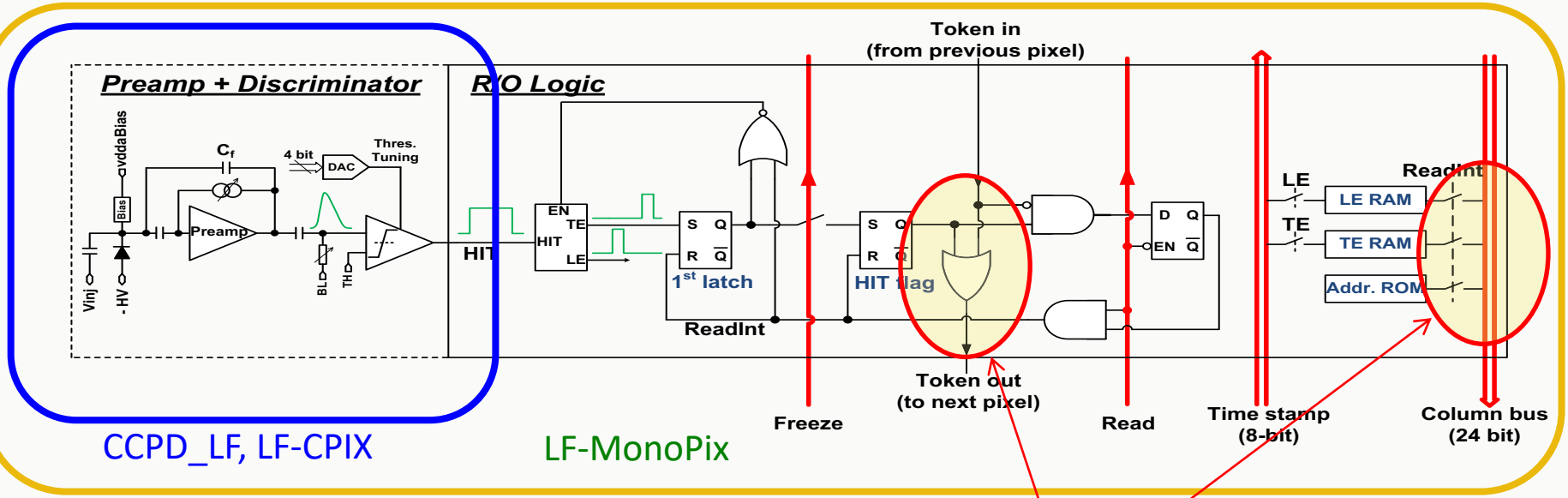
❑ LF-MonoPix (Fully Monolithic)



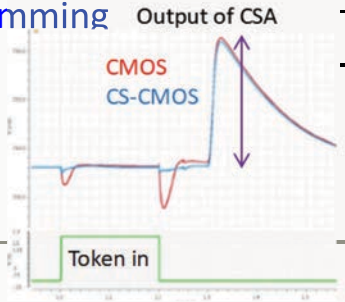
Sensor + Analog + Digital

- Pixel size: 50 µm x 250 µm
- Chip size: 10 mm x 10 mm
- Column drain R/O architecture
- Thickness: 750, 200, 100 µm
- Bonn/CPPM/IRFU

PIXEL DESIGN



- Charge sensitive amplifier
- In-pixel 4-bit DAC for threshold trimming
- Hit register (1-bit counter)
- 8-bit time stamp @ 40 MHz
  - *Time, charge of signal*



- Full-custom dig. circuit
  - *Minimized area => for less C_d*
  - *Low noise circuit design for critical dig. blocks*

eg. current steering logic, Source follower readout of SRAMs

BIAS VOLTAGE (I-V CURVES)

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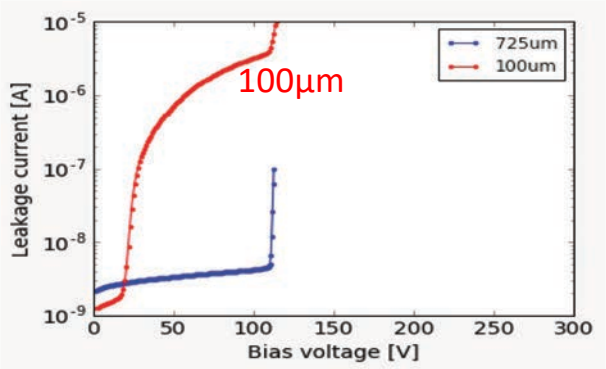
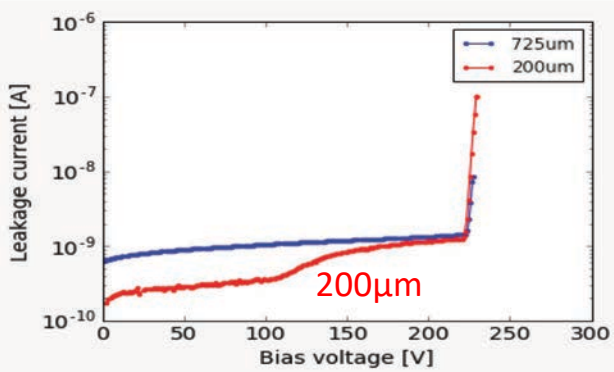
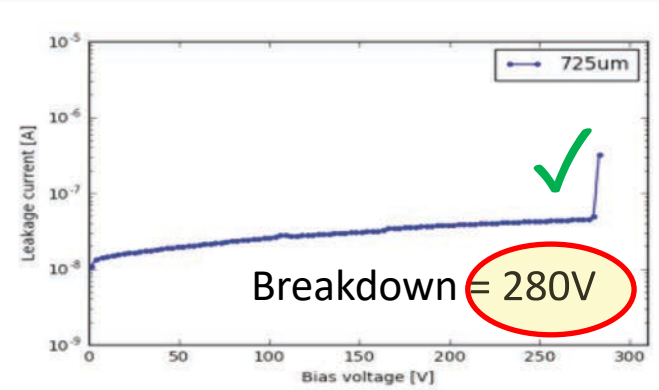
❑ CCPD_LF



❑ LF-CPIX



❑ LF-MonoPix



- Guard rings have been improved to increase the breakdown voltage
- Leakage current performance @ full depletion improved by better backside processing (polishing)
- Full depletion voltage **@ 100 µm, unirr. = 17 V**, irradiated @ 130 V

RADIATION HARDNESS (TID)

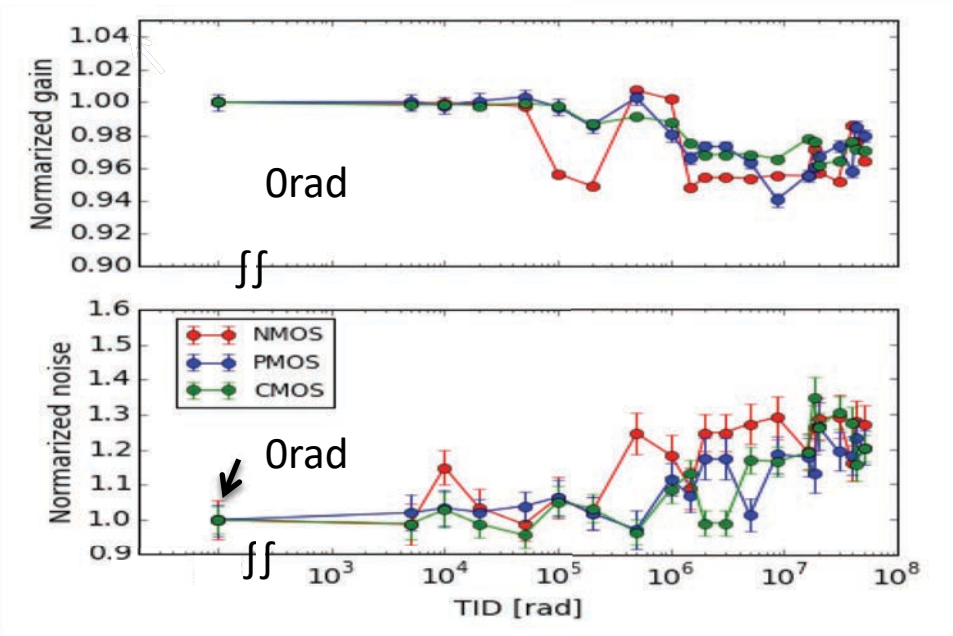
The prototype chips (CSA+Discr.) were irradiated with X-ray up to 50 Mrad

- Input transistor of CSA
  - NMOS
  - PMOS
  - CMOS
- Bias voltage: -100V

- **Gain degradation: <5%** ✓
- **Noise increase: ~30%**

- No significant difference between the 3 flavors

Normalized gain and noise of LF-CPIX



RADIATION HARDNESS (TID)

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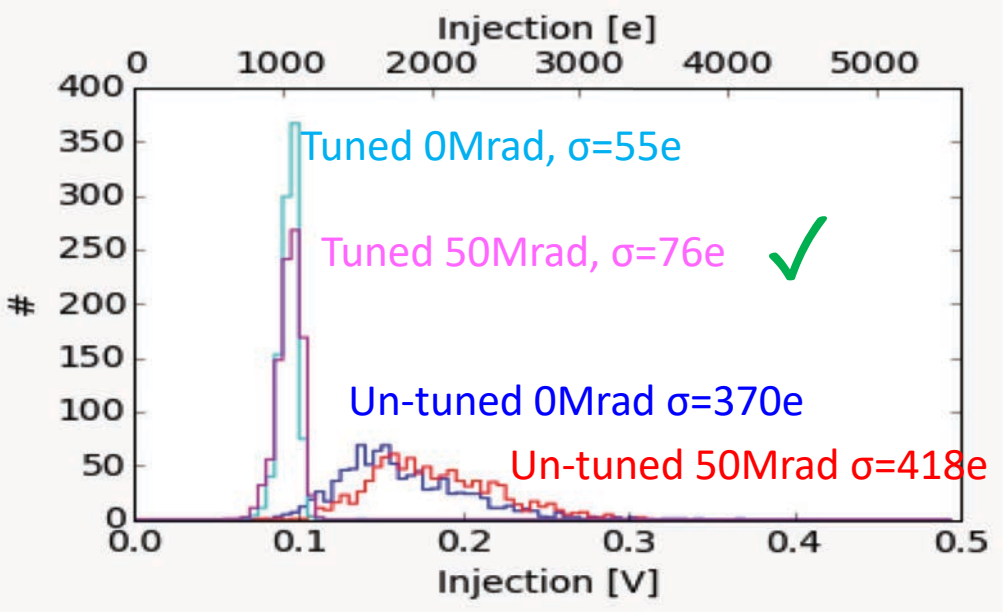
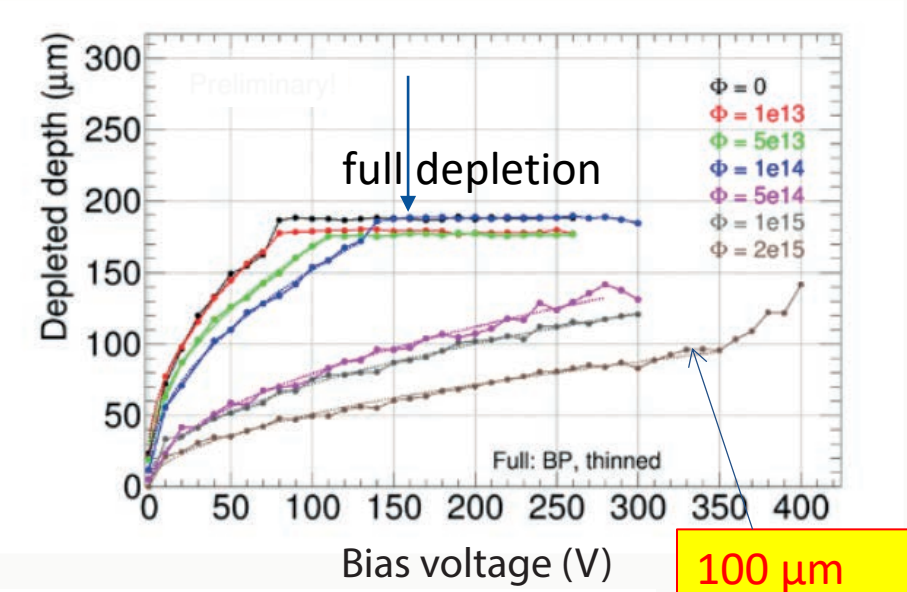
Un-tuned and tuned threshold dispersions of LF-CPIX (flavor=PMOS)



- The threshold is still tunable after TID=50Mrad (σ < 100e)
- Mitigation circuitry to avoid cross coupling of digital transient signals into pixel cell seems to work

RADIATION HARDNESS (NIEL)

The neutron irradiation test was done in JSI annealing @ 80min @60C



I. Mandić et al., JINST 12 (2017) no.02, P02021

✓

100 µm
after 2×10^{15}
=> large signal

RADIATION HARDNESS (NIEL)

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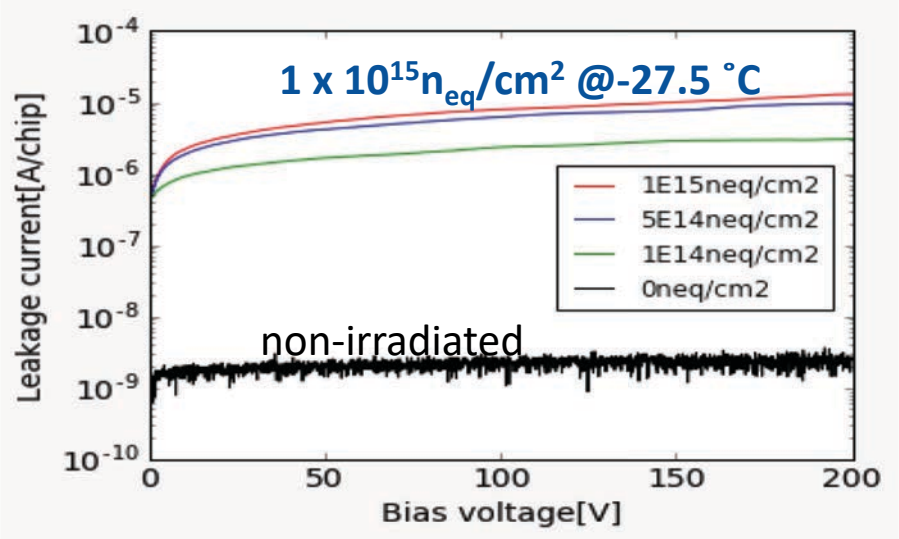
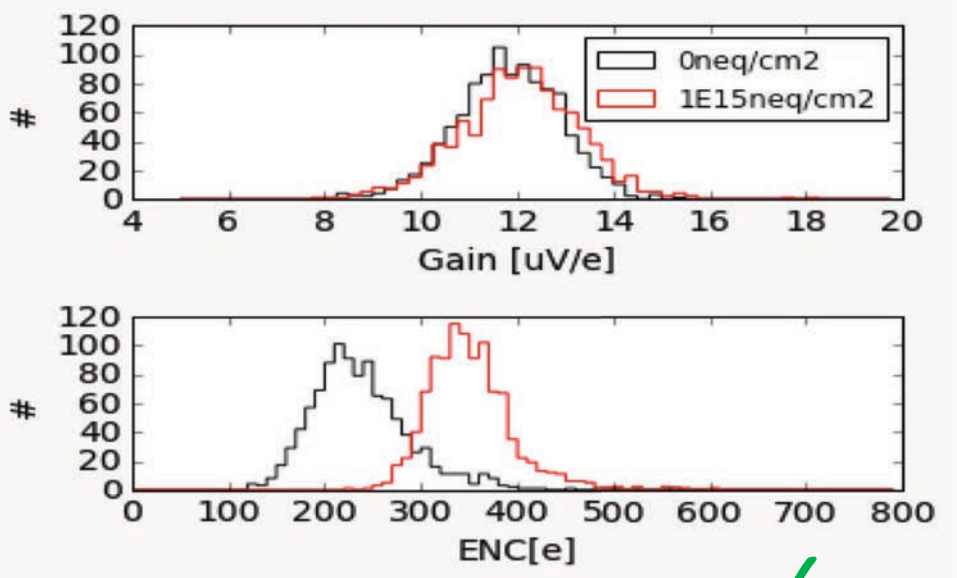
- I-V curve of MonoPix

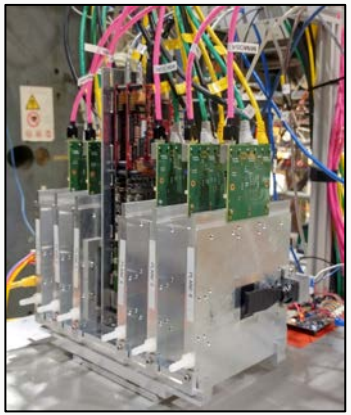


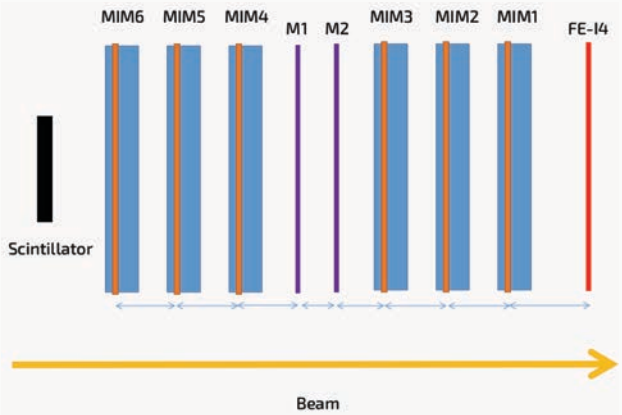
- Gain and noise



- Breakdown voltage is higher than 200V

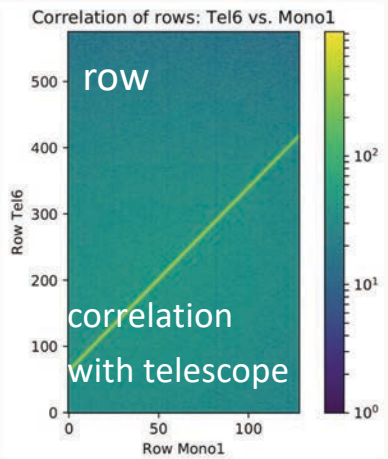
LF – MONOPIX IN TESTBEAM

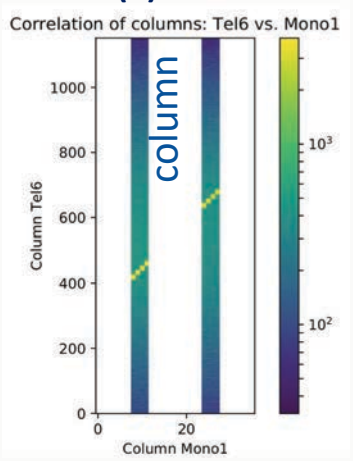




LF-MONOPIX (unirradiated and n-irradiated)
ELSA (2.5 GeV e-) CERN SPS H18 (180 GeV π)

Sample of event correlation (@SPS)
MONOPIX <-> MIM26 (6)





- **MIMOSA26 x 6**
  - Pixel size: 18.2 µm x 18.2µm
  - 1152 µs/frame (rolling shutter)
- **FE-I4 x 1**
  - Pixel size: 250 µm x 50 µm
  - Timing resolution: 25ns (trig. by scintillator + TLU)

TESTBEAM RESULTS -> EFFICIENCIES

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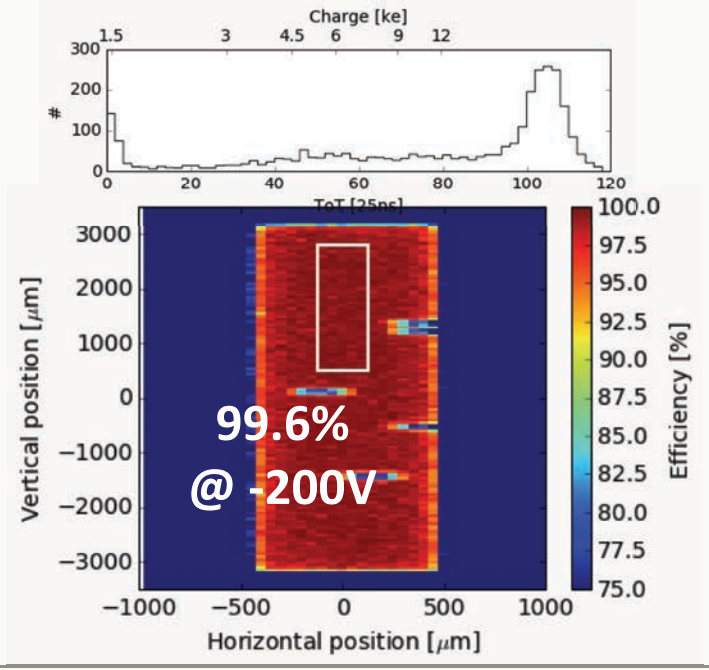
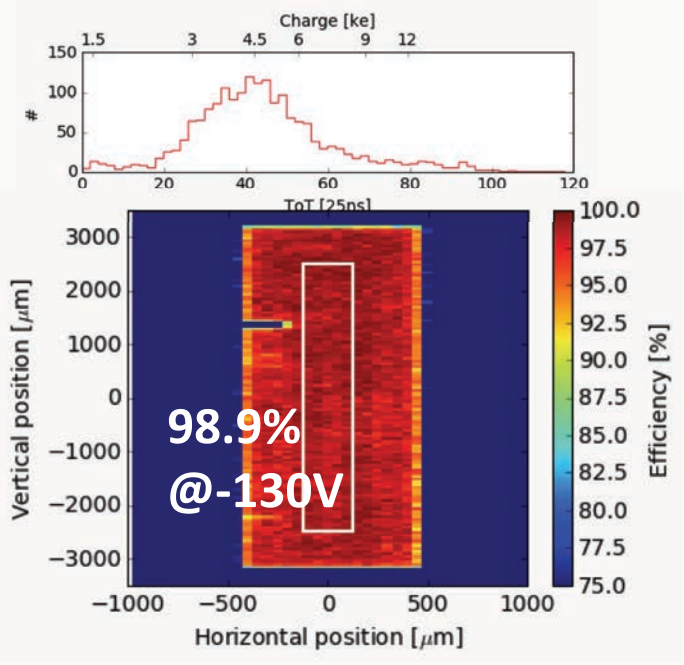
- **un-irradiated**
  - Hit efficiency **@ Noise occ. << 10^{-7} , thr~1700e- (<10^{-7} @ 1400e-)**
  - 1% masked pixels from noise tuning



- **Neutron irradiated (1 x 10^{15} n_{eq}/cm^2)**
  - Hit efficiency **@ Noise occ. < 10^{-8}, thr~1700e-**
  - < 0.2% masked pixels from noise tuning.



✓

IN-PIXEL EFFICIENCY

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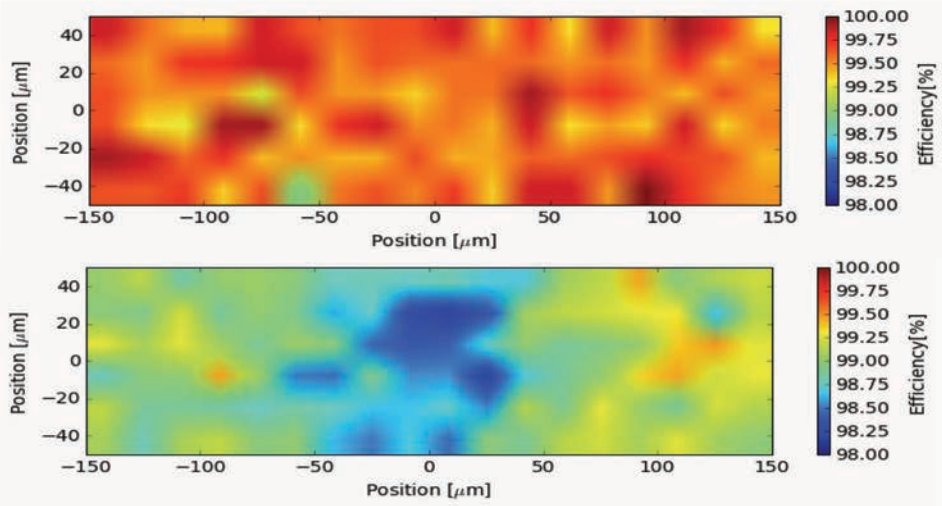
N-well (collection well)

P-well

Un-irradiated

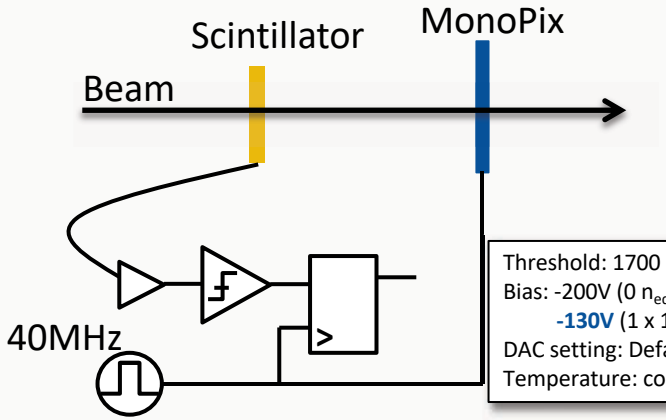
$1 \times 10^{15} n_{eq}/cm^2$



✓

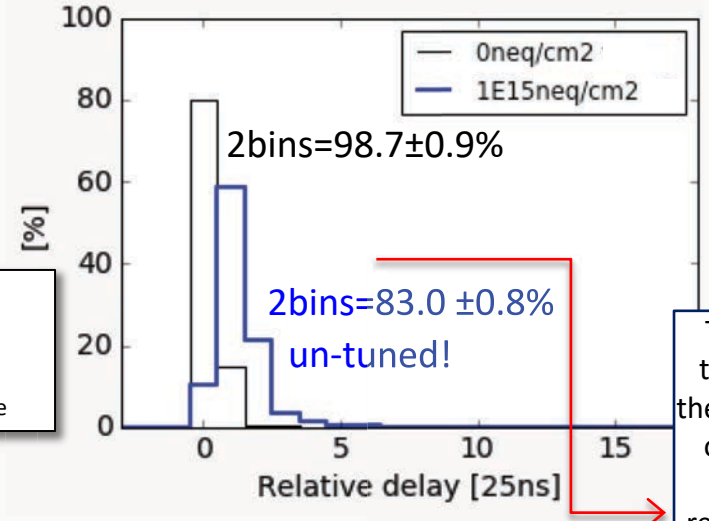
In the irradiated sample, the degradation of the efficiency is observed not only at the corner of pixels but also in the middle of the pixel => normal degradation

TIMING PERFORMANCE



Threshold: 1700 e-
Bias: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
DAC setting: Default
Temperature: cooled by dry ice

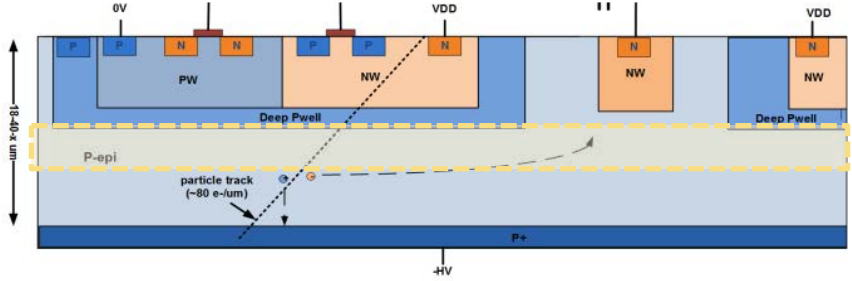
Delay = (Scintillator LE) – (MonoPix LE)



Two bins are "in-time" efficient, as the absolute position of the scintillator signal is random relative to the clock edge

- **>80% in-time efficient after** 1 x $10^{15} n_{eq}/cm^2$.
  Remarkable for C_D ~ 400fF and promising for new design with smaller C_D (Optimized FF)
- **Note that there is still room for improvement by tuning:**
  Optimize: CSA, discriminator currents, etc., higher bias voltage, back side process.

TJ – MALTA & **MONOPIX**



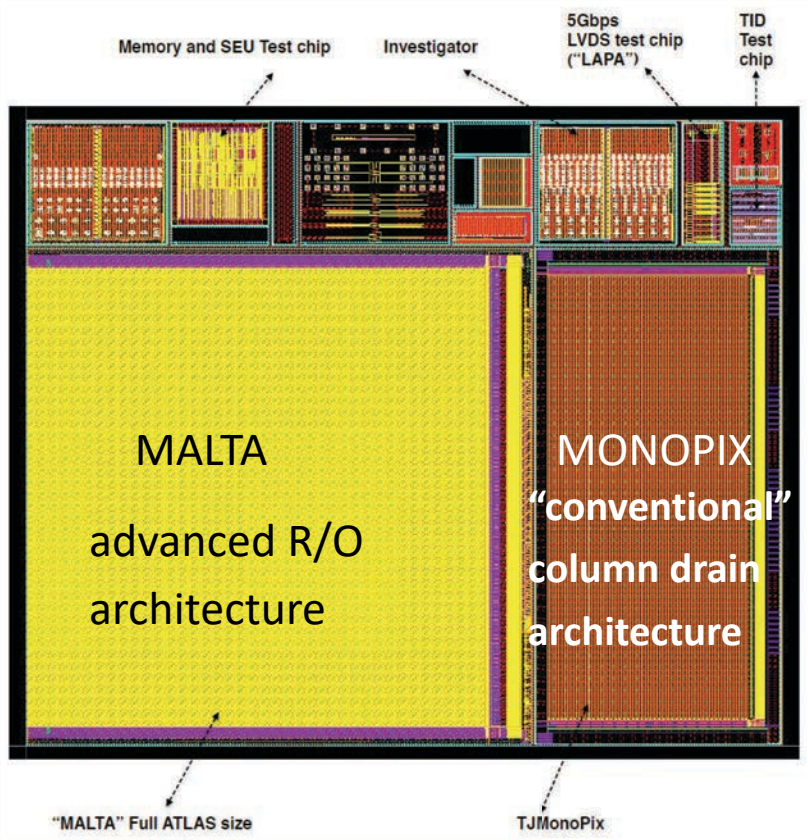
- **TowerJazz** 180 nm CMOS CIS
- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Thickness: 18 – 40 µm
- High resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Derived from ALICE development (CERN)

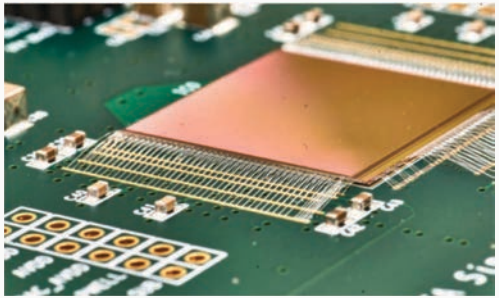
Design: CERN (MALTA), Bonn (MONOPIX)

Collaboration: M.Barbero[3], I. Berdalovic[2], C. Bespin[1], P. Breugnon[3], I. Caicedo[1], R. Cardella[2], Y. Degerli[4], N. EgidosPlaja[2], S.Godiot[3], F. Guilloux[4], T. Hemperek[1], T. Hirono[1], T. Kugathasan[2], C. A. Marin Tobon[2], K. Moustakas[1], P. Pangaud[3], H.Pernegger[2], P. Riedler[2], P. Rymaszeweski[1], E. J. Schioppa[2], W. Snoeys[2], M. Vandenbroucke[3], T. Wang[1] and N. Wermes[1]

[1]Bonn, [2]CERN, [3]CPPM, [4]CEA/IRFU

TJ – MALTA AND TJ - MONOPIX





- Sensor design is identical
- Front ends similar (different biasing schemes)
- R/O architectures very different

MALTA:

- Hits are stored using in-pixel flipflops and are transmitted asynchronously over high-speed buses to the end-of-column logic.
- No clock distribution over the active matrix – reduces power consumption!

TJ MODIFIED PROCESS: SENSOR DESIGN

- **Modified** TJ-180 process:
  Full depletion radiation tolerant to bulk damage
- **Small** n-well collection electrode,
- Small electrode to electrode distance **(small pixel size)**
  ↑ efficiency
- **Low analog power**

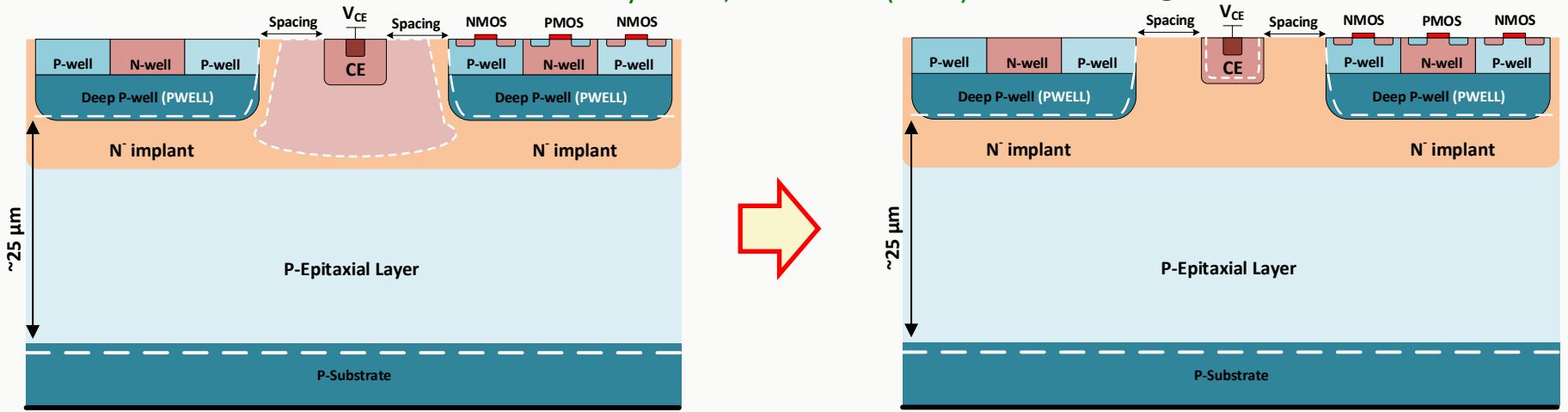
$$\frac{S}{N} \approx \frac{Q/C}{\sqrt{g_m}} \sim \frac{Q/C}{\sqrt[m]{P}} \Rightarrow P \sim \left(\frac{Q}{C}\right)^{-m}$$

- Biasing potentials: **PWELL, PSUB, V_{CE}**
- Reverse biasing will increase depletion and input signal amplitude
- High frontside bias possible with the **TJ-Monopix HV flavour**
- 0 PWELL **-6V**, 0 PSUB **-20V** (after full depletion)
- 0 HV **+50V 2V/µm** (including PSUB)

No reverse bias

W. Snoeys et al., NIM A871 (2017) 90 – 96.

High reverse bias



TJ-Monopix: Electronics Design

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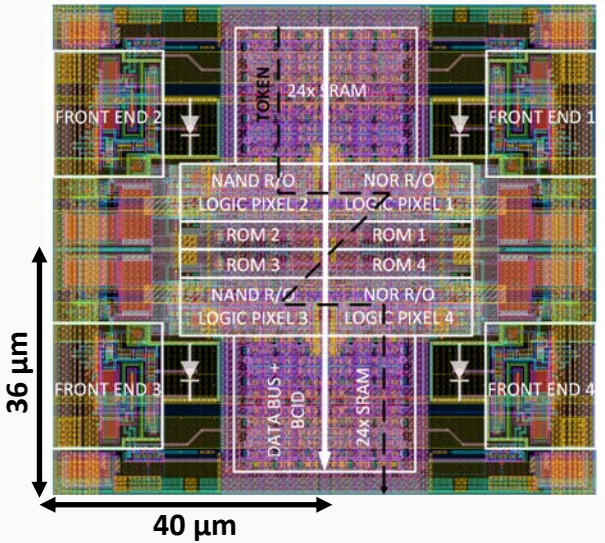
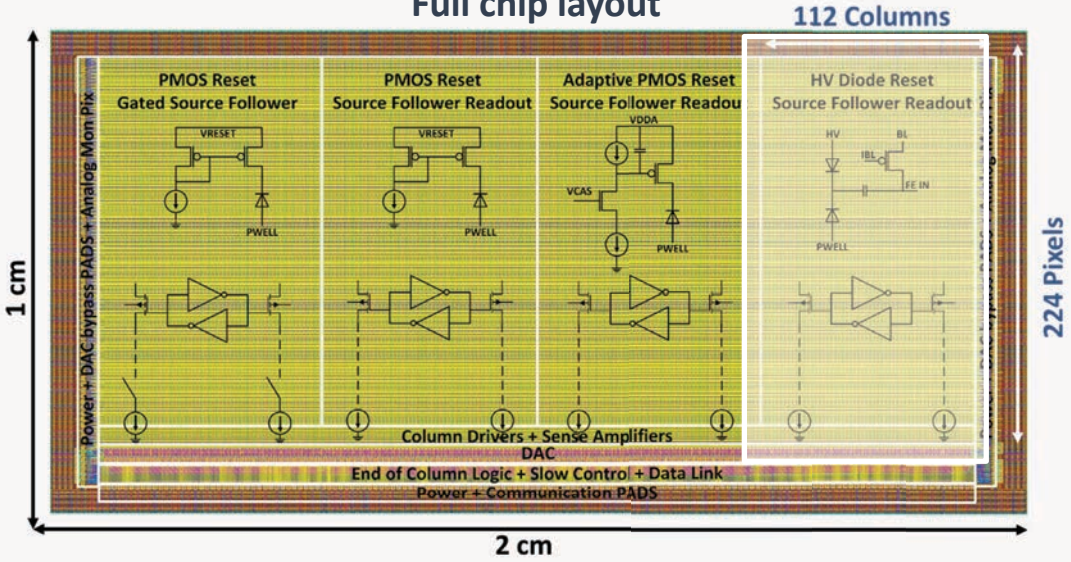
2x2 Pixel Layout



Full chip layout



- Non-conventional front-end design to take advantage of the low capacitance (voltage amplifier with LF feedback)
- **Low power:** 110 mW/cm^2
- **High gain:** 0.3 - 0.6 mV/e$^-$ (due to the small C_d)
- Optimized for **fast timing response**
- **Low threshold dispersion**, no in-pixel tuning

- 1x2cm^2 (1/2 of final size)
- 36x40µm^2 pixel size, 224x448 pixels
- 6-bit analog (charge) ToT information
- 4 different flavors implemented
- 160 MHz total data output

SOME TYPICAL CHARACTERISTICS (4 FLAVOURS)

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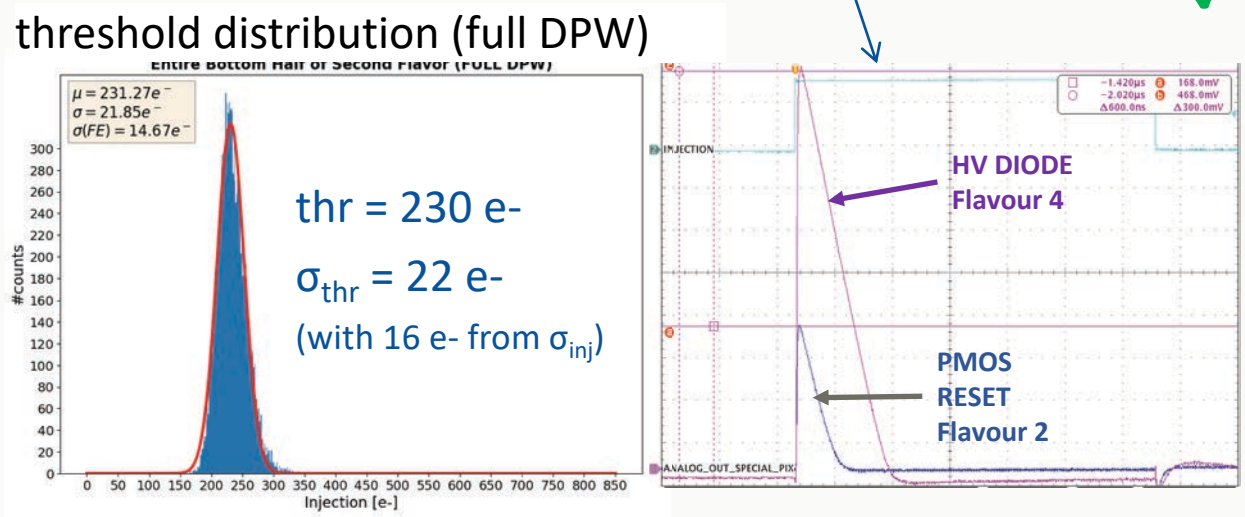
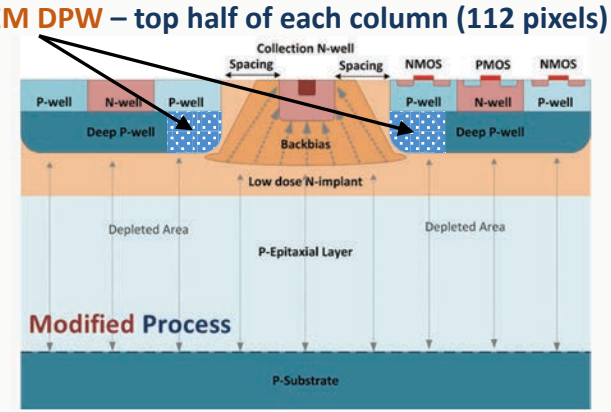
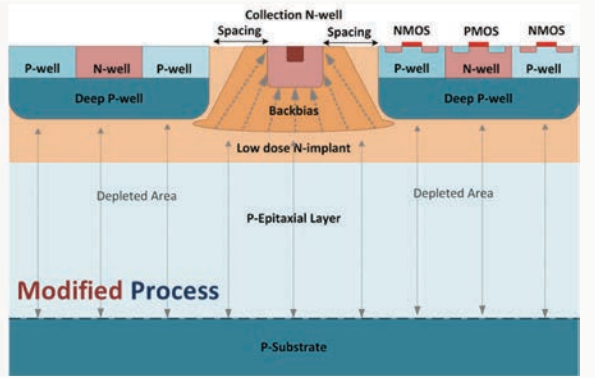
- All flavours working as expected: **thresholds (230 – 370) e-**
- ~ 0.1% masked pixels and **noise occupancy << 10^{-6} hits/BX**
- **ENC = (9 – 12) e- and σ_{thr} = (15 – 38) e-**
- Best results with front side diode **HV biasing (incr. signal)**
  -> can decrease C_{in} to < 1 fF







TJ-Monopix characterization: Gain

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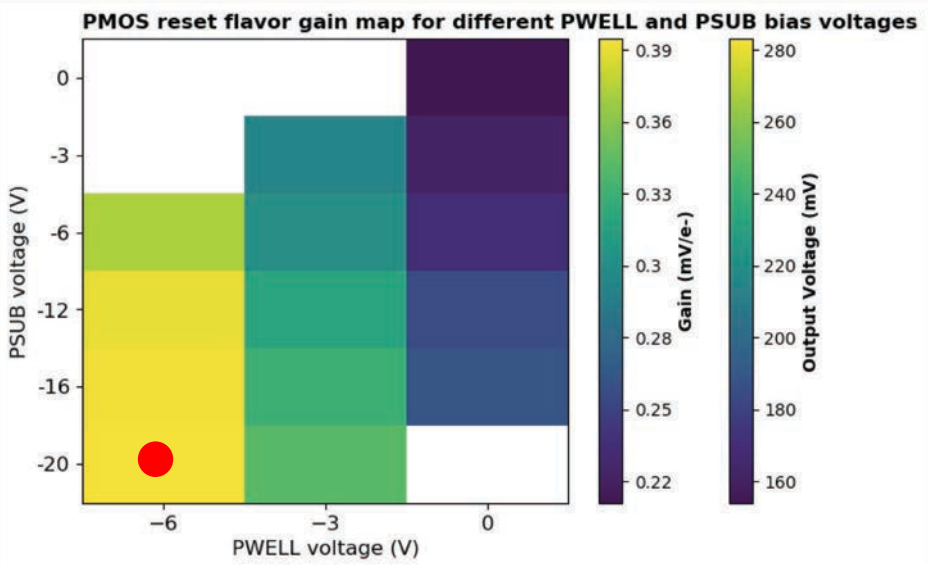
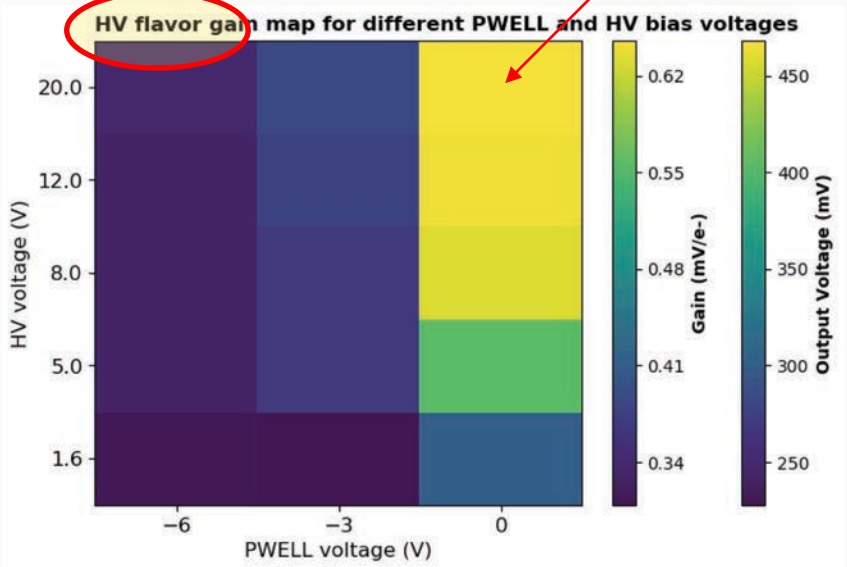
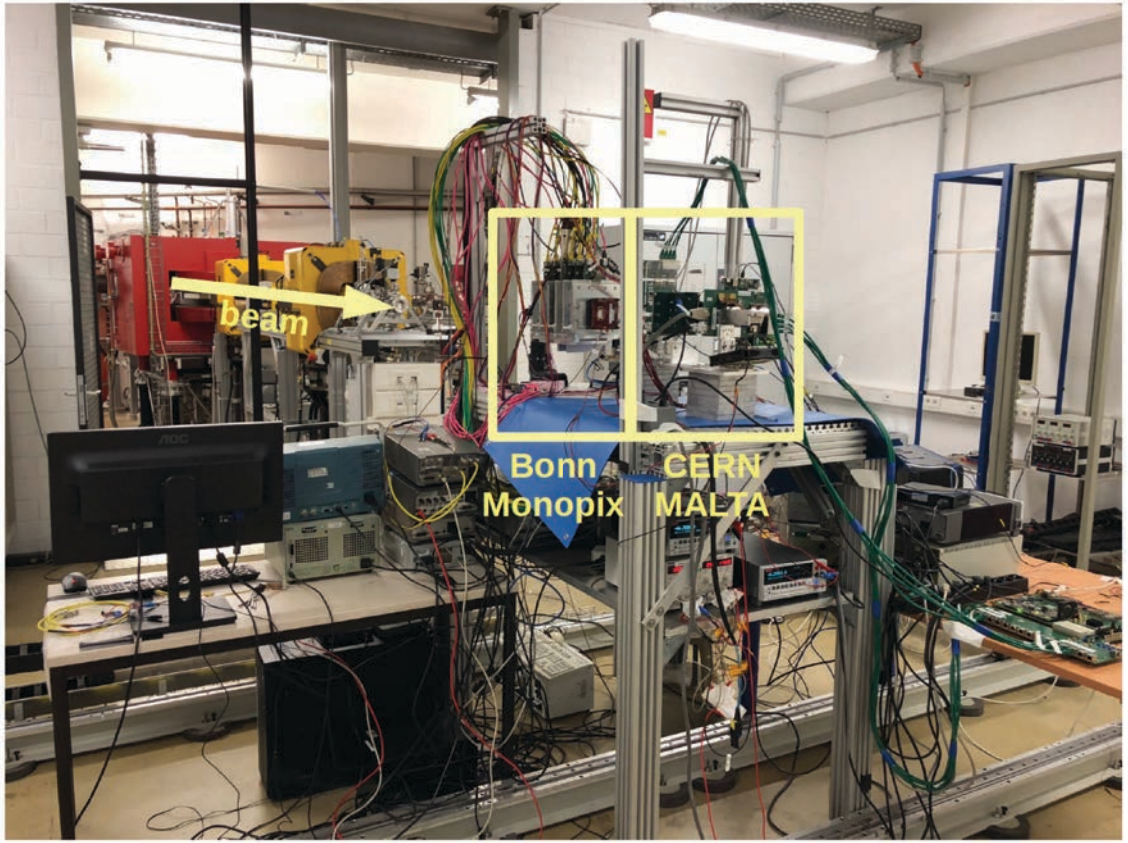
- Gain dependence on the sensor biasing potentials for the PMOS reset (left) and HV (right) flavors
- PSUB was set to -6V for the HV map. For HV $\geq$ 5V it has minimal impact
- Gain is affected by the varying detector capacitance (depletion)
- **Up to 0.65mV/e- gain** can be achieved, **≅70% maximum gain increase** compared to the PMOS reset flavor

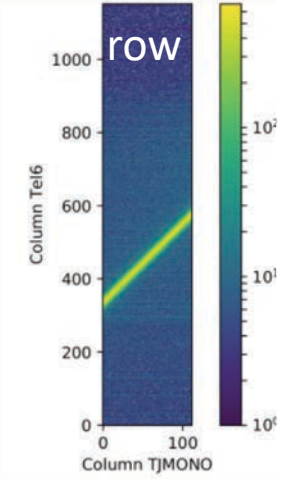
high gain

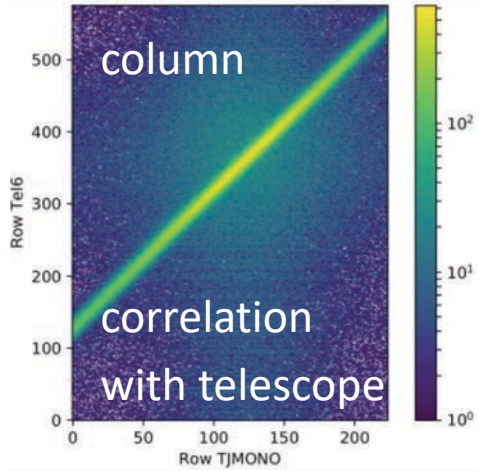




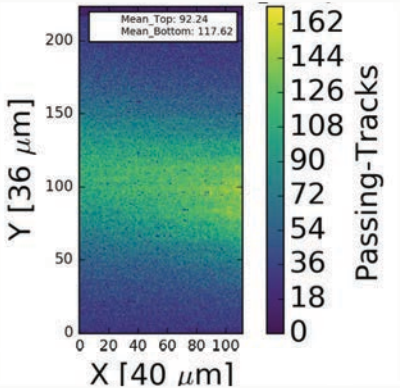
TESTBEAM 2.5 GEV E- (ELSA) AND CERN SPS (MALTA ONLY)







beam profile



SMALL ELECTRODE AND RADIATION TOLERANCE

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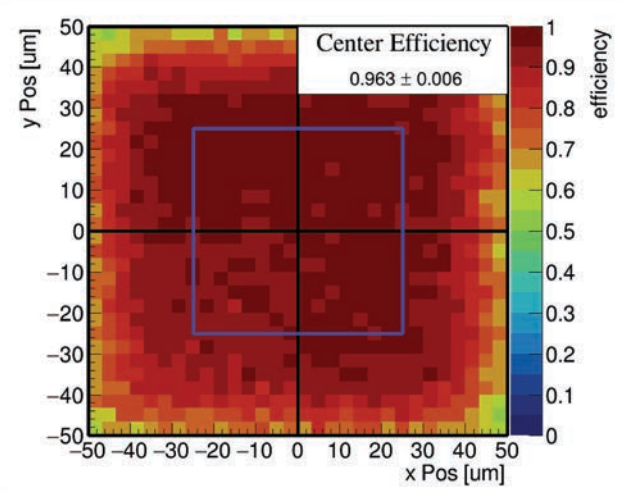
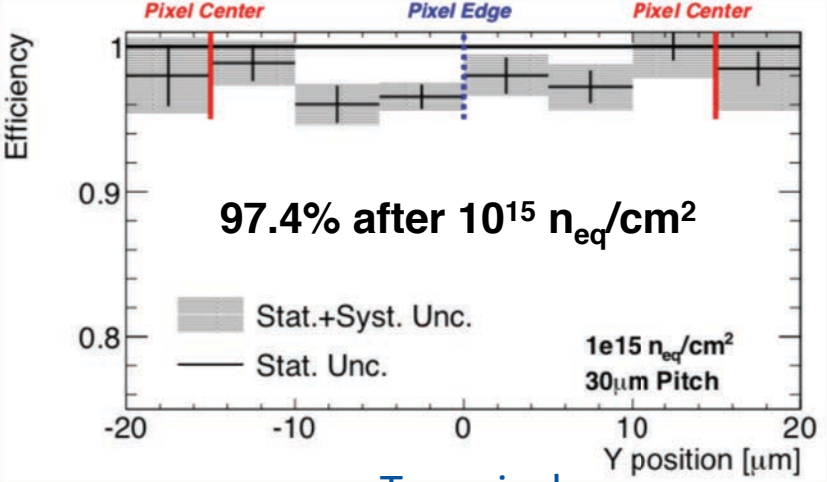
Investigator Chip to investigate modified technology

JINST 12 (2017) no.06, P06008

50x50µm pixel pitch,
3µm electrode,
40µm opening

30x30µm pixel pitch,
3µm electrode
9µm opening





Two pixels

SOME VERY PRELIMINARY IRRADIATION RESULTS

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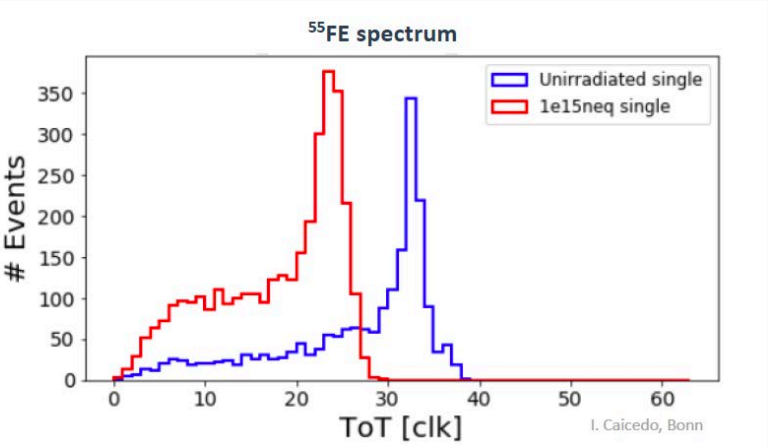
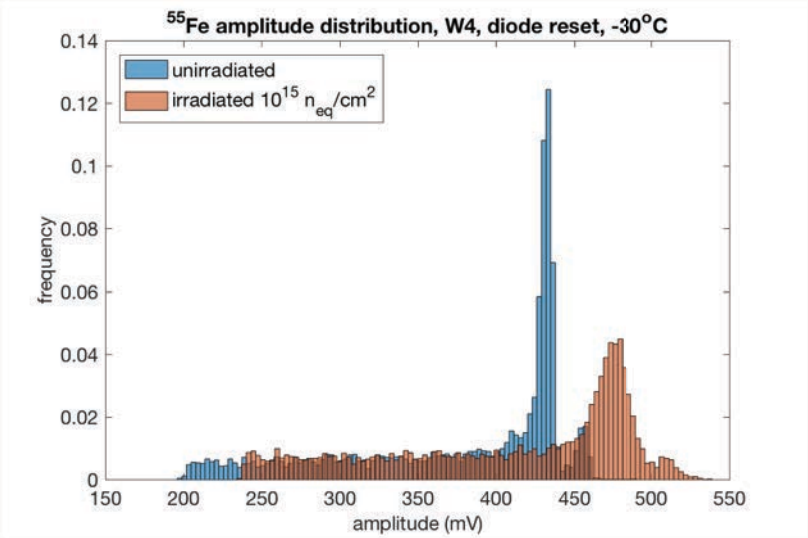
After 1 x 10^{15} n_{eq}/cm^2

MONOPIX



MALTA



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ANOTHER BRANCH TO WATCH

PASSIVE CMOS PIXEL SENSORS

PASSIVE CMOS SENSORS

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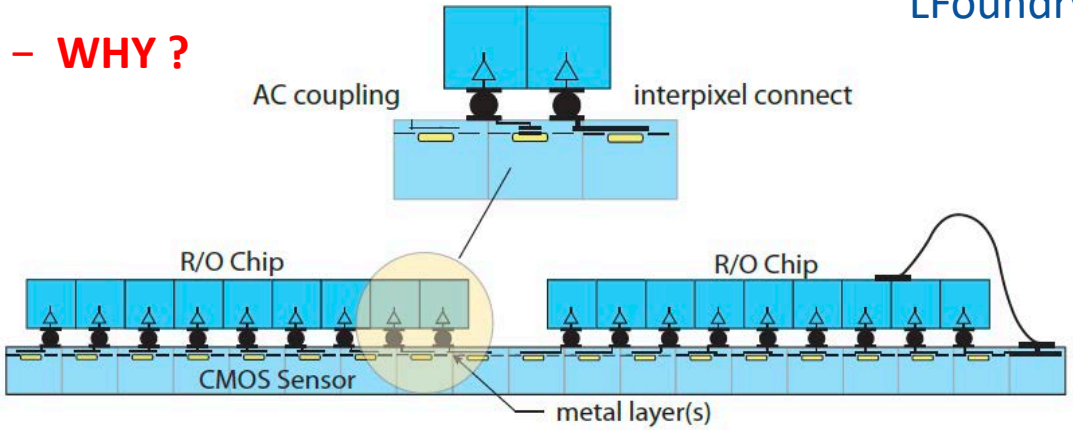
- **WHY ?**

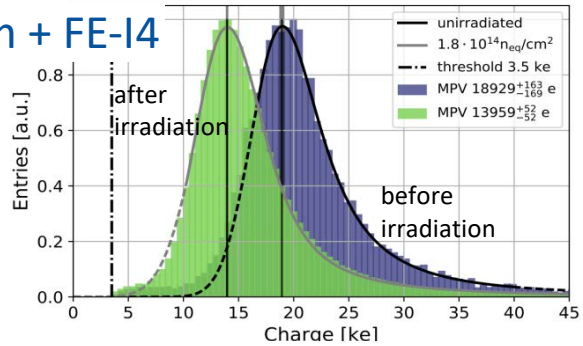


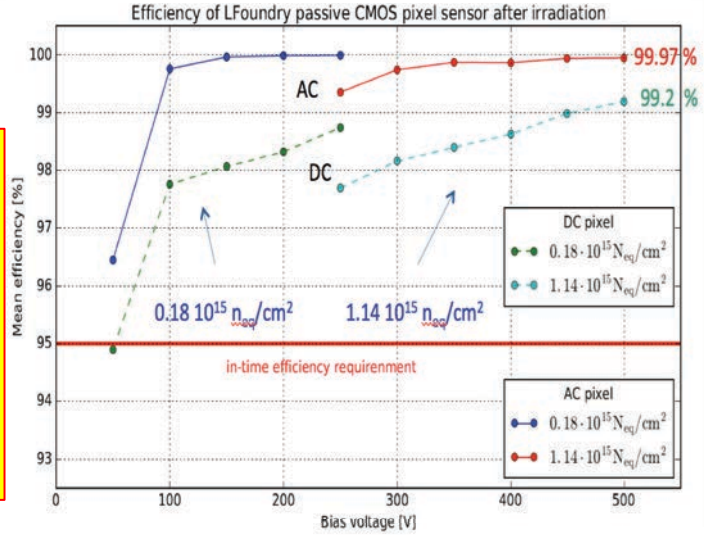
- Cheaper
- High wafer throughput
- Exploit metal layers for AC coupling and rerouting

Results

- **bias 120 V** -> 500 V
- **~220 µm** depletion depth
- same as standard sensors in i_{leak} and noise
- **high eff. after** ($1x10^{15} n_{eq}/cm^2$)

LFoundry 150 nm + FE-I4

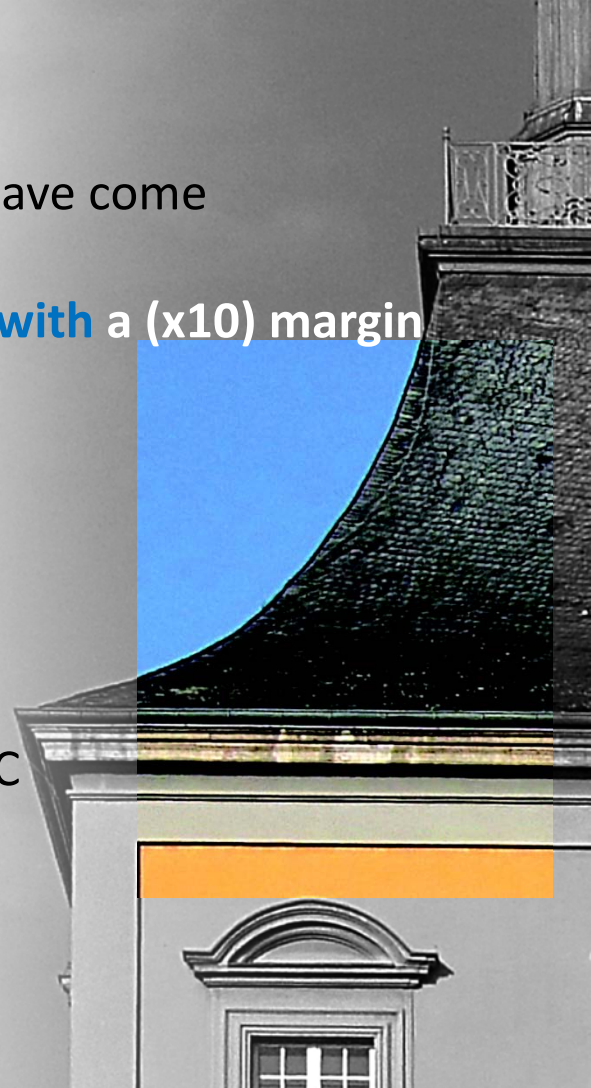




D.-L. Pohl et al., JINST 12 (2017) no.06, P06020

CONCLUSIONS

- Depleted CMOS pixels (DMAPS) combining HV and HR have come a big step forward towards usage @ HL-LHC
- Simulation: Col-drain architecture **meets 5th layer rates with** a (x10) margin
- Large FF (AMS & LFoundry) features:
  - high beak down voltage
  - large signal
  - high efficiency after 10^{15} n_{eq}/cm^2
- Small FF (TJ) features (MALTA / Monopix)
  - low capacitance, low noise
  - low power (60 mW / 110 mW/cm^2 in matrix), large Q/C
  - all flavours working in testbeams
  - irradiated to 2 x 10^{15} n_{eq}/cm^2 -> results to come



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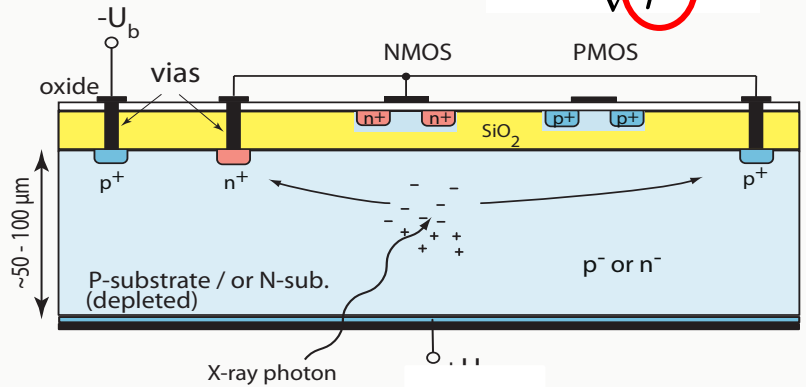
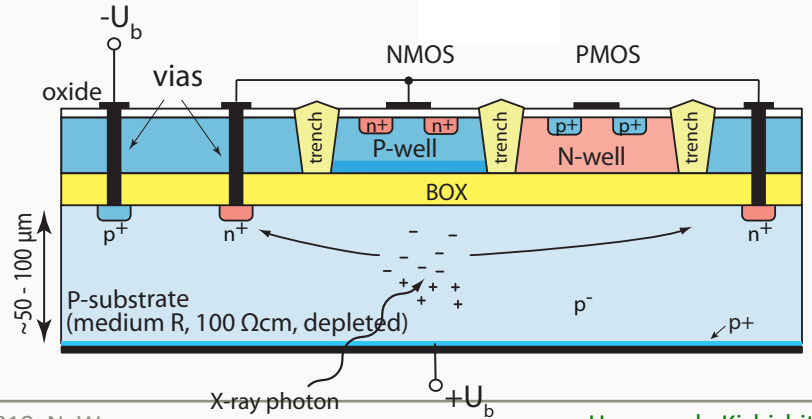
BACKUP

SOI MONOLITHIC PIXELS

FD CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$





- **fully depleted SOI (thin film)**
  @ Lapis/KEK
- issues
  - back gate effect
  - coupling of sensor to circuit
  - radiation (TID) issues due to BOX
- cures developed in recent years
  - buried p-well, nested wells
  - “double SOI” structures

- **HV-SOI (thick film)**
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

Hemperek, Kishishita, Krüger, Wermes, NIM A796 (2015) 8-12