A novel HV silicon JFET for ATLAS, and other silicon R&D activities at BNL

32nd RD50 workshop – 4-6 June 2018 Hamburg

Gabriele Giacomini, Wei Chen, Francesco Lanni, David Lynn, Alessandro Tricoli
(Brookhaven National Lab)

Enrico Rossi
(Stony Brook University and Brookhaven National Lab)

BROOKHAVEN NATIONAL LABORATORY

U.S. DEPARTMENT OF ENERGY

Outline

Activities on-going at Brookhaven National Lab:

- HV silicon JFET for multiplexing in ATLAS Inner Tracker (ITk) for HL-LHC phase
  → BNL is involved in strip sensor stave R&D and constructions

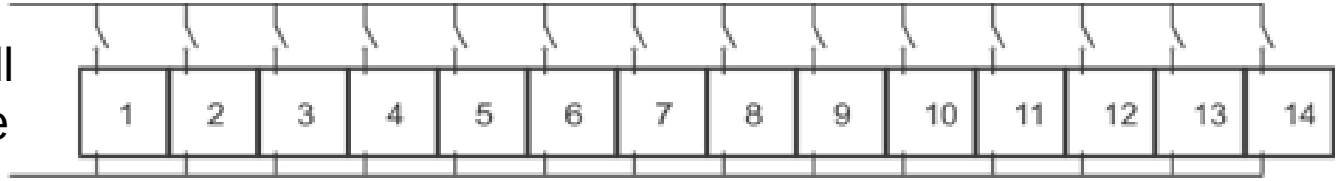
- LGAD R&D
  → High Granularity Timing Detector

- Commissioning of BLIP, a new irradiation facility for silicon R&D

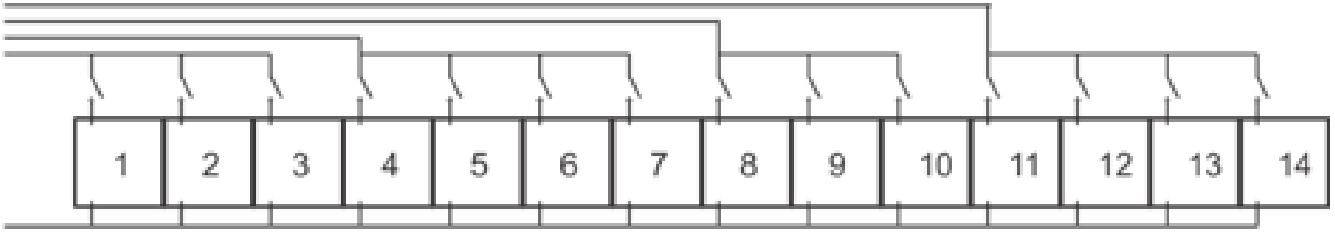
HV multiplexer in ATLAS ITk

- Cable space limitations do not permit each module in the stave to have its own HV power supply
- The solution has been proposed by BNL: have multiple modules connected to the HV bus with slow controlled switch that can disconnect malfunctioning sensors

Single HV supply for all strip sensors in a stave



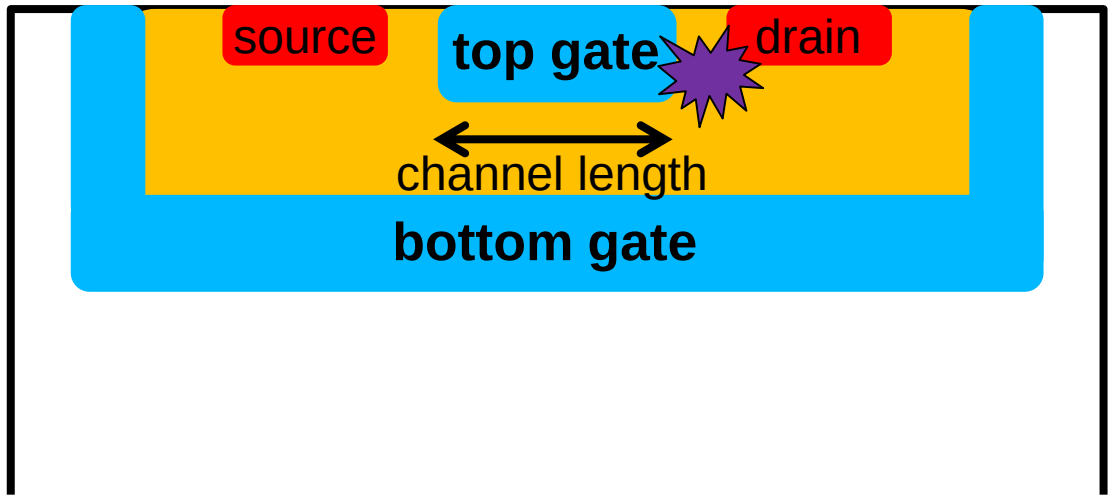
A HV supply for 3 or 4 strip sensors



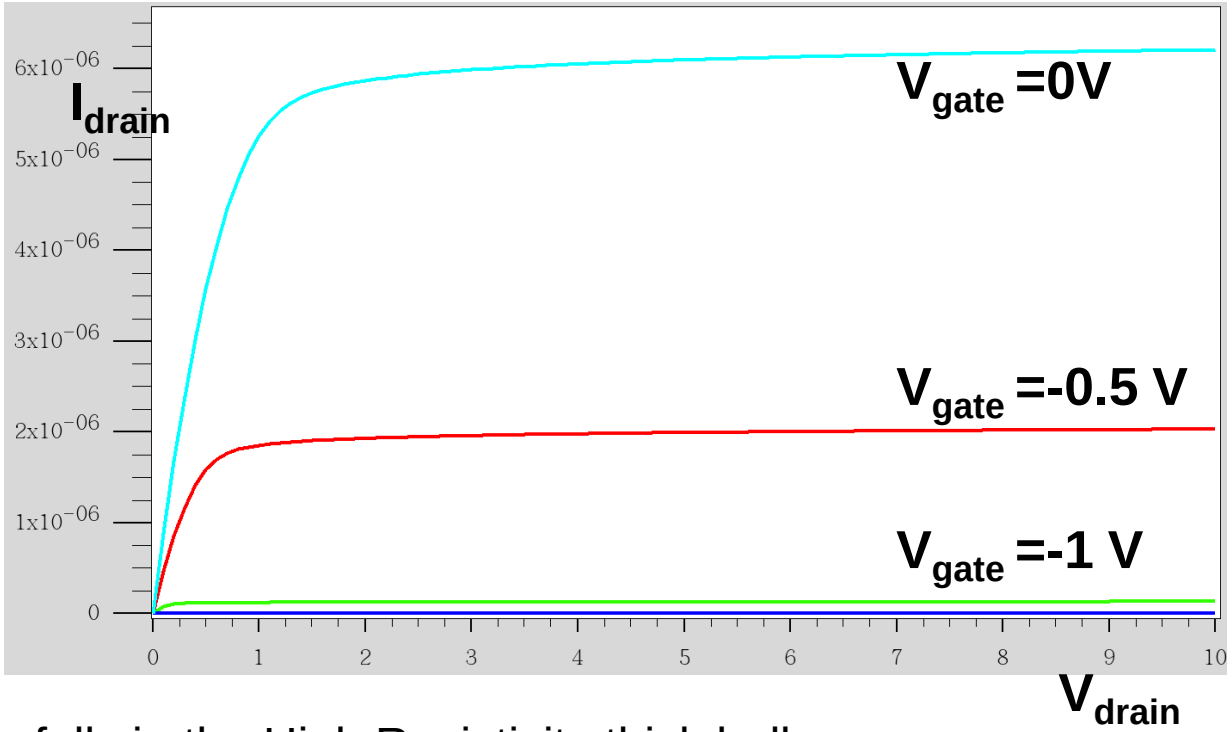
- Transistor must switch greater than 500V, be radiation hard and operate in a 2 T magnetic field
- Converged on Panasonic GaNFET as single candidate
- devices powered either in on- or off-state survived irradiations with pions, neutrons, photons and protons
- Can we do a HV-JFET made of silicon ?

Standard planar JFET

It is a basic electronic device solvable analytically.
Essentially a 1-D structure.
$V_{drain\text{-}gate}$ is limited by the breakdown at that junction.



n-channel, doping 1e16cm^{-3}, thickness =1μm,
width = 1μm, length = 5μm

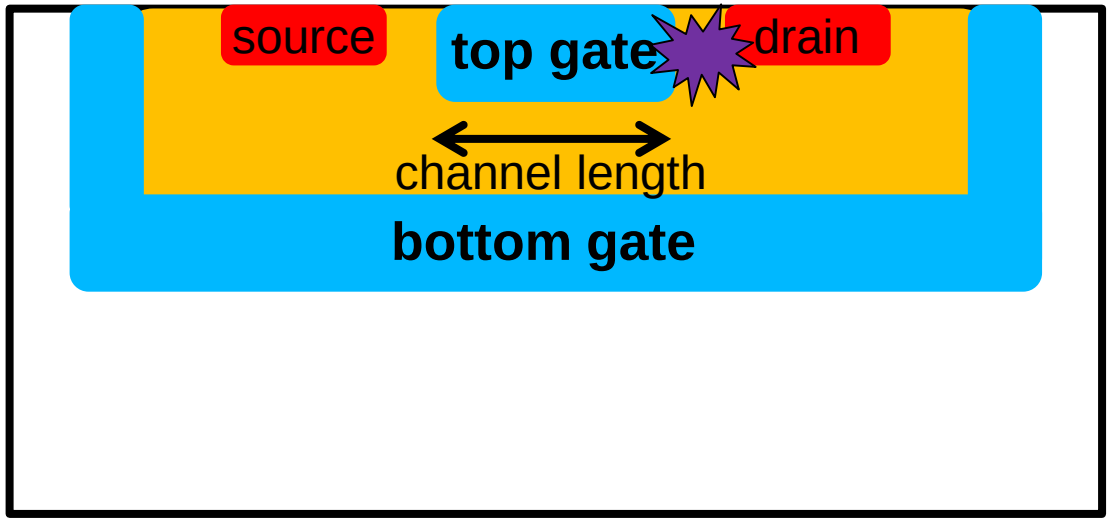


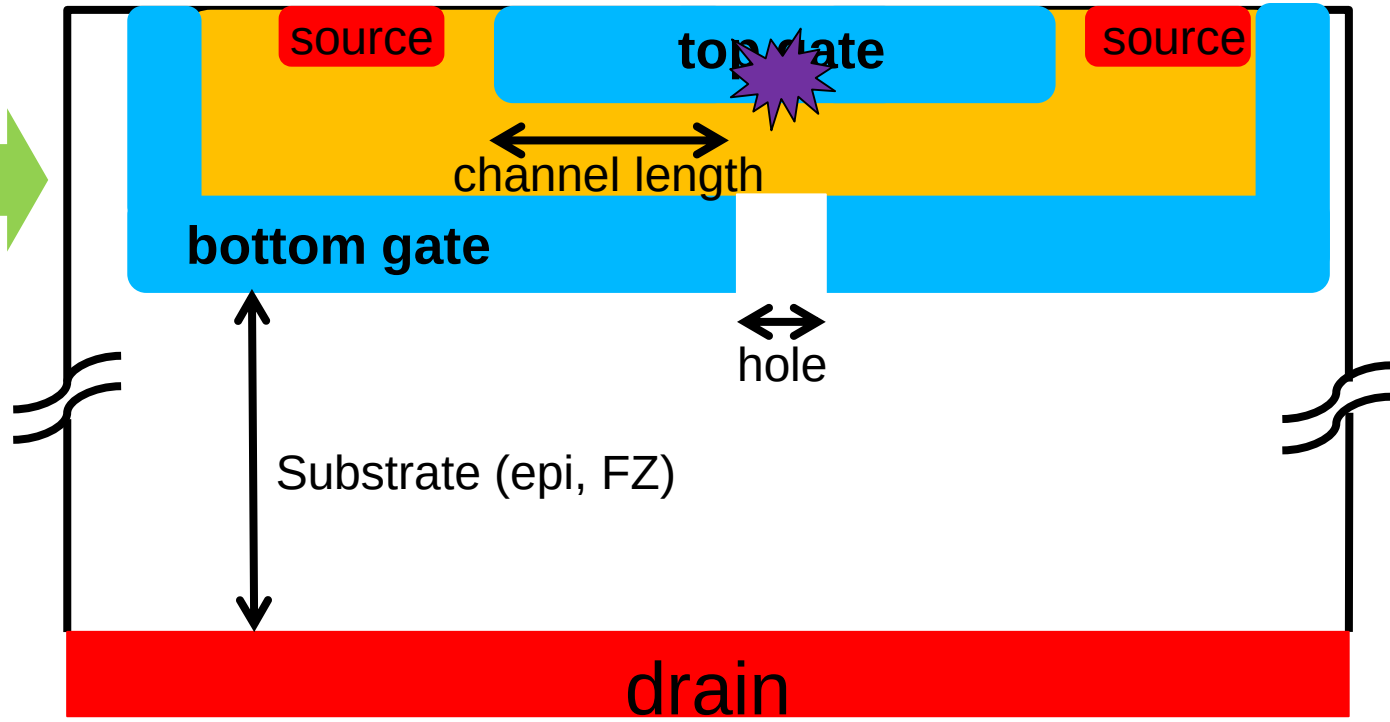
Power semiconductor devices go vertical: the high voltage falls in the High Resistivity thick bulk.
Example: power MOSFET, thyristors (SCR), pin diode.

Can we do a Vertical JFET?

The vertical HV Silicon JFET

We can modify the structure of the standard JFET by making a hole in the bottom-gate.
Over the hole, the top-gate. The channel and the source as in the standard JFET. The drain is the back contact.
The current flows (= drifts) from source to drain through the hole in the bottom-gate.
The high voltage applied to the drain falls in the thick substrate, being the bottom-gate almost a planar implant.



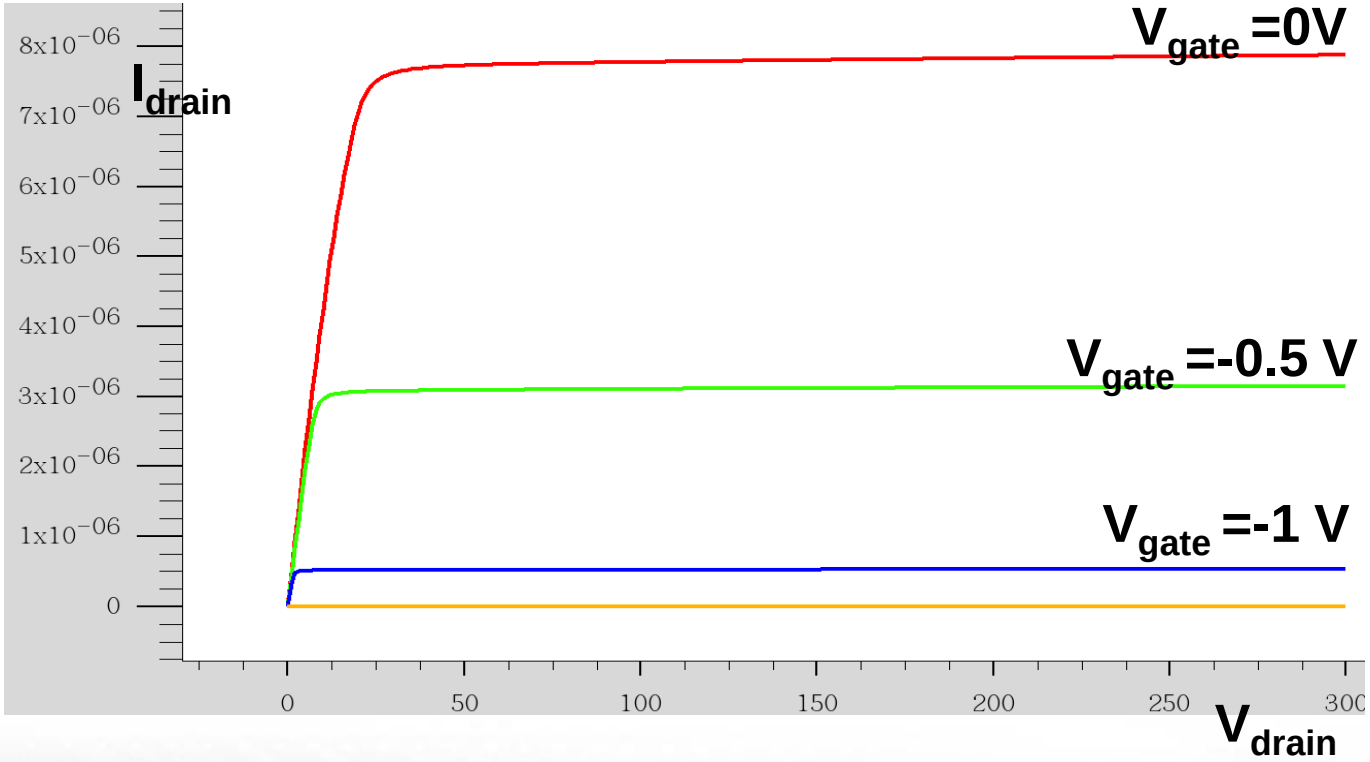


The highest electric field develops at the junction top-gate/channel, so special care in the choice of the parameters (hole width, channel doping concentration).
GR termination also needed at the border of the bottom-gate.

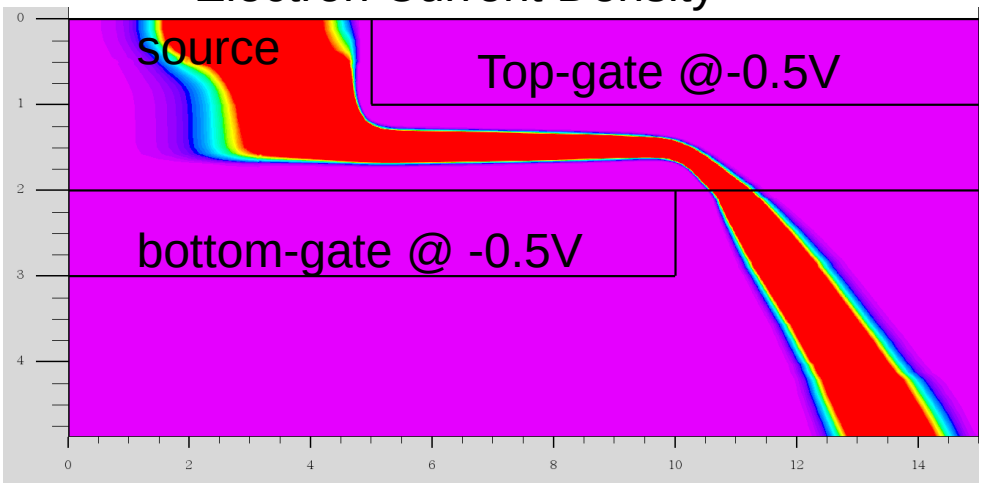
TCAD simulations

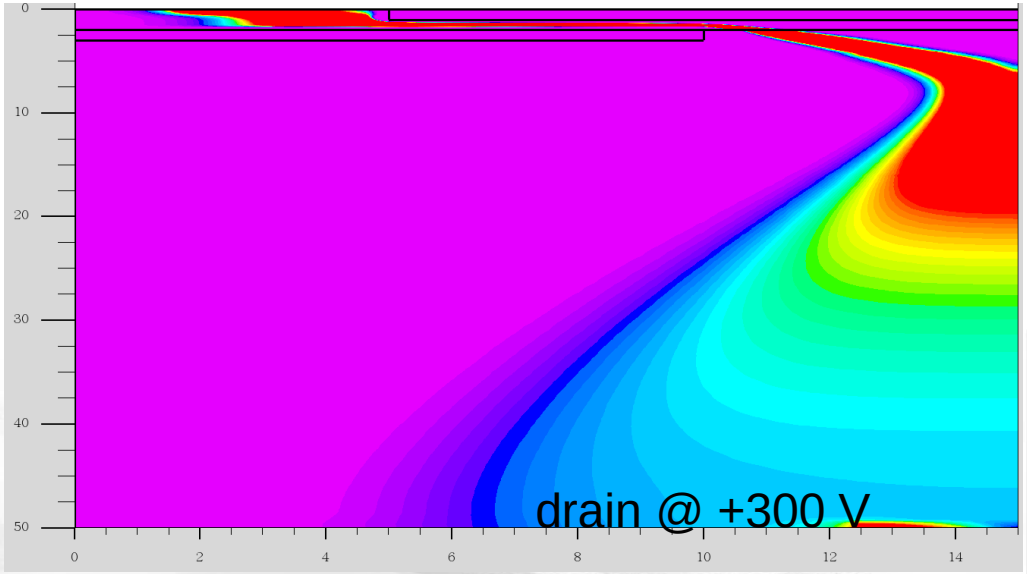
TCAD simulations show that it works!

- The ON currents are essentially the same.
- Also the pinch-off gate-voltage is the same.
- high $V_{D\ saturation}$, because the bottom-gate shields the drain voltage, so that the channel gets its pinch-off voltage at high V_D



Electron Current Density





The current flows from source to drain without encountering any potential barrier. Then it spreads into the resistive bulk.

A few Points to be considered

Choice of the substrate:

→ resistivity as low as possible to avoid a high-resistance path for the ON current. But, V_{BD} depends on the doping, so a compromise has to be chosen. Once we set the max operational voltage (< V_{BD}), we can choose the doping and the thickness of the epitaxial layer.

For example, we want V_{BD} > 600V, so N_C = 1e14cm^{-3} and 50 μm thick is OK

Fabricated test diodes show V_{BD} > 600V, but the GR termination has to be redesigned, for not standard N_C.

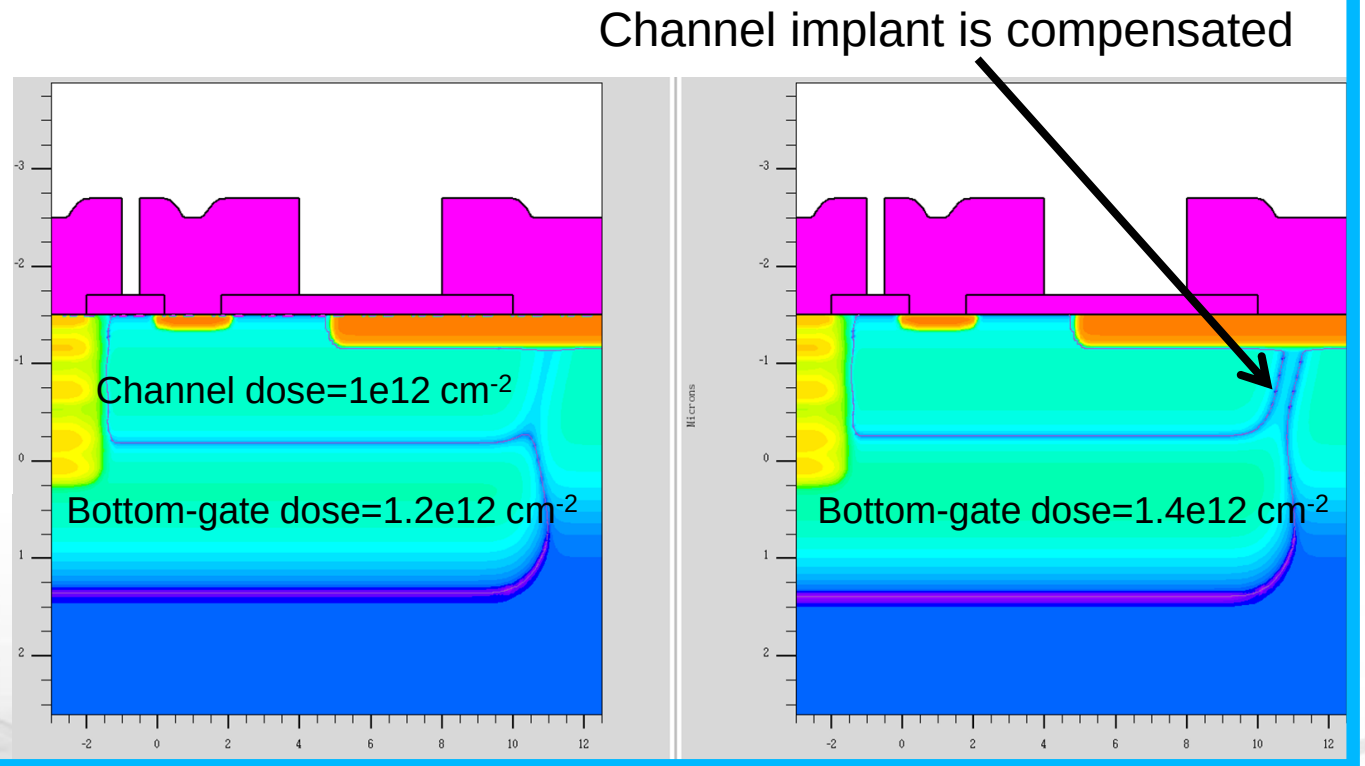
Dimension of the hole:

The larger the hole, the higher the electric field, but the smaller the V_{Dsat}, also here a compromise.

Horn effect:

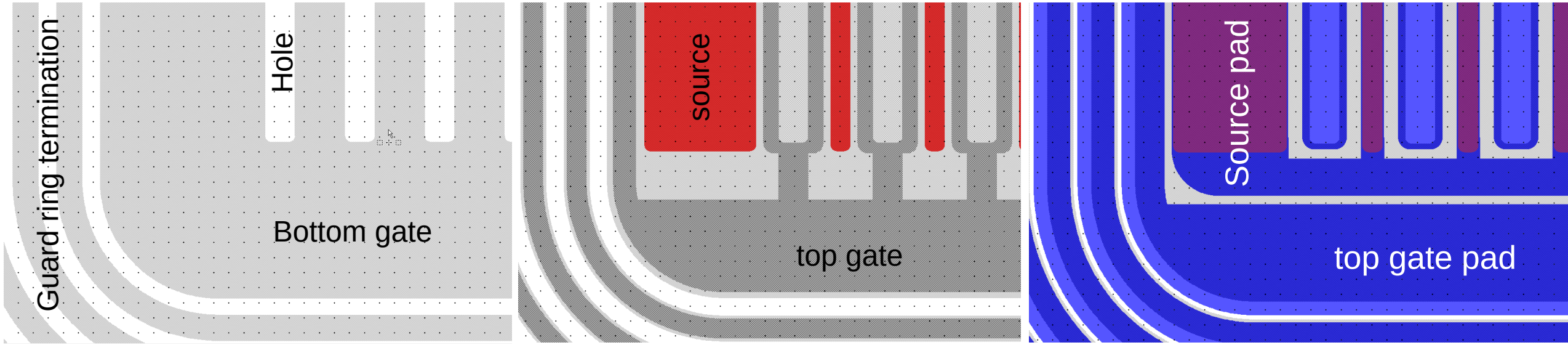
When implanting the bottom gate, the implant is blocked in the hole region by a thickness of resist and oxide. But at the border of this region some implant passes and leaves an unwanted doping. This horn can compensate the channel doping. So in turns, it sets a limit to the doping of the bottom gate.

For the real, fabrication we can choose within a limited range of parameters (splittings will help).



The layout-1

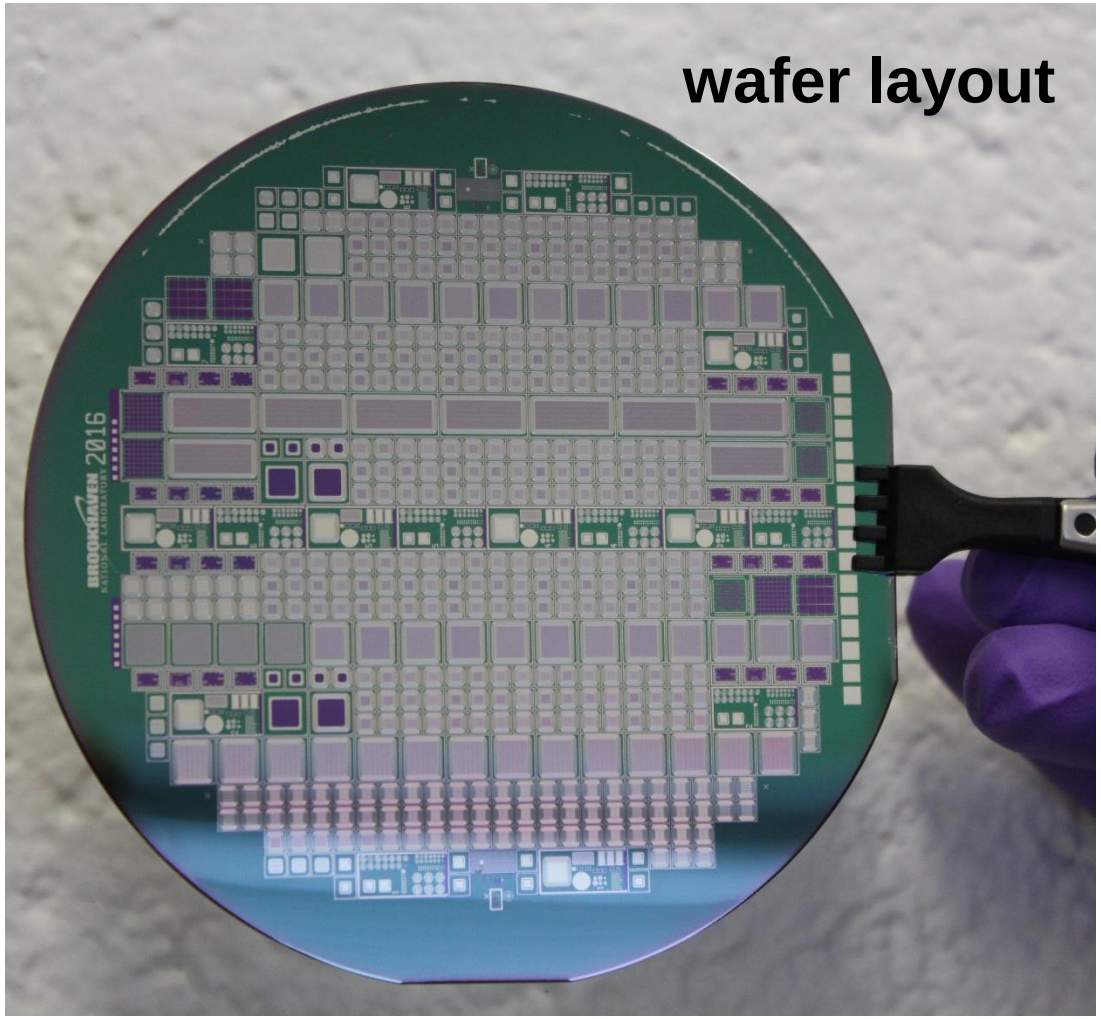
6 photolithographic masks, 4 implants.

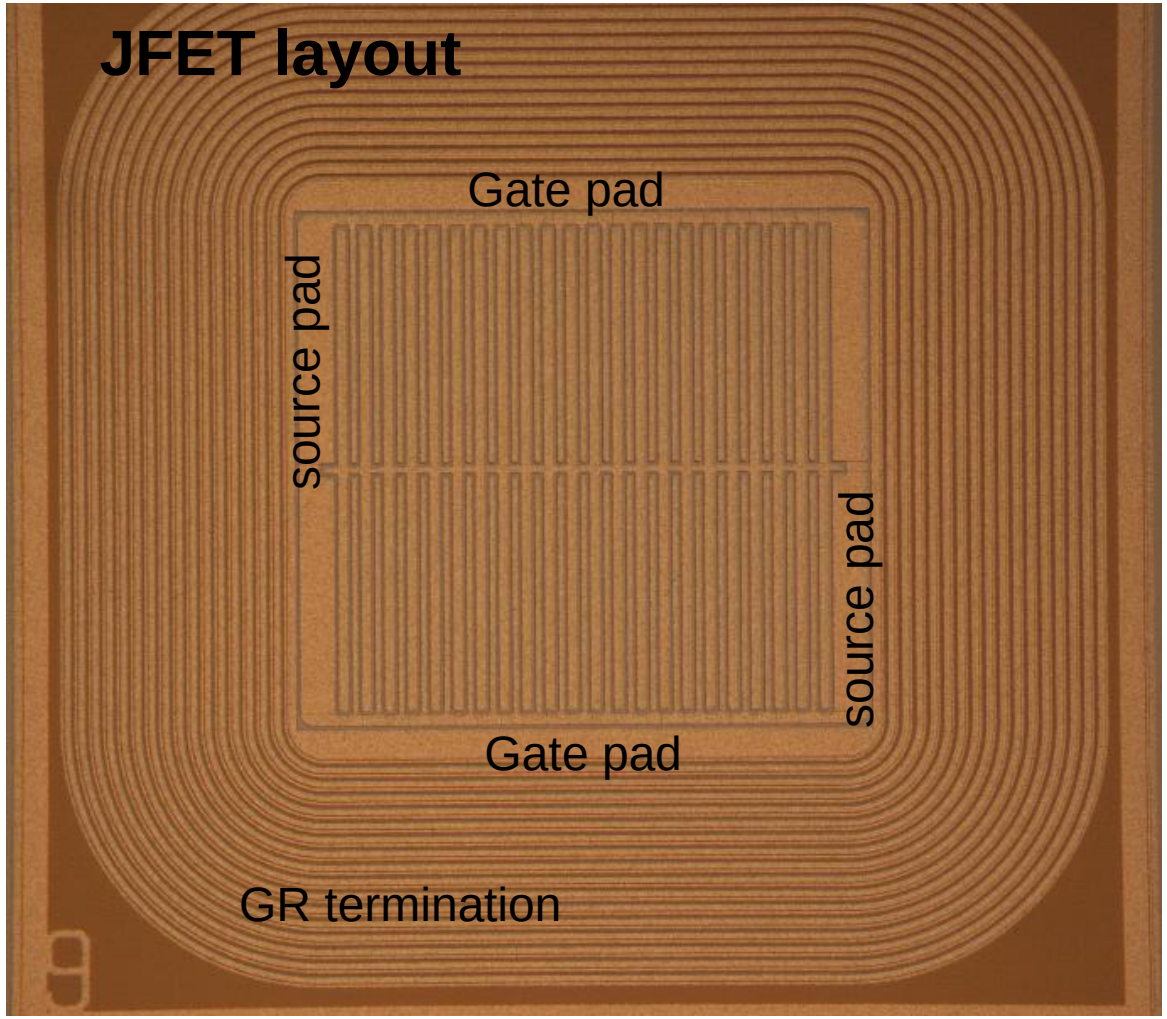


Interdigitated design to increase the gate width and thus the ON current (especially after irradiation).
The active area is 1x1 mm^2, which sets the gate width to 20 cm.
Triode configuration, top-gate connected to the bottom-gate.

Both *n*-type and *p*-type JFET, on 4” epitaxial wafers (TOPSIL): 50μm thick, N_C~ 1e14cm^{-3}.

The layout-2



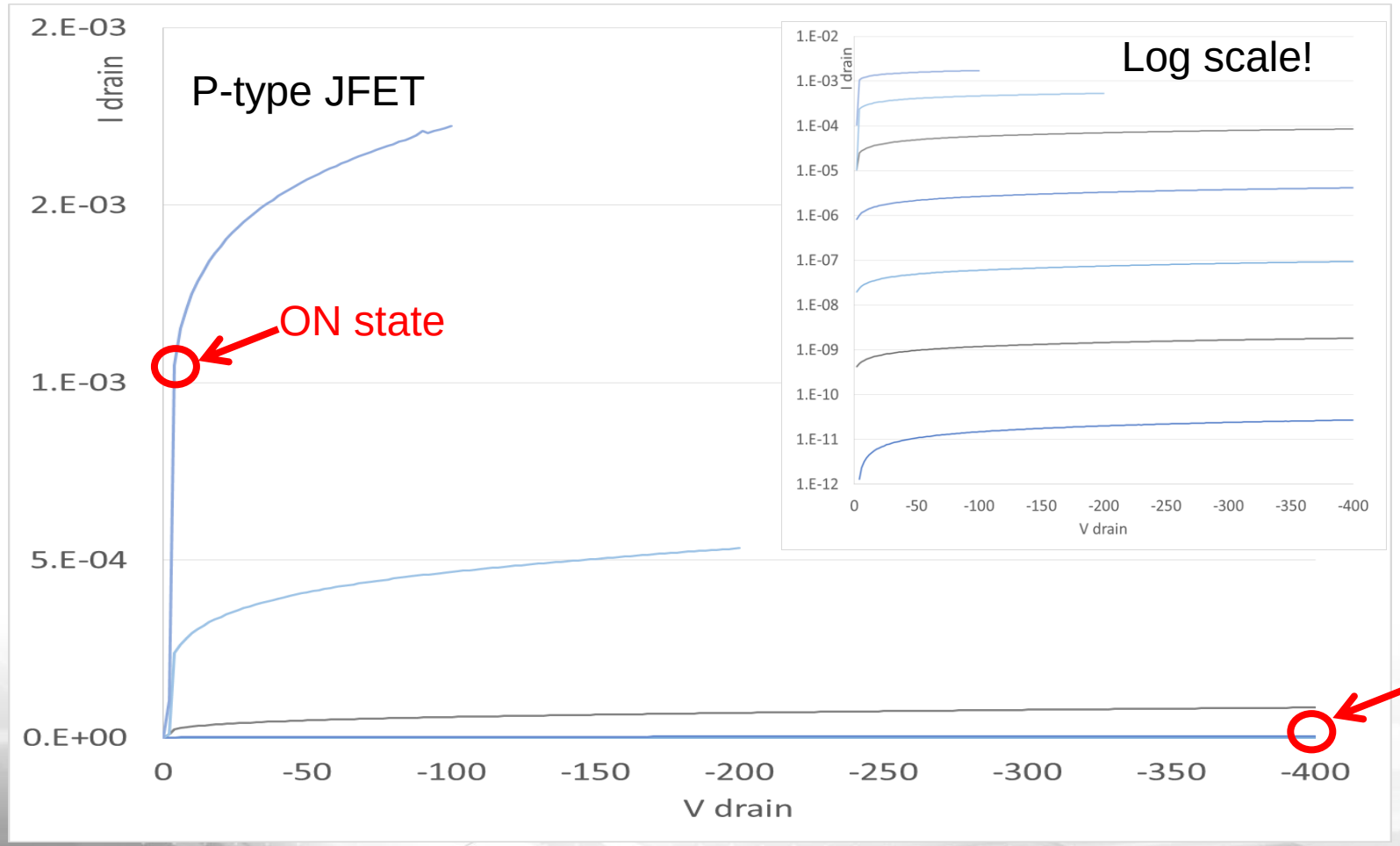


Process splittings in the dose of the channel, mainly to fight the horn effect.
Layout splittings in the width of the hole and in the length of the channel.

IV characterization

- Lower channel doses feature a closed channel already at V_{gate}=0 V (out of 4 wafers, 2 are OK).
- Higher Channel doses have lower V_{BD}.

N-type HV JFETs have V_{BD} at 600V or 400V (for a channel dose of 6 and 8e12 cm^{-2}, respectively)
P-type HV JFETs have V_{BD} at 400V or 250V (for a channel dose of 5 and 7e12 cm^{-2}, respectively)



Only hole width = 5μm works.
Larger hole width leads to early breakdown.

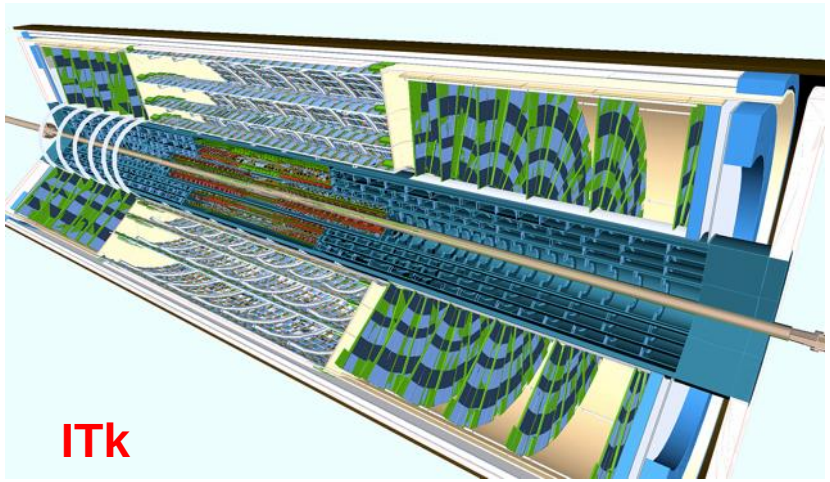
OK as switch for un-irradiated sensors.
To be irradiated and re-checked.

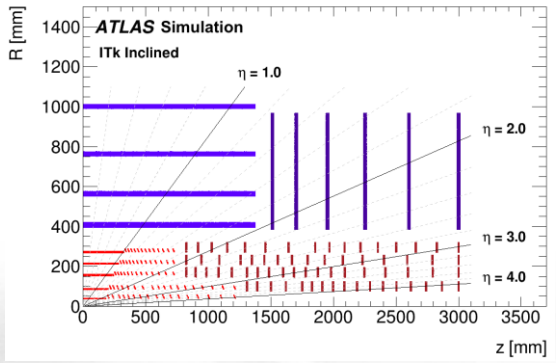
Other on-going activities at BNL

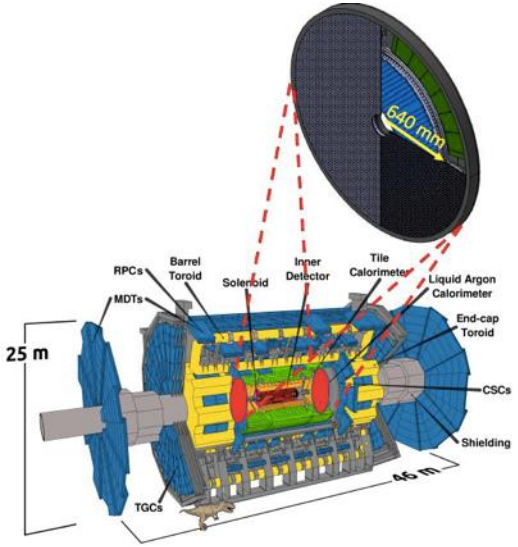
Silicon R&D: LGADs

Microstrip for the Inner Tracker (ITk)

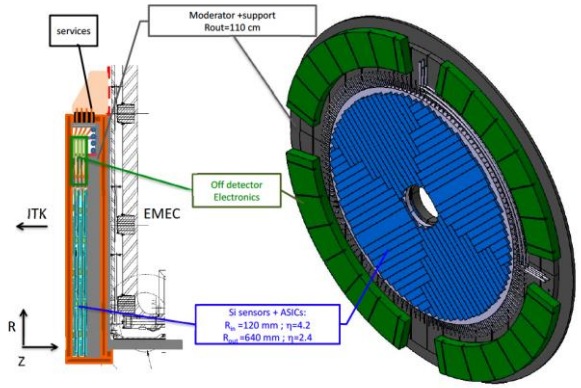
and High Granularity Timing Detector (HGTD) of ATLAS







|η|>2.4 (R=640mm)
|η|<4.0 (R=120mm)
z=3500 mm
Δz = 7.5 cm



HGTD

We are involved in testing LGADs from HPK and CNM, through TCT, CSA, fast current amplifier (SCIPP), and dedicated ALTIROC ASIC for the ATLAS HGTD.

2- LGAD R&D

We use the same epitaxial wafers of the HV-JFET:
(100), N_A=1e14cm^{-3}, 50μm thick

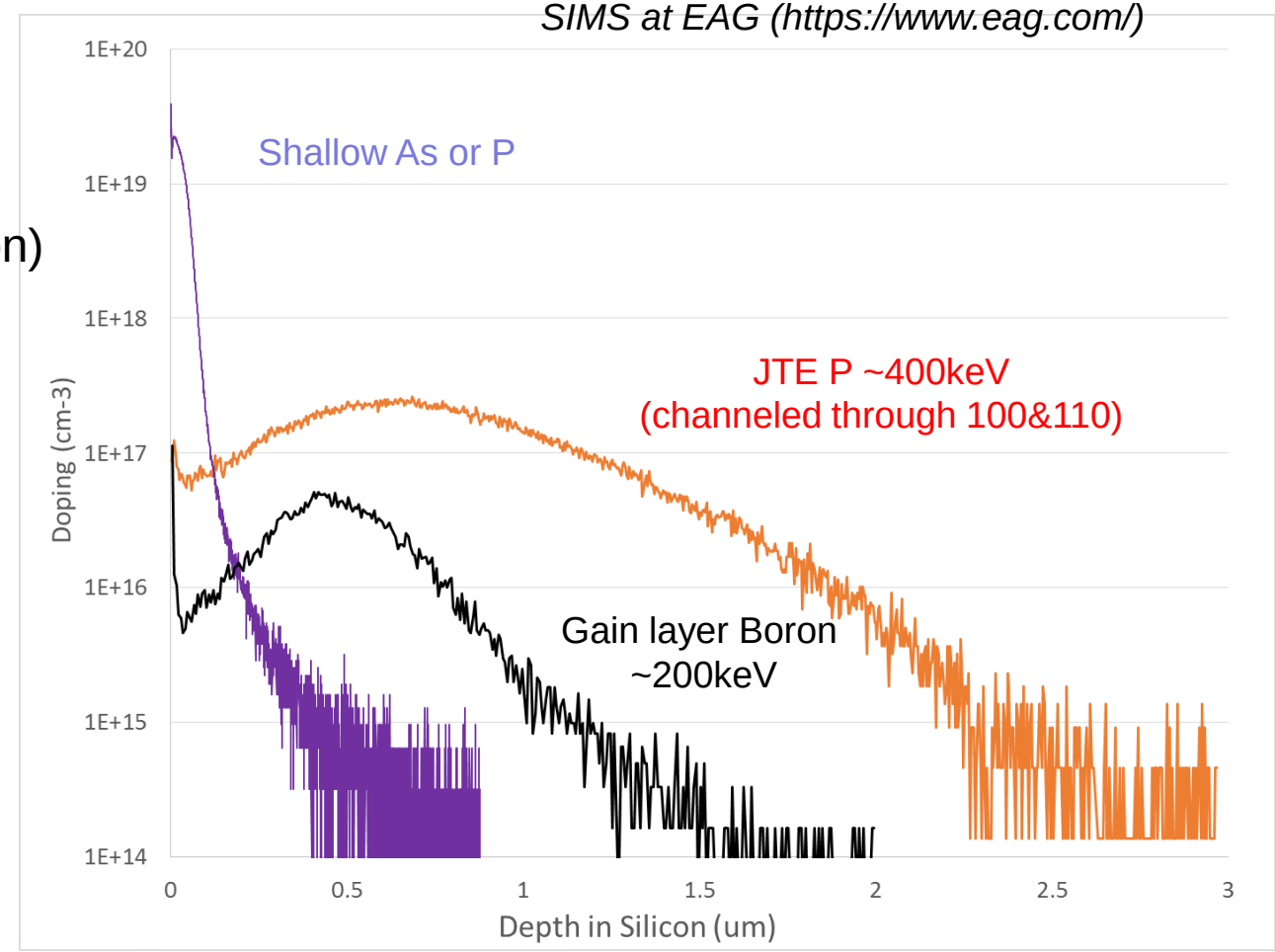
P-spray isolation (patterned to avoid implant on gain region)

Little thermal drive-in (mainly for the JTE)

JTE layer as deep as possible (~400keV)
Gain layer as deep as possible, within the JTE (~300keV)
N+ as shallow as possible
(to avoid compensation of gain layer)

Plan to do LGAD for photon science.

SIMS at EAG (https://www.eag.com/)

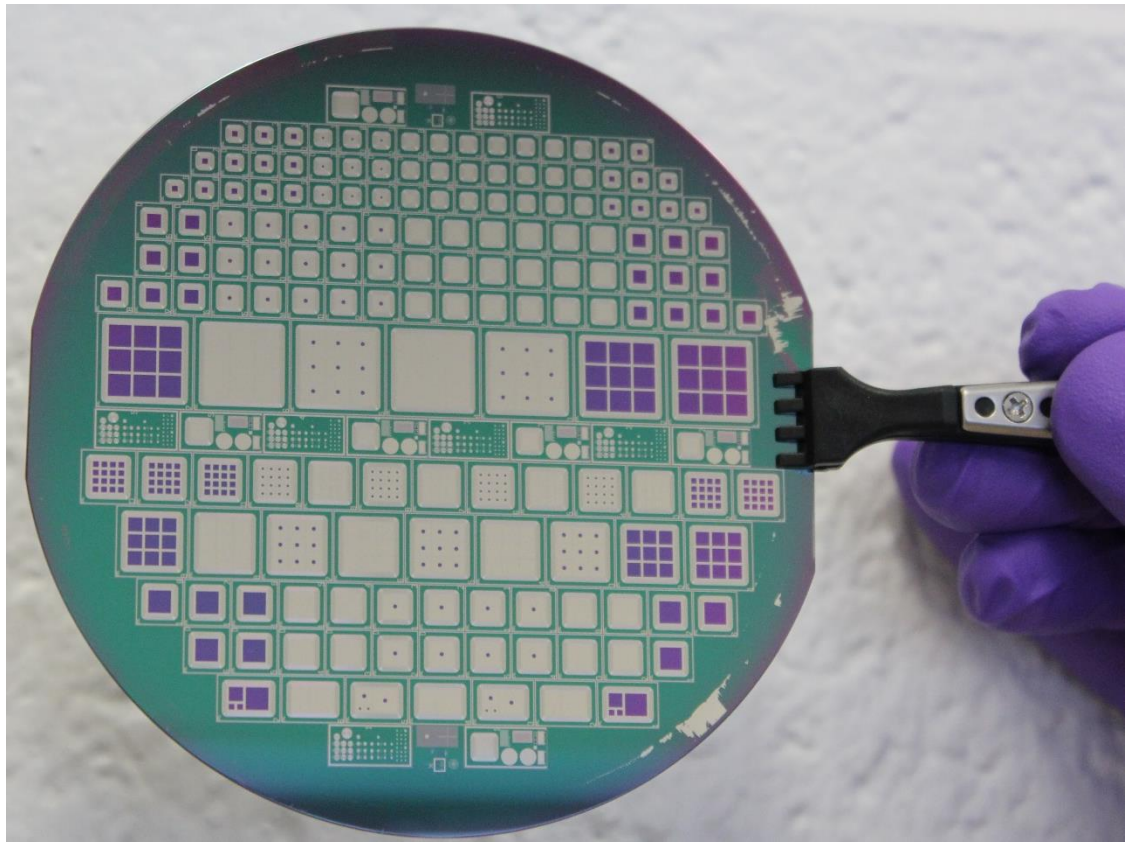


2- LGAD R&D

4” layout with 1x1 mm^2, 2x2 mm^2, 3x3 mm^2 and arrays.

First fabrication shows low leakage currents (< 1nA/cm^2), high breakdown voltage but no gain, so need to tune the doping profiles.

New run expected to complete on June 2018.



3- Commissioning of BLIP as a new irradiation facility for silicon R&D

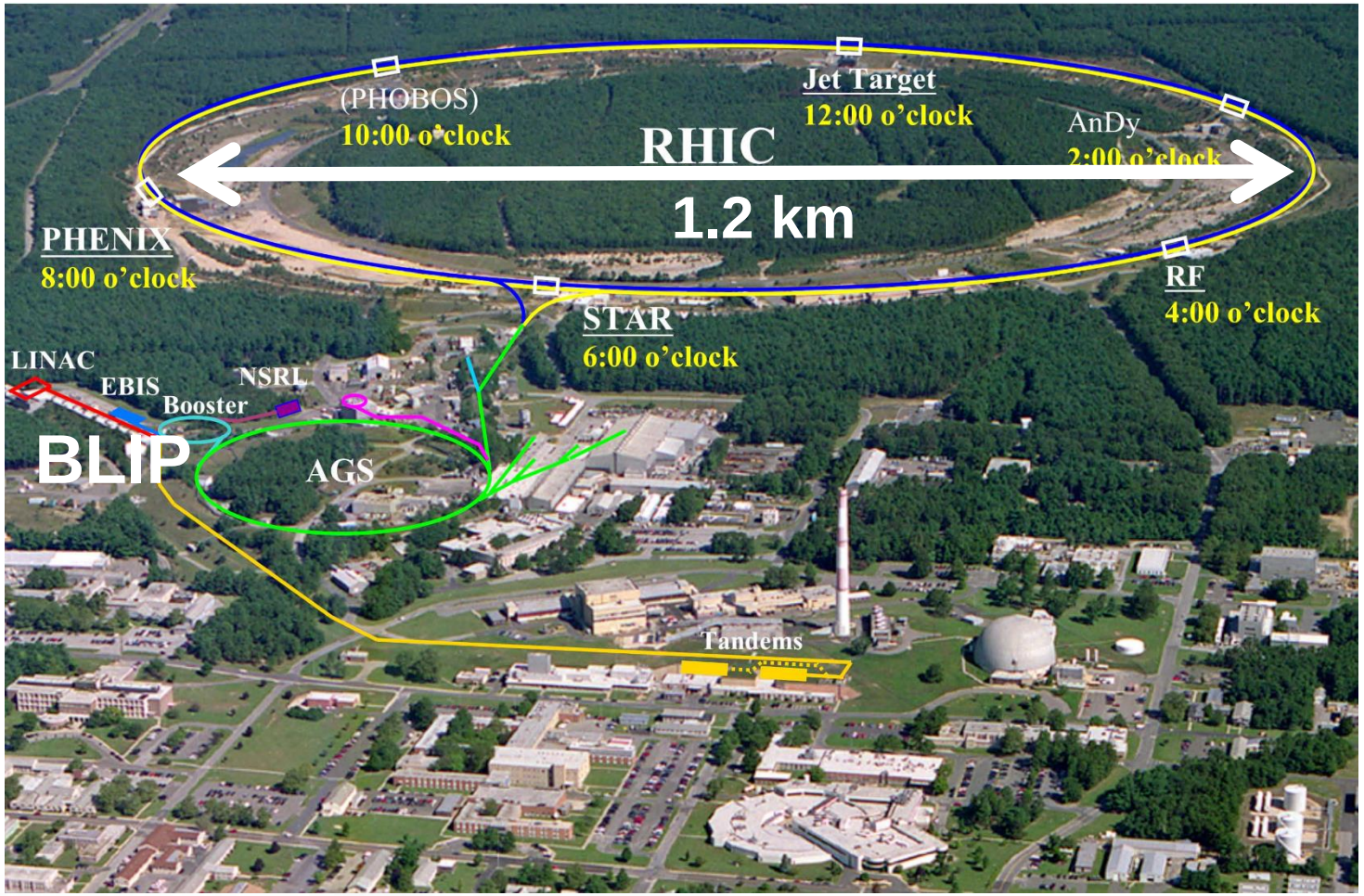
In coll. with James Kierstead, Nicolaos Simos *(BNL),*
Keith Baker, Christian Weber *(Yale University)*

The Brookhaven Linac Isotope Producer (BLIP) consists of a beam line and target area for isotope production.

It uses protons up to 200 MeV and up to 110 μA from the BNL Linac.

BLIP generally operates parasitically with the BNL nuclear physics program at the Relativistic Heavy Ion Collider (RHIC).

It produces certain commercially unavailable radioisotopes to distribute to the nuclear medicine community and industry (research to develop new radioisotopes desired by nuclear medicine investigators).



https://www.bnl.gov/cad/accelerator/

3. Commissioning of BLIP

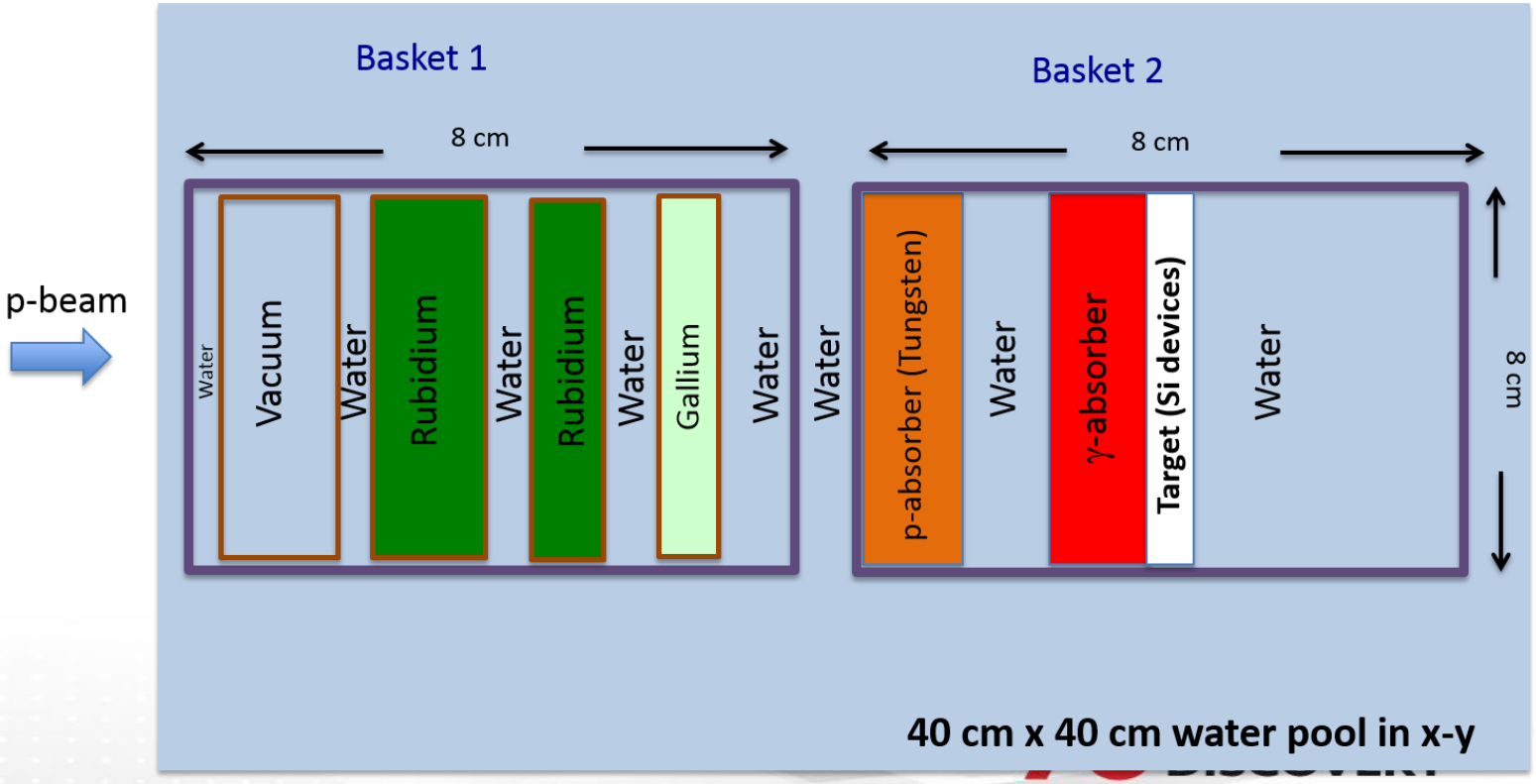
BLIP would be ideal for Si sensor irrad. as it can provide

- Both protons and neutrons
- Adjustable proton energies (65 MeV to 200 MeV) and currents (few μA to 110 μA)
- Low cost
- Proximity to BNL Physics Dept.

We already received interest in BLIP from several collaborators

The samples are loaded down into a 9m deep well, water cooled. Two baskets along the beam:

- first (upstream) for proton irradiation,
- second (downstream) for spallation neutron irradiation. Runs parasitically to proton irradiation. Protons are absorbed in first basket and in additional absorber in II basket. Gamma absorbed in II basket too. Neutron Fluence is ~1e15 1-MeV $n_{eq}/cm^2/hr$.
- proton contamination during neutron irradiation of 1-10 Mrad/hr and negligible EM contamination (FLUKA simulations).



Conclusions

- Custom fabrication of not-standard devices
  → HV-JFET successful (still irradiation campaign to do)

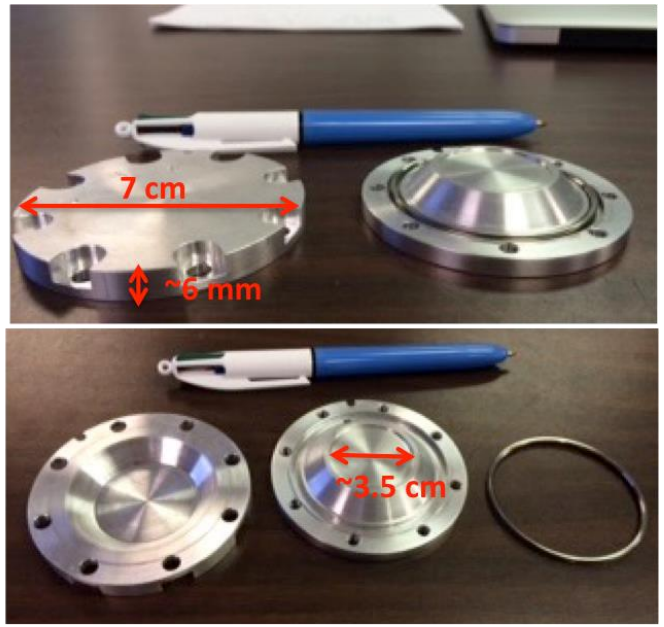
- LGAD development, fabrication and testing

- Plans to have an irradiation facility in house

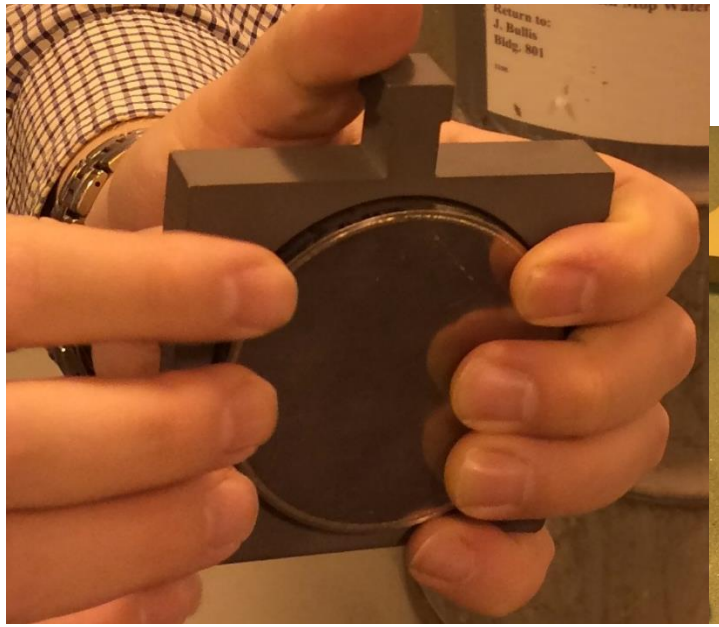
Post-doc position open at BNL:
https://inspirehep.net/record/1672347

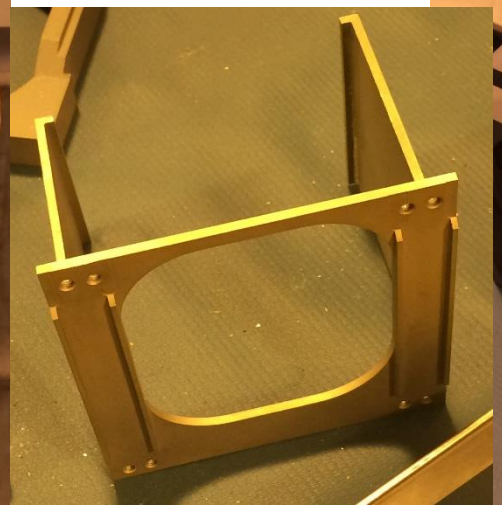
Back up

Sensors are held in between two aluminum plates

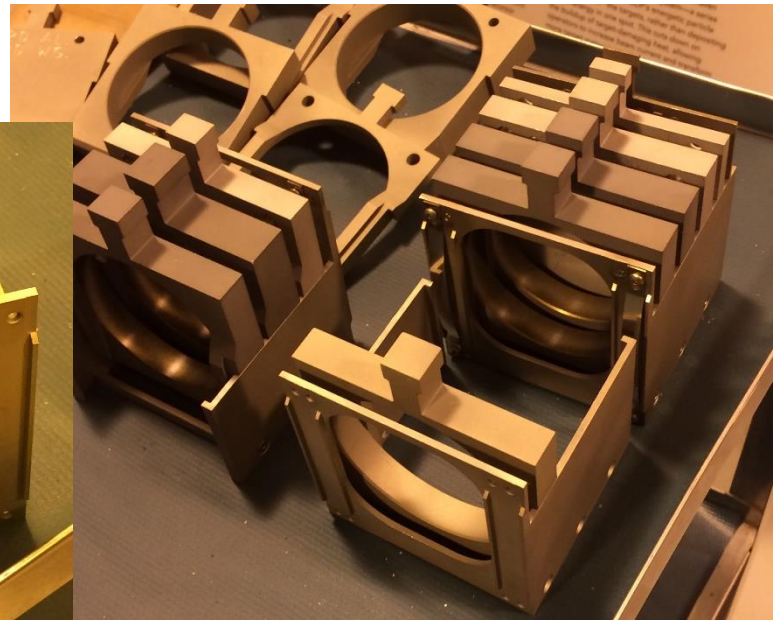


The plates in a holder





A few plates fill up a tray



The tray goes in a box, which is lowered at the irradiation point