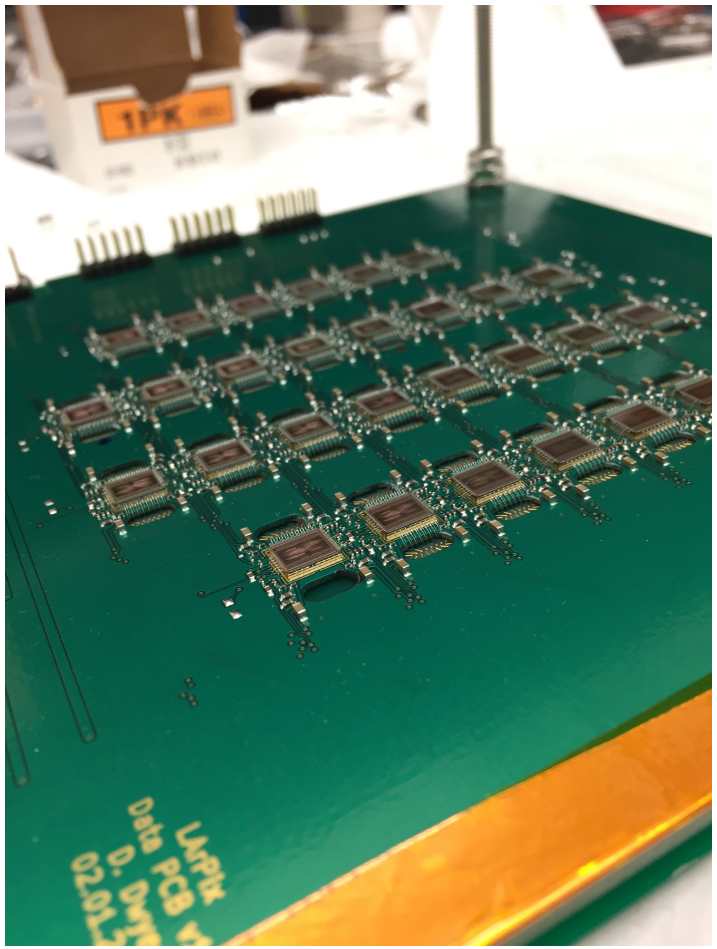
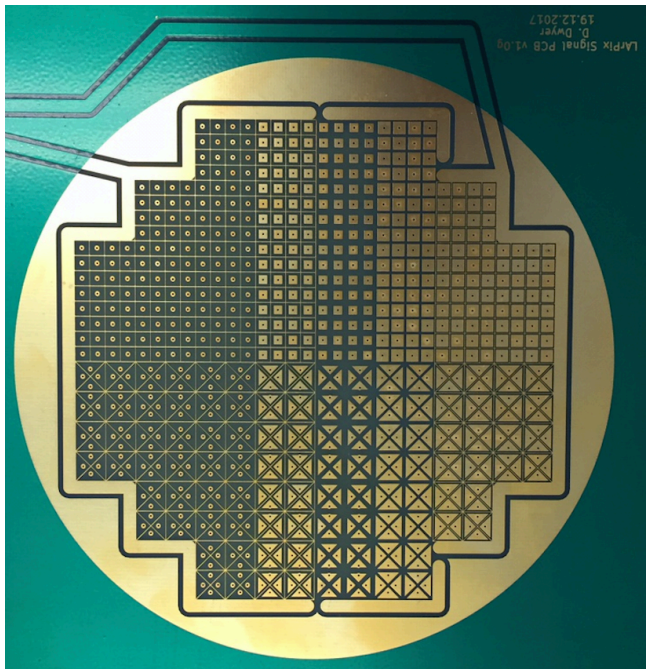
LArPix Readout: Status and Plans

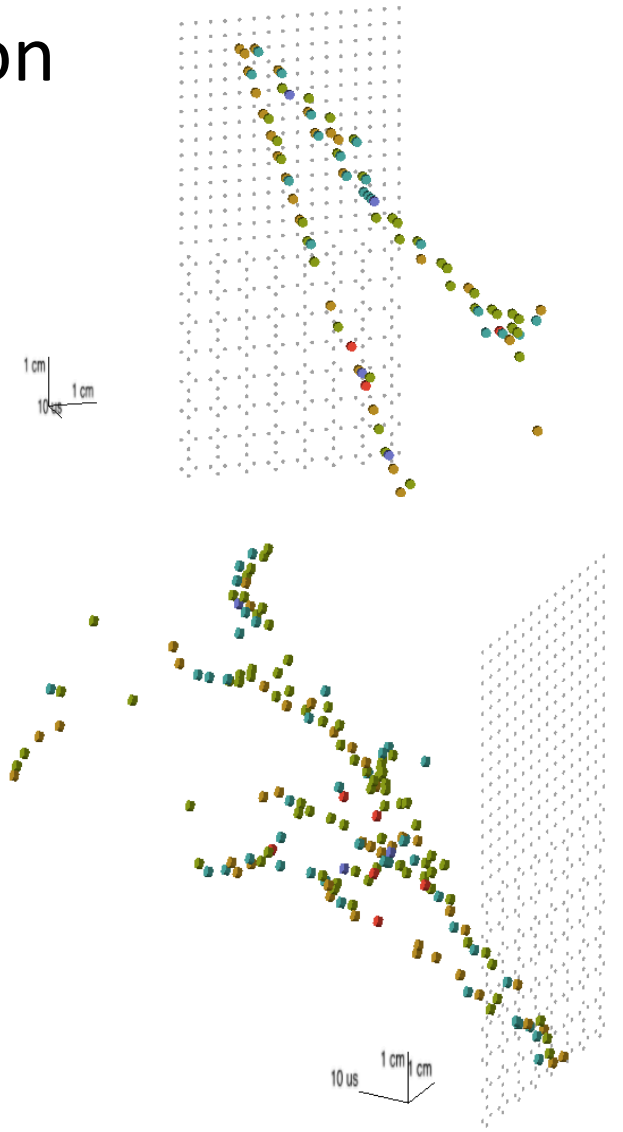
Dan Dwyer (LBNL)

ArgonCube Collaboration Meeting

June 12, 2018

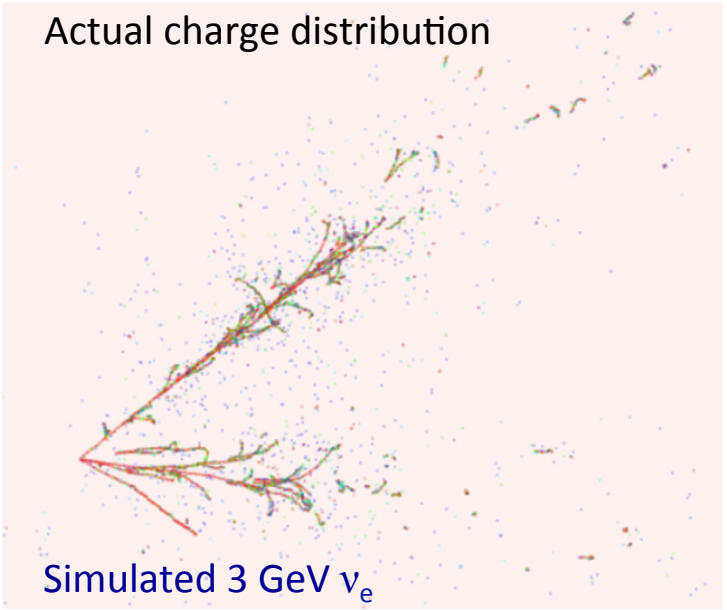


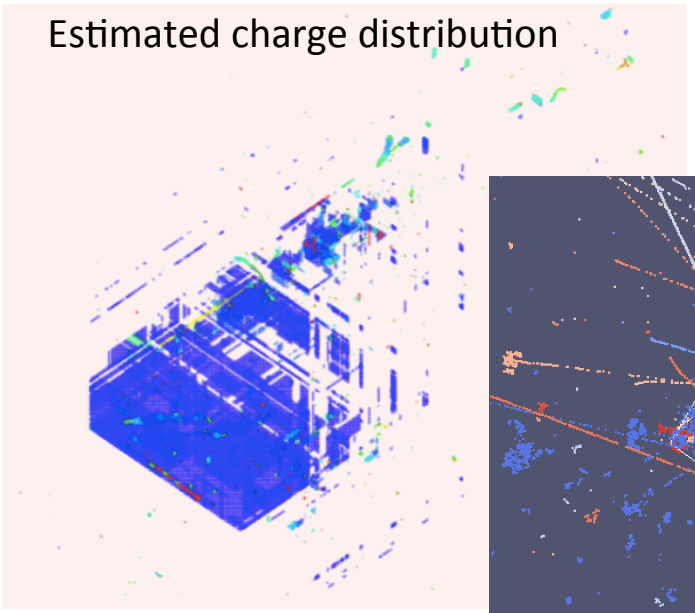




3D LArTPC

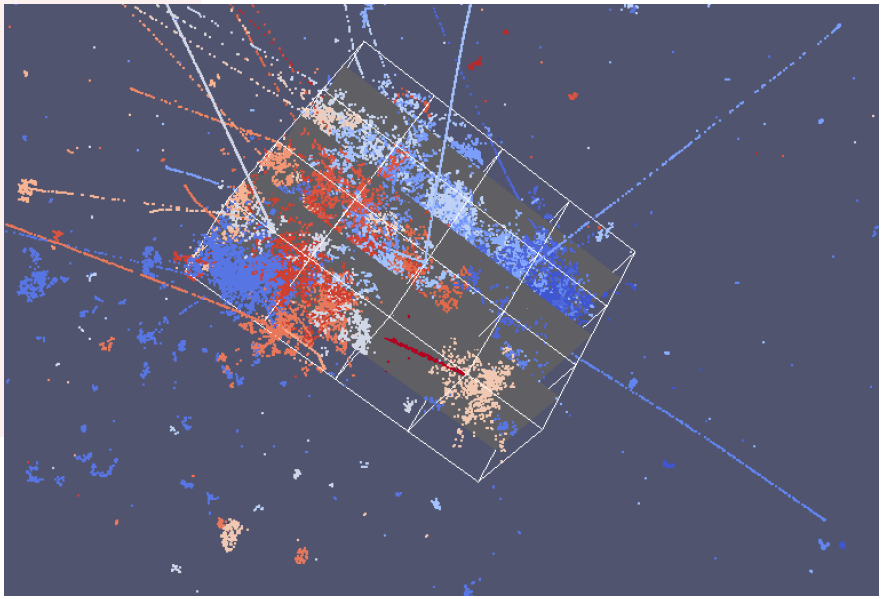
Ambiguities in projective wire readout:





DUNE Near LArTPC:

High neutrino rate exacerbates ambiguities.



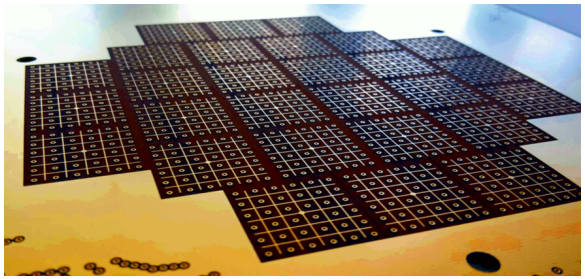
Example neutrino signals from one LBNF spill

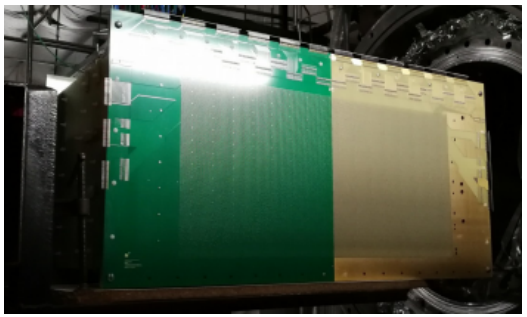
Pixel Readout Development

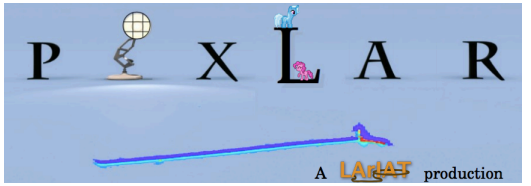
Demonstration of pixel sensor feasibility (Bern/ArgonCube)

Progress with in-beam tests (PixLAr)

→ Low-power pixel electronics (LBNL)

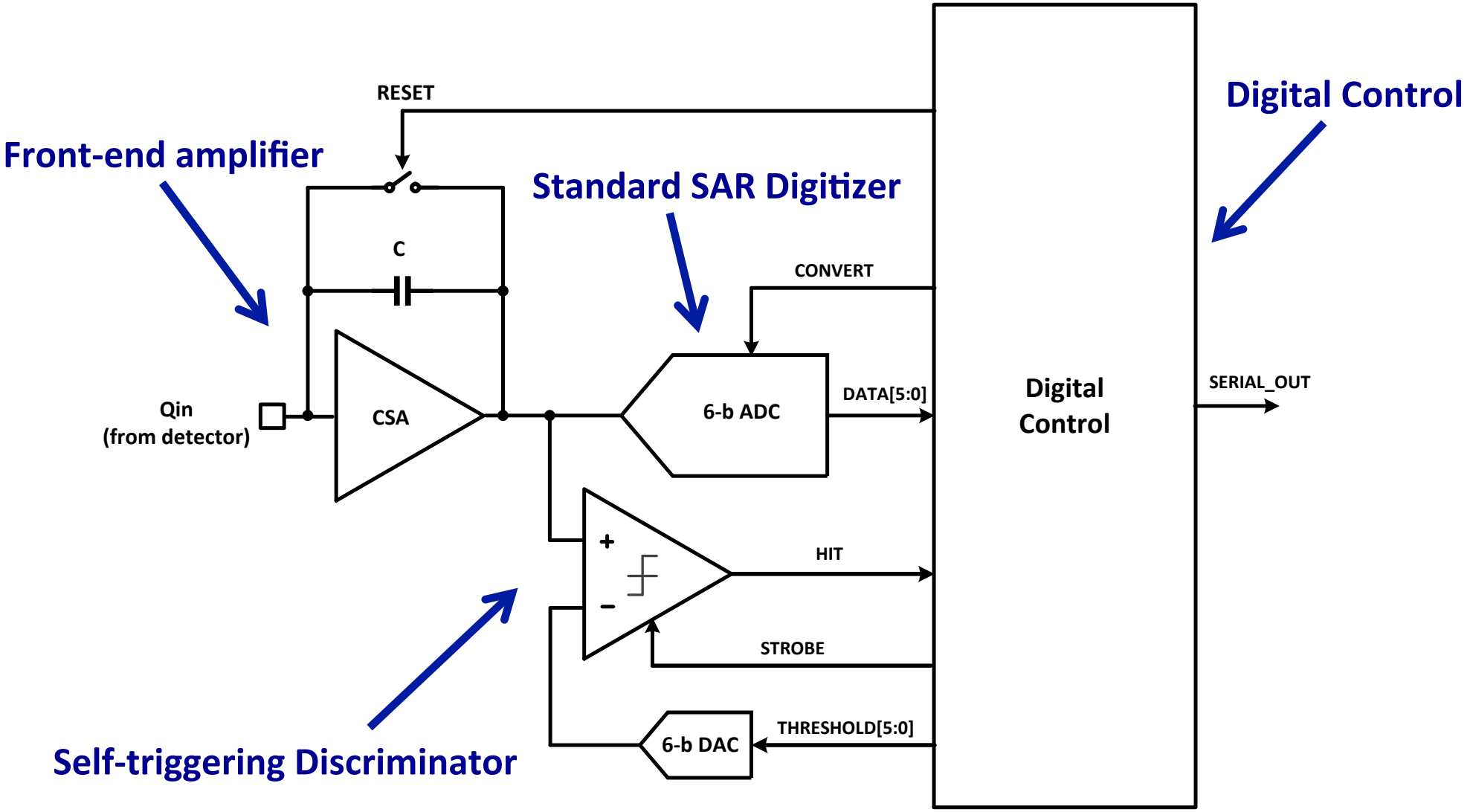






LArPix-v1 Design

Amplifier with Self-triggered Digitization and Readout



Achieve low power: avoid digitization and readout of mostly quiescent data.

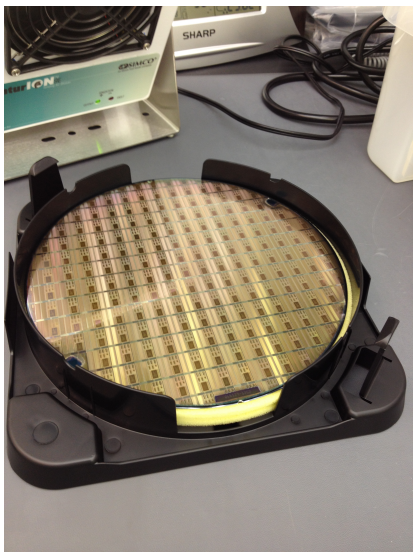
LArPix-v1 Progress

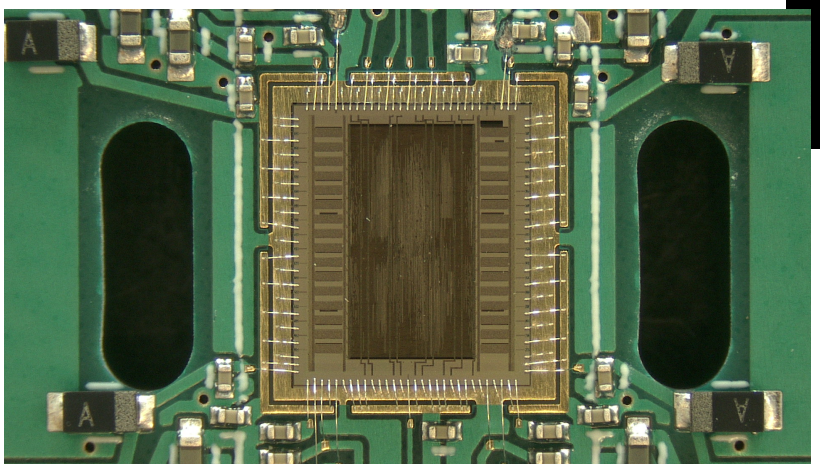
LArPix-v1 ASIC:

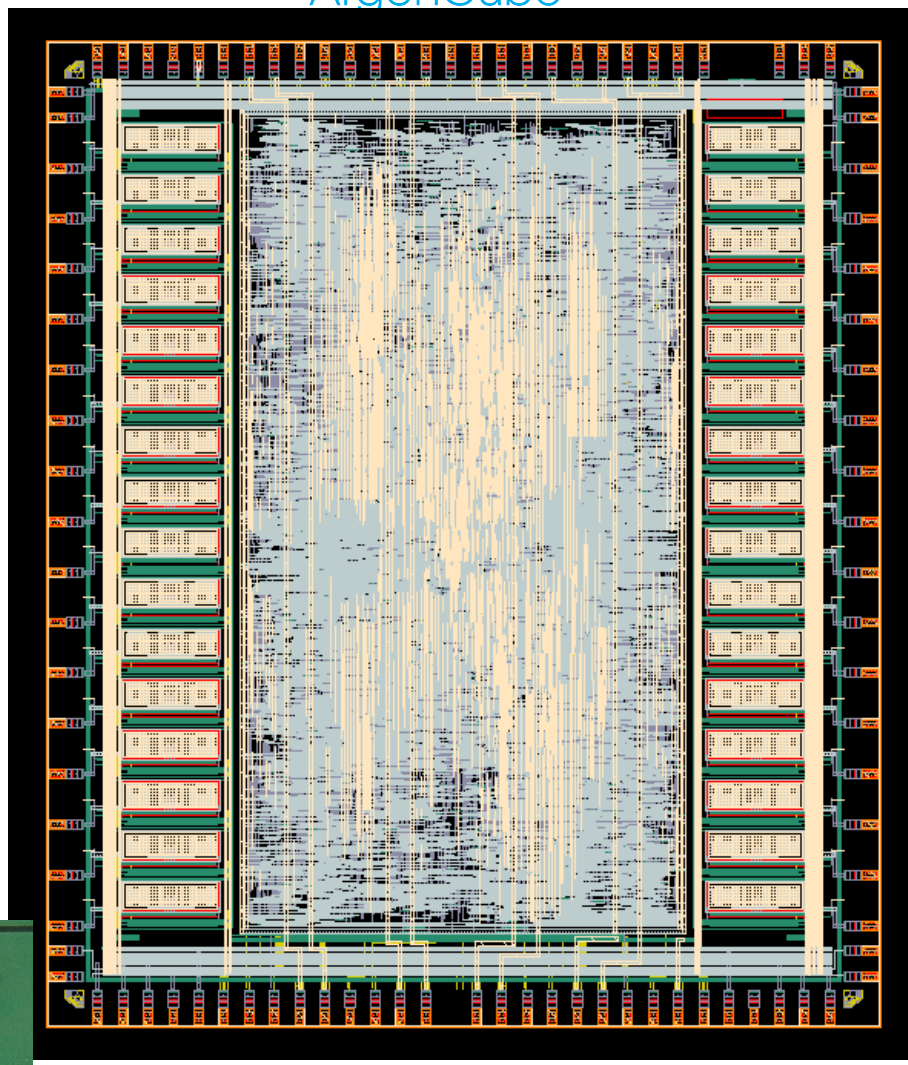
- Dec. 2016: Design began
- June 2017: Submitted for fabrication
- Oct. 2017: First chips, test boards @ LBNL
- Dec. 2017: Bench tests successfully completed
- Jan. 2018: Assembled sensor, integrated LArTPC

Progress since last collaboration meeting:

- Feb. 2018: First tracks from true 3D LArTPC @ LBNL
- Mar. 2018: Developed integrated control system
- Apr. 2018: Assembled scalable 512-channel system, operated in 60-cm-drift TPC @ Bern
- May 2018: Operated 832-channel system @ LBNL







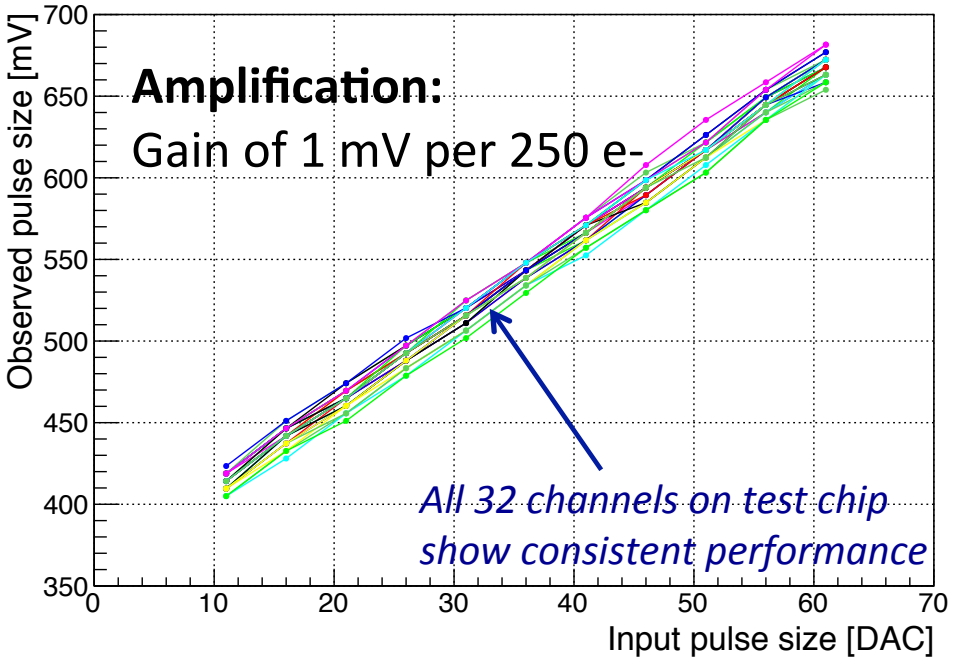
Process: 180nm bulk CMOS

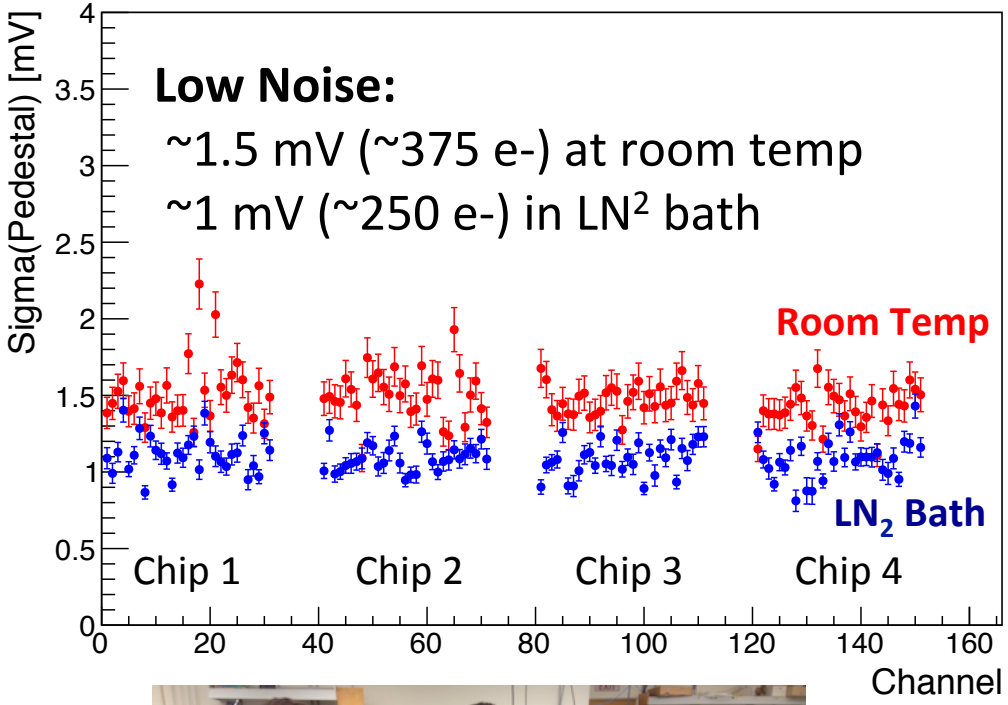
Design and testing team @ LBNL:

D. Dwyer, C. Grace, M. Garcia-Sciveres, A. Krieger, D. Gnani, T. Stezelberger, S. Kohn, P. Madigan, H. Steiner

Gain, Noise, Power

Demonstrated low-noise low-power cryogenic amplification, digitization, and readout:



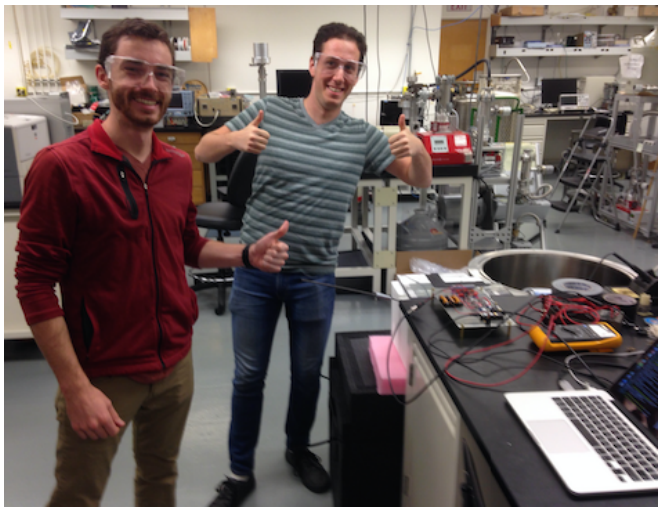


Low Power:

Average power for 128-channel readout:

- Analog: 24 µW/channel
- Digital: 38 µW/channel
- **Total: 62 µW/channel**

See talk from DUNE Collaboration Meeting (January 2018) for more details.



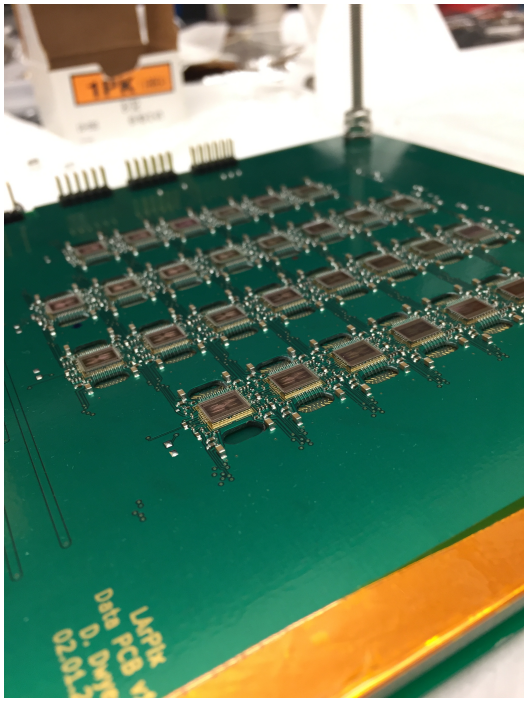
P. Madigan, S. Kohn: drove testing effort

Control System

Developed Prototype Control System:

- Warm electronics for LArPix sensor operation
- Provides power, reference voltages, clock, data I/O, and integrated DAQ system
- Main components:
  - Off-the-shelf Cmod FPGA module ($60): Provides real-time clock, I/O
  - Raspberry Pi Zero ($5): Complete DAQ system, control computer
- Requires: 5V power supply or battery, ~400 mA average current.
- Access via wifi

Pixel system



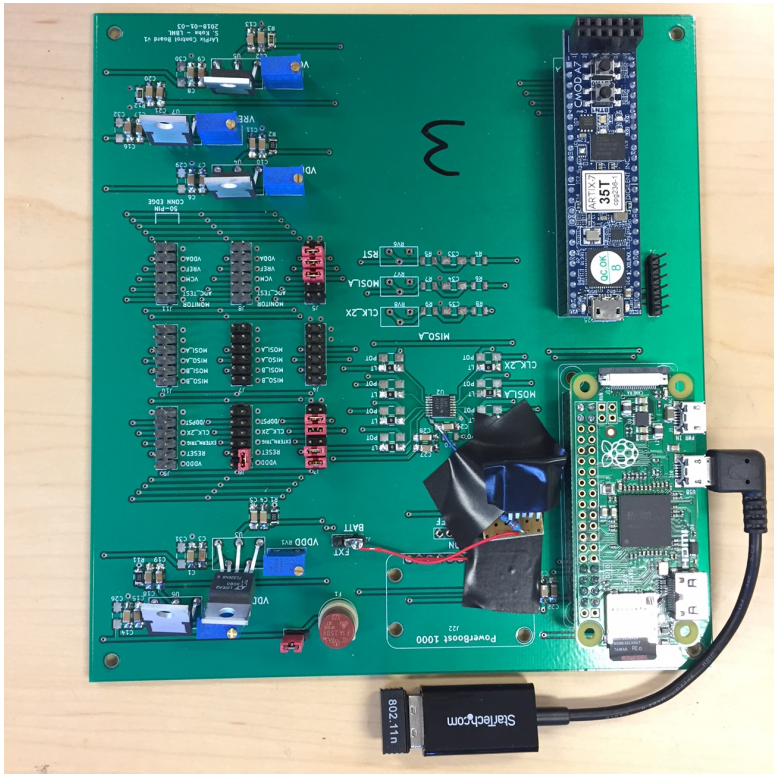
Inside Cryostat

50-pin ribbon cable

Existing layout should scale to ~8000 pixels.

With minor changes to FPGA firmware and PCBs, should support up to ~10^5 pixels.

Control System



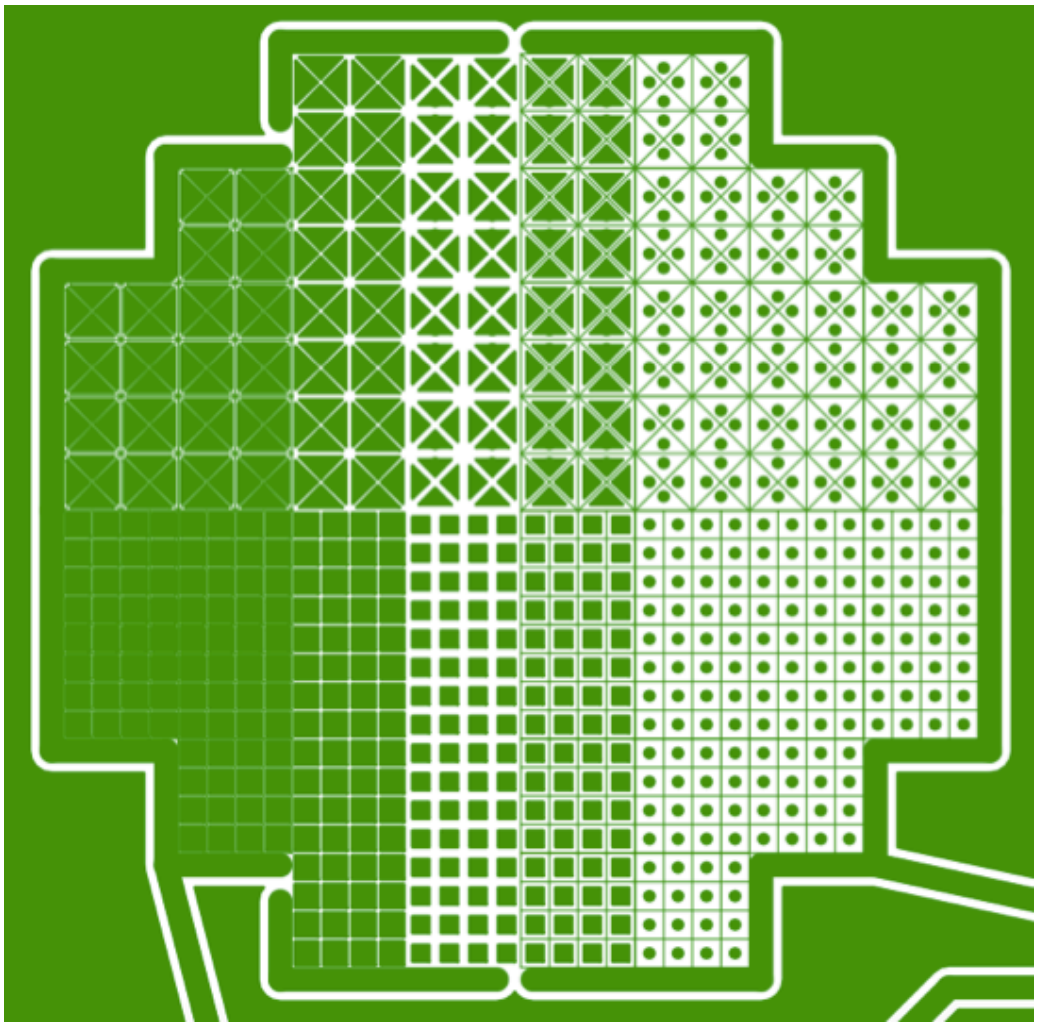
Outside Cryostat

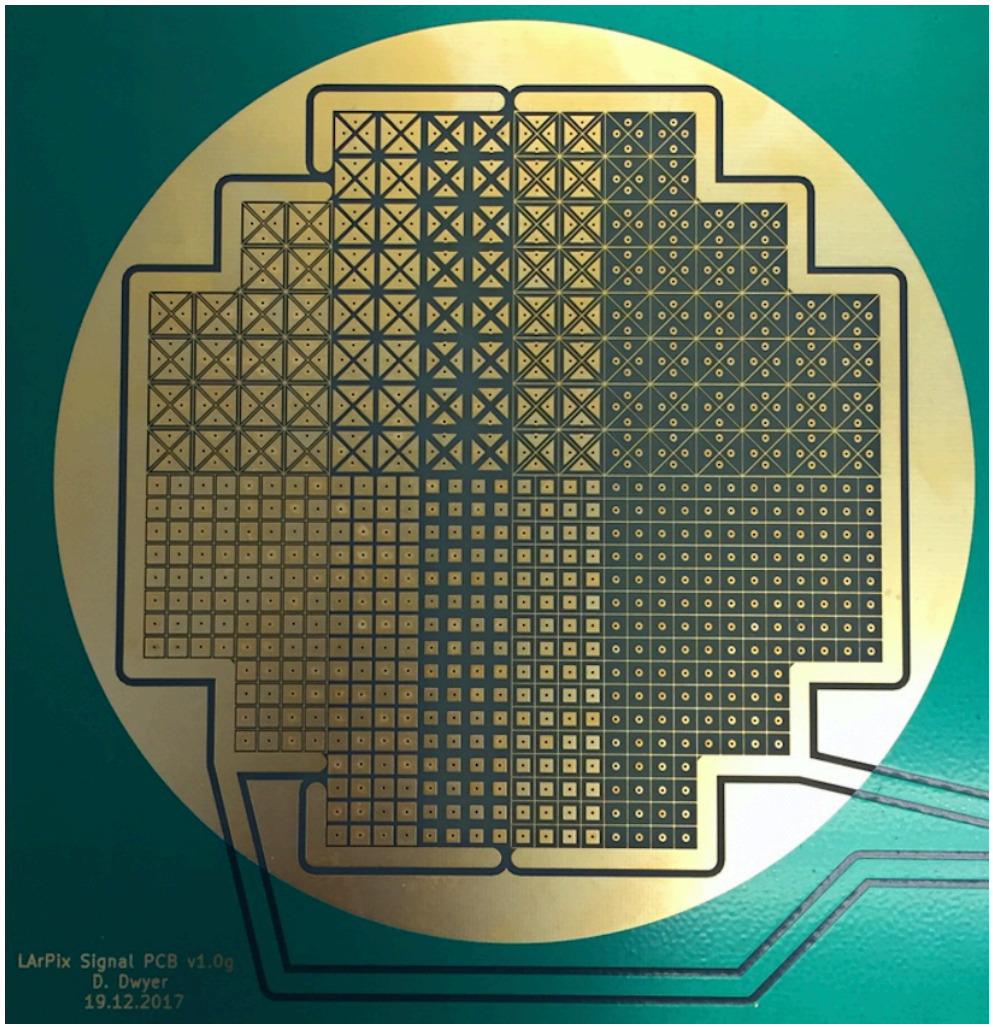
Pixel Prototypes

Prototyped a variety of pixel geometries

Sensor PCB board designed to fit Bern Pixel Demonstrator TPC

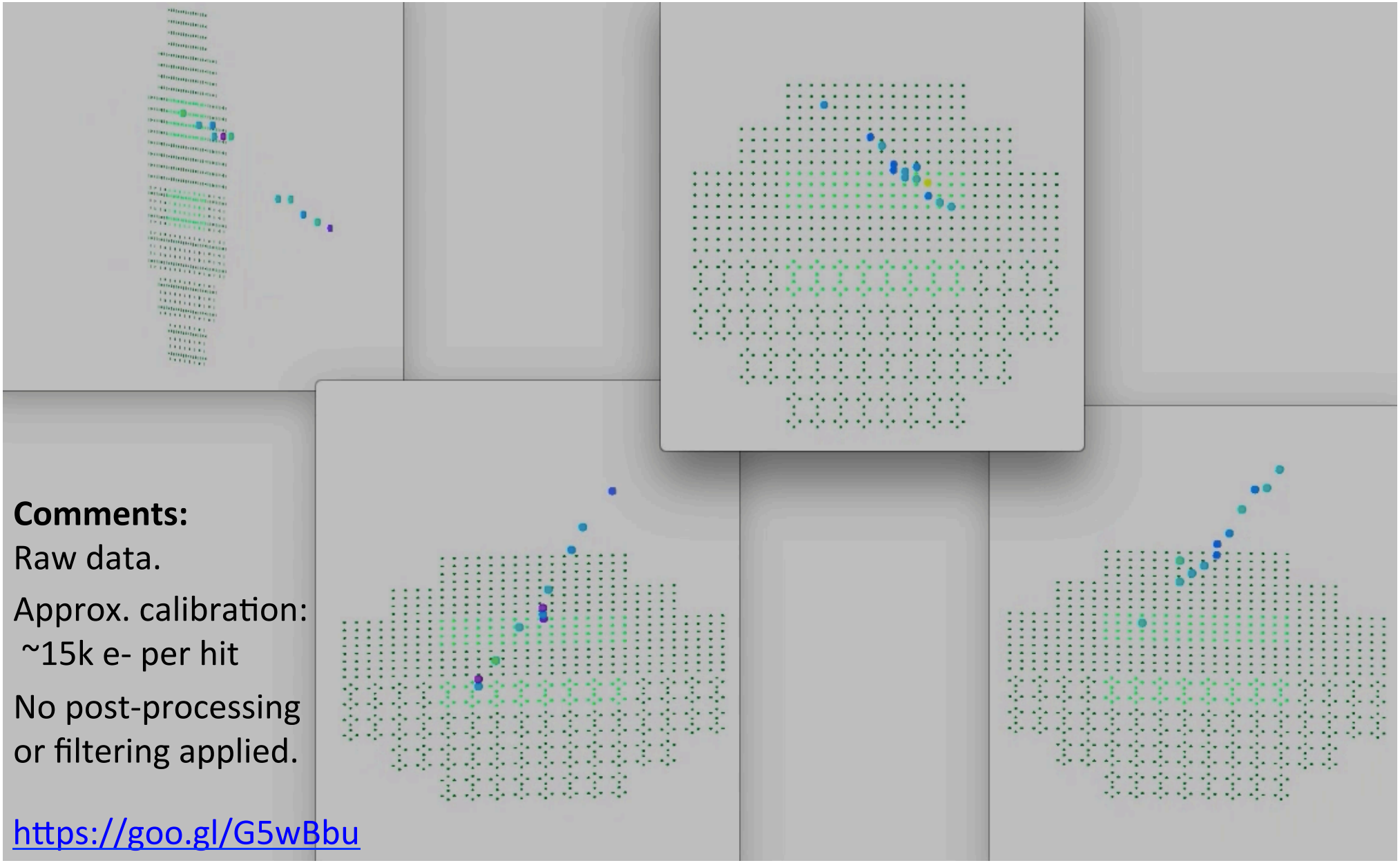
Includes 10 different pixel geometries/configurations





128-channel @ LBNL

Feb. 13, 2018: Detected first cosmic ray tracks



Comments:

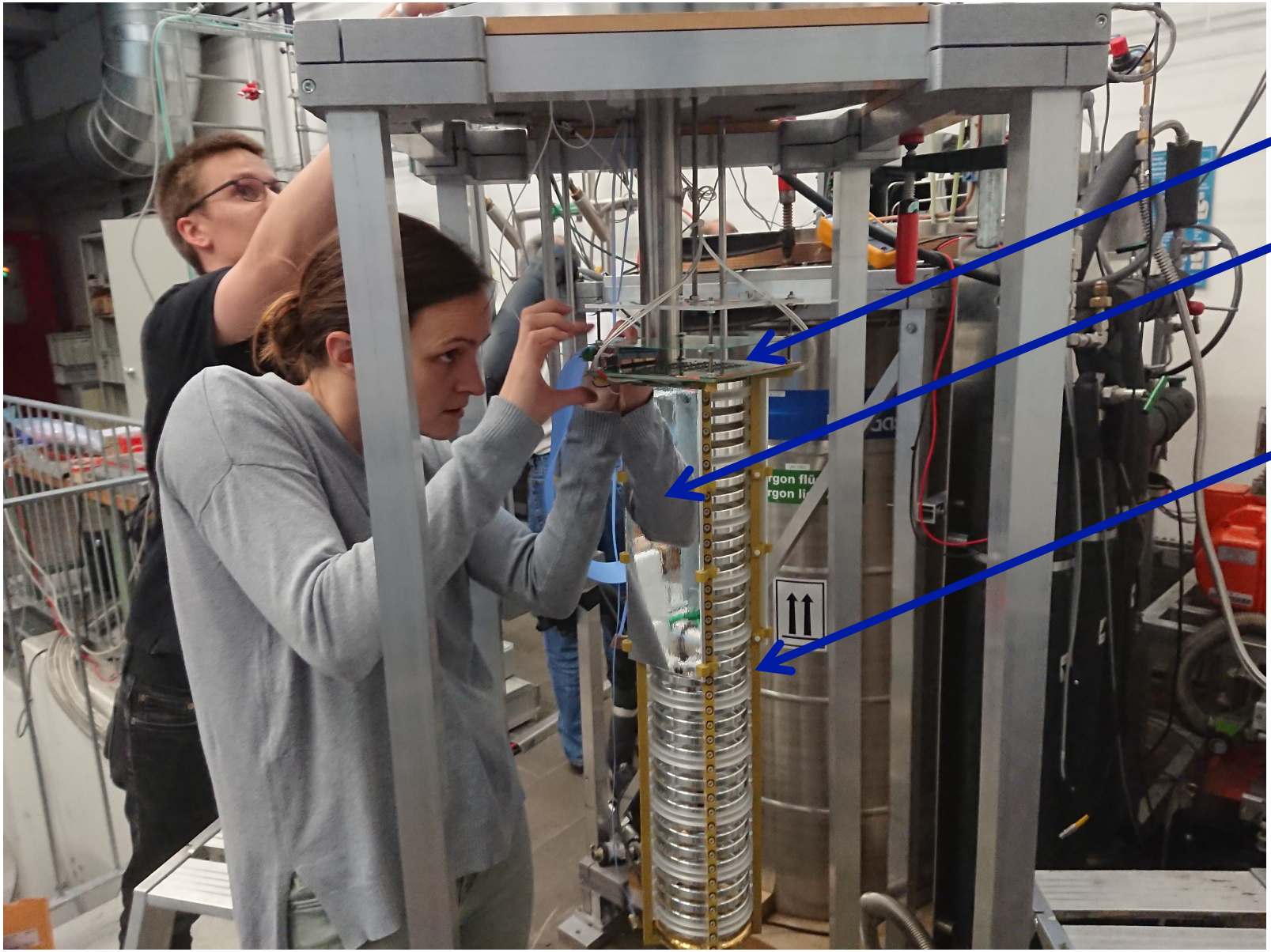
Raw data.

Approx. calibration:
~15k e- per hit

No post-processing or filtering applied.

https://goo.gl/G5wBbu

512-channel @ Bern



LArPix Readout

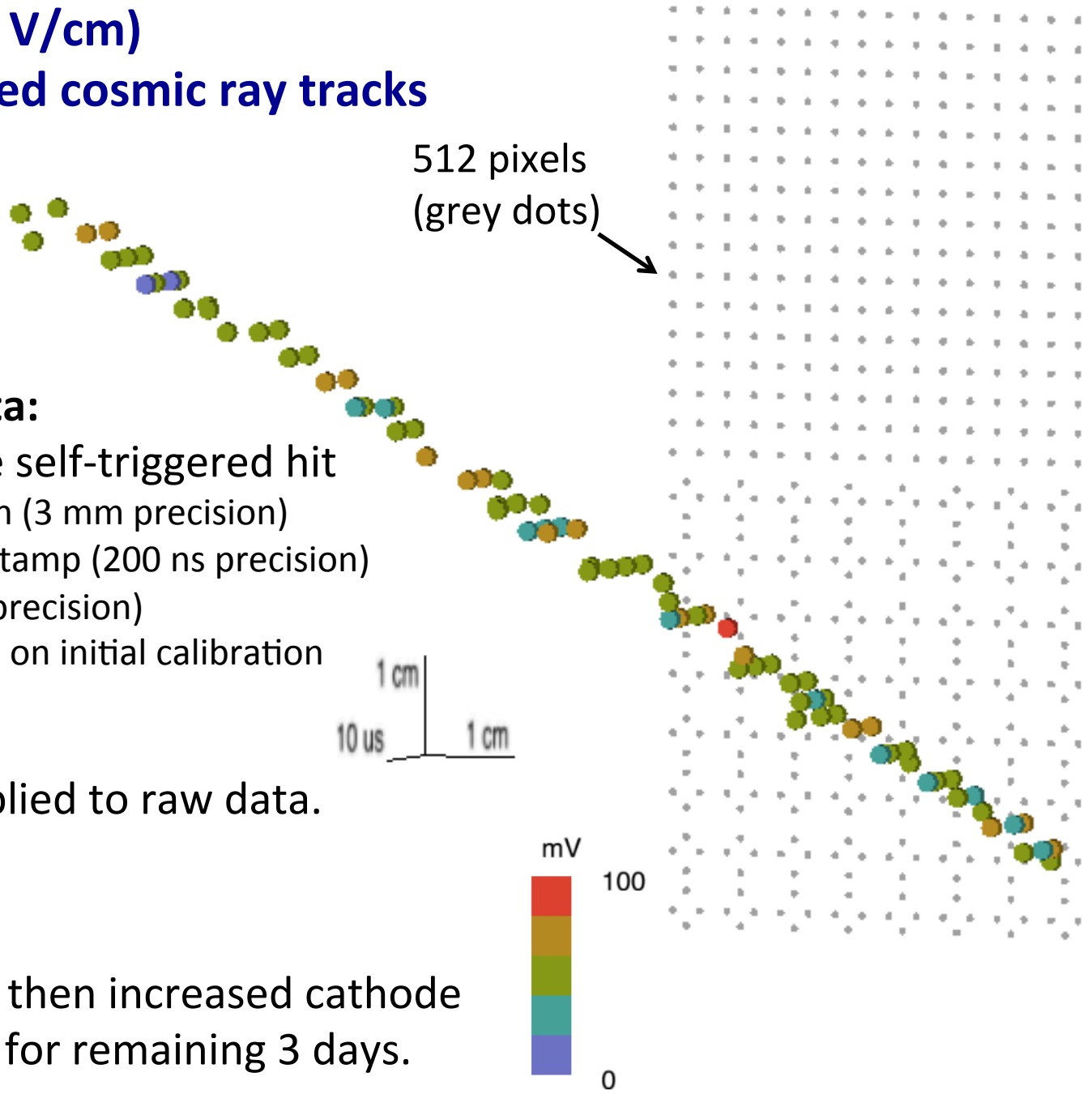
ArCLight System

ArgonCube Pixel Demonstrator (60-cm-drift TPC)

512-channel @ Bern

Raised HV to 31.5 kV (500 V/cm)

→ Immediately observed cosmic ray tracks



3D image from actual raw data:

Each colored point shows one self-triggered hit

- Hit x, y position from pixel location (3 mm precision)
- Position along drift given by timestamp (200 ns precision)
- Color shows hit amplitude (2 mV precision)
- ADC value converted to mV based on initial calibration

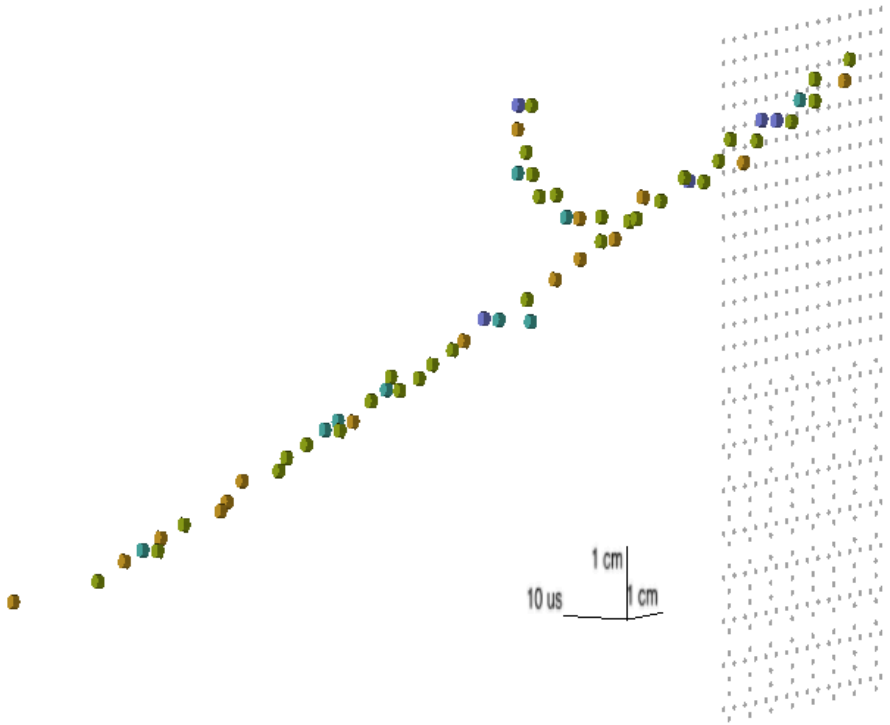
No filtering, manipulation applied to raw data.

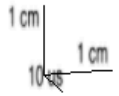
→ Noise is very low.

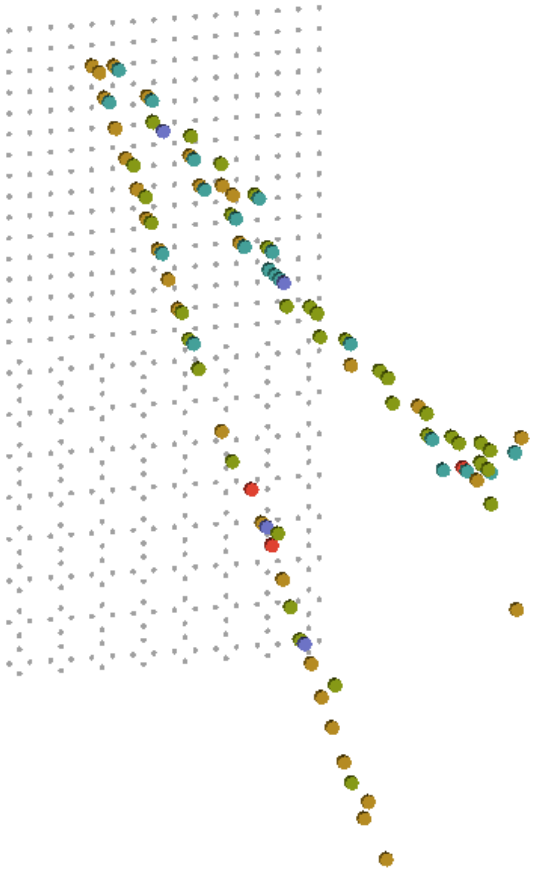
Operated 2 days at 500V/cm, then increased cathode voltage to 63 kV (1000 V/cm) for remaining 3 days.

512-channel @ Bern

Slightly more interesting topologies



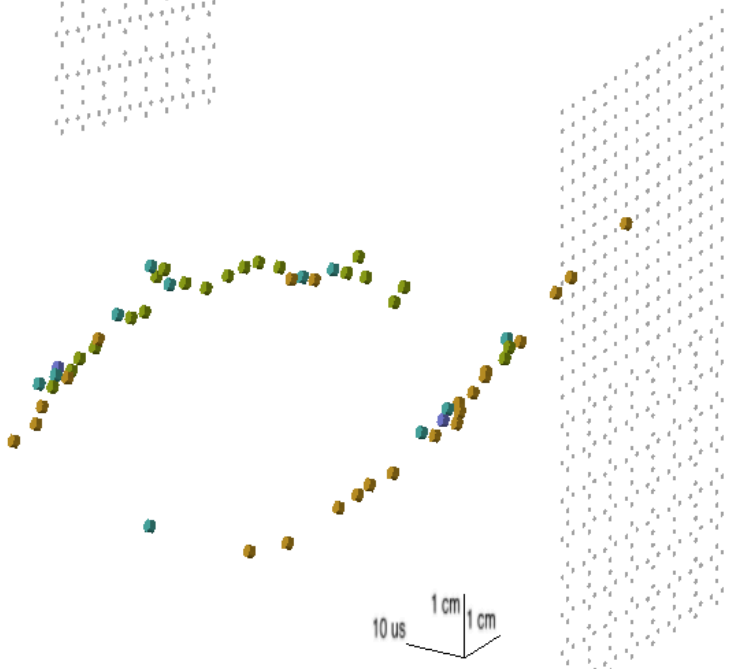




Straight MIP (at 45° to sensor):
35 ± 5 ADC (over pedestal)

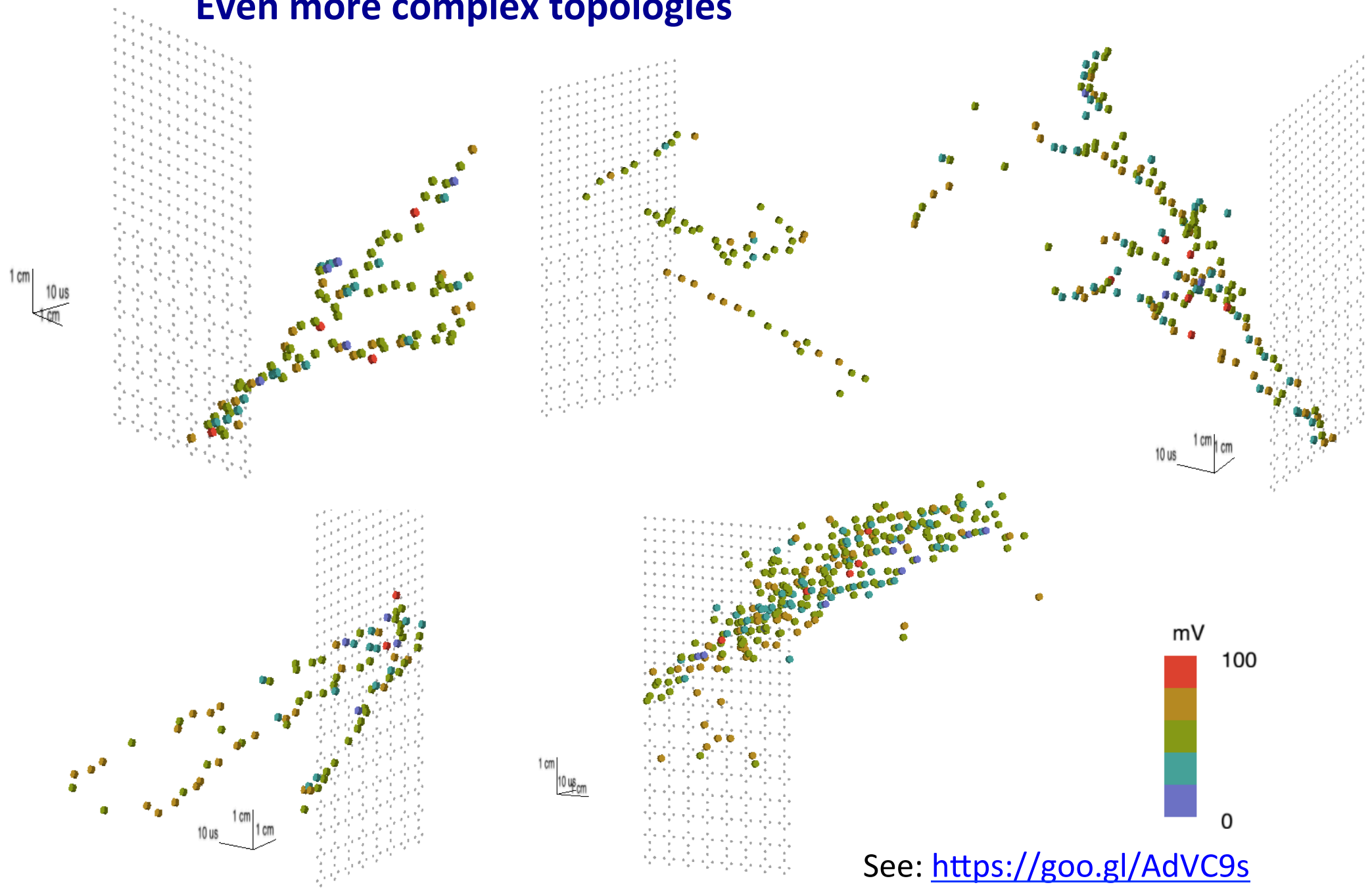
Noise:
2 ± 0.5 ADC

S/N Ratio:
17 ± 3 ADC



512-channel @ Bern

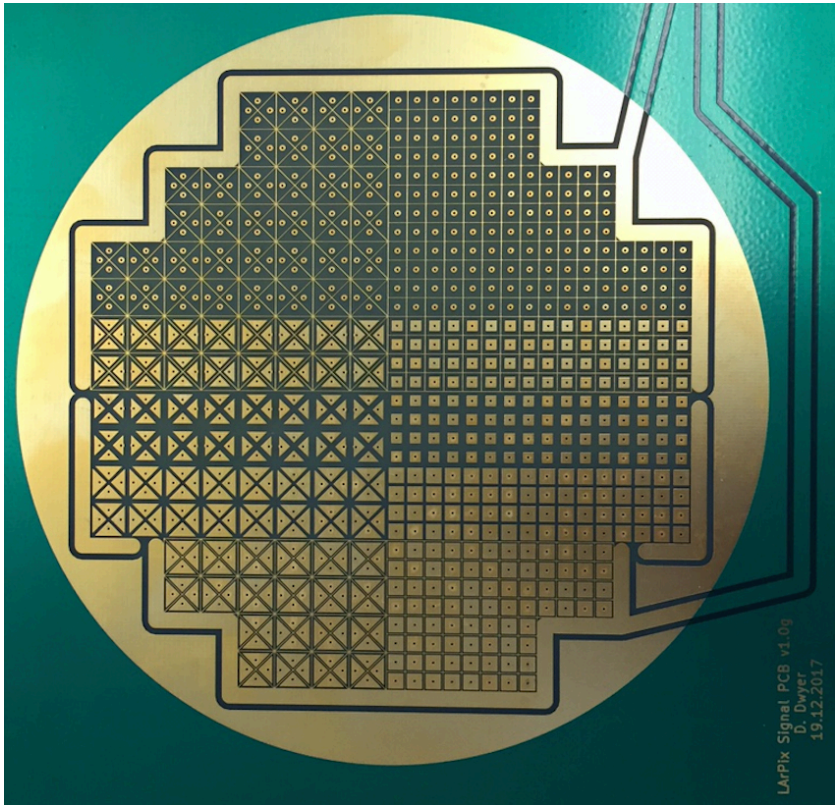
Even more complex topologies

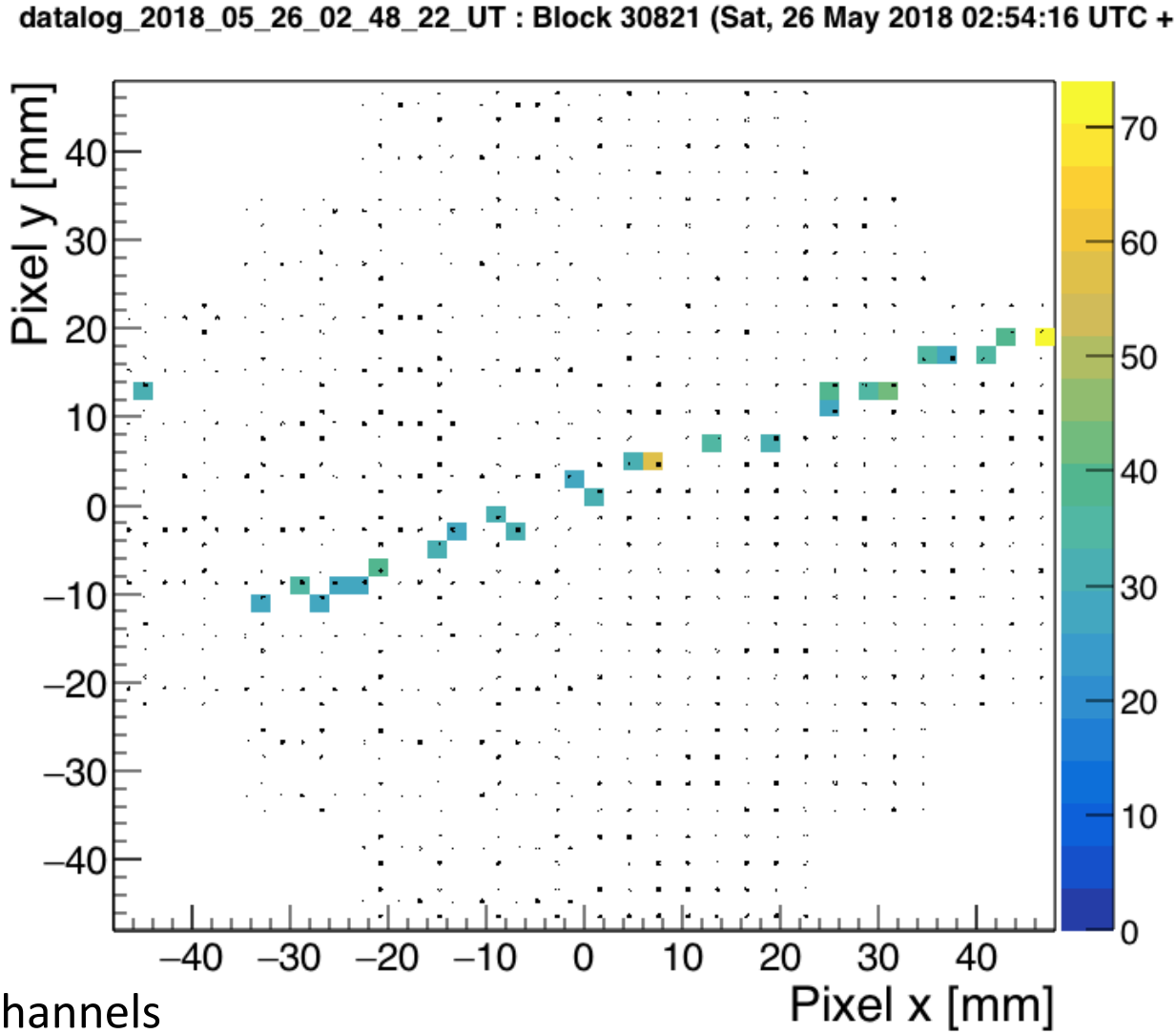


See: https://goo.gl/AdVC9s

832-channel @ LBNL

Completed full instrumentation of first-generation readout





May 21:
Began readout upgrade: 512 → 832 channels

May 25:
Completed testing in LArTPC @ LBNL

Initial conclusions: relative to test @ Bern
- System noise reduced by factor of ~4
- Poorer LAr purity → reduced data quality

Next Steps

Characterization of pixelated readout:

1) Establish calibration techniques
2) Comparison of performance of pixel types
   → Will determine the design for version 2 of Pixel Readout PCB
3) Assess performance of LArPix triggering and readout
   → Will motivate targets for LArPix version 2 ASIC design

See P. Madigan's talk

Near-term system revisions: targeting improved prototype system

1) v2 Readout PCB:
   - Improve isolation between pixel inputs and digital activity, and facilitate bypassing
   - Intermediate step toward modular readout tile
2) v2 Control Electronics (warm):
   - Work with LHEP to establish scalable (>10^6 pixel) control electronics
   - Stepping-stone to ArgonCube 2x2 control system
3) v2 Control Software:
   - Improve structure of high-level python configuration and control
   - Add flexible interface to low-level hardware communication with LArPix ASICs

See S. Kohn's and C. Tognina's talks

Mid-term system revisions: targeting LArIAT, ArgonCube 2x2 Demonstrator

1) v2 LArPix ASIC (see next slide)
2) v3 Readout PCB (see slide after next)

LArPix-v2

Exploring LArPix-v2 for full physics performance:

Simultaneously obtain high resolution and large dynamic range for charge signal

(with LArPix-v1 you can only choose one or the other at a given time)

Make daisy chain I/O robust to chip failure.

Improve hit timestamp: catch rollover and remove jitter.

Reduce input pad voltage requirements.

Improve default configuration settings.

Improve handling of chip ID.

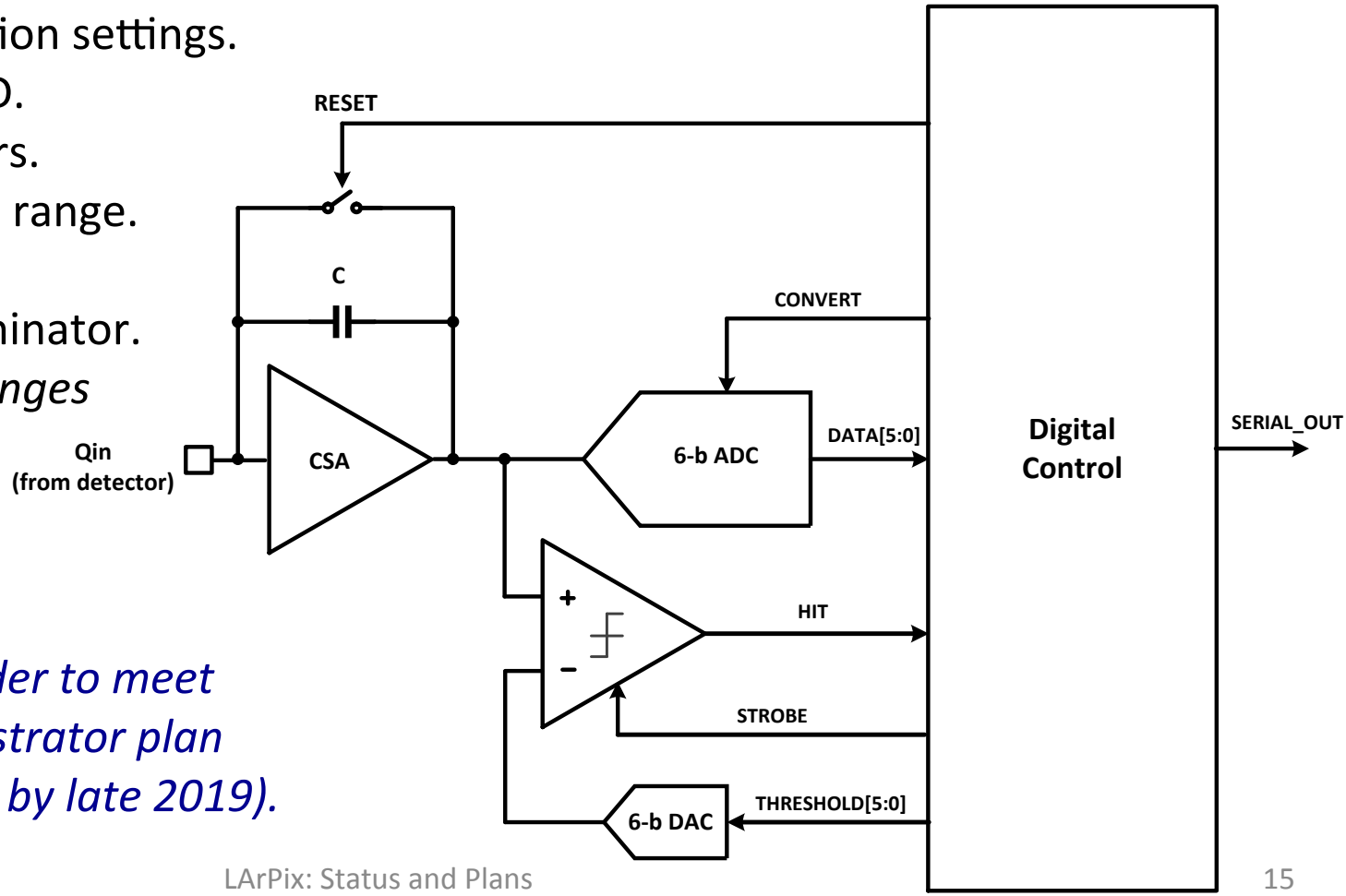
Add internal bias generators.

Increase channel threshold range.

Improve front-end pulser.

Tailor bandwidth of discriminator.

Plus a number of other changes

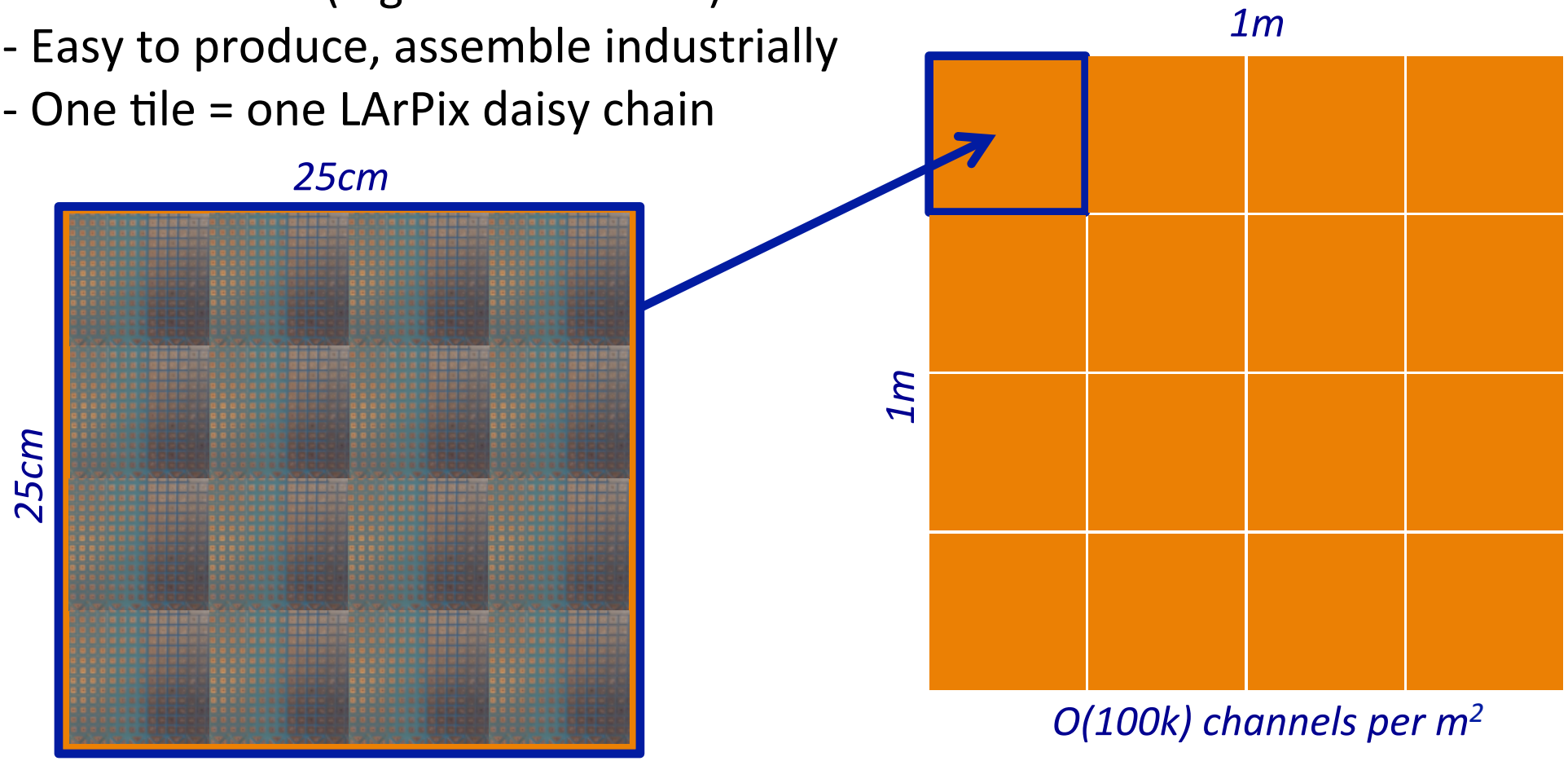


→ *Should start soon in order to meet ArgonCube 2x2 Demonstrator plan (~6 m^2 of readout ready by late 2019).*

Scalability

Design modular pixel tile for instrumenting large area sensors

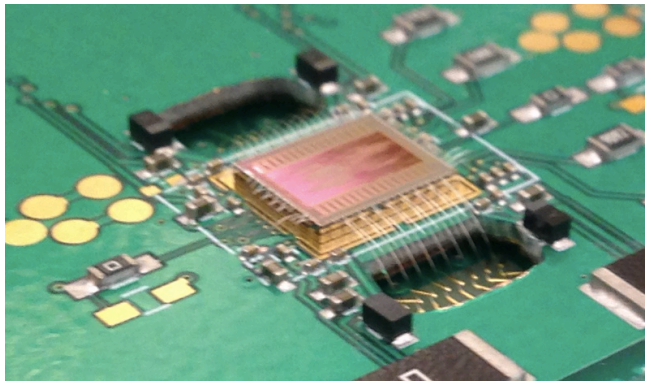
- Standard size (e.g. 25cm x 25cm)
- Easy to produce, assemble industrially
- One tile = one LArPix daisy chain



Demonstration targets:

- Spring 2019: LArIAT TPC: collect particle test beam data at FNAL
- Autumn 2019: ArgonCube 2x2 Demonstrator, 6-m²-scale, a stepping-stone to the DUNE Near Detector.

Discussion



LArPix Characterization:

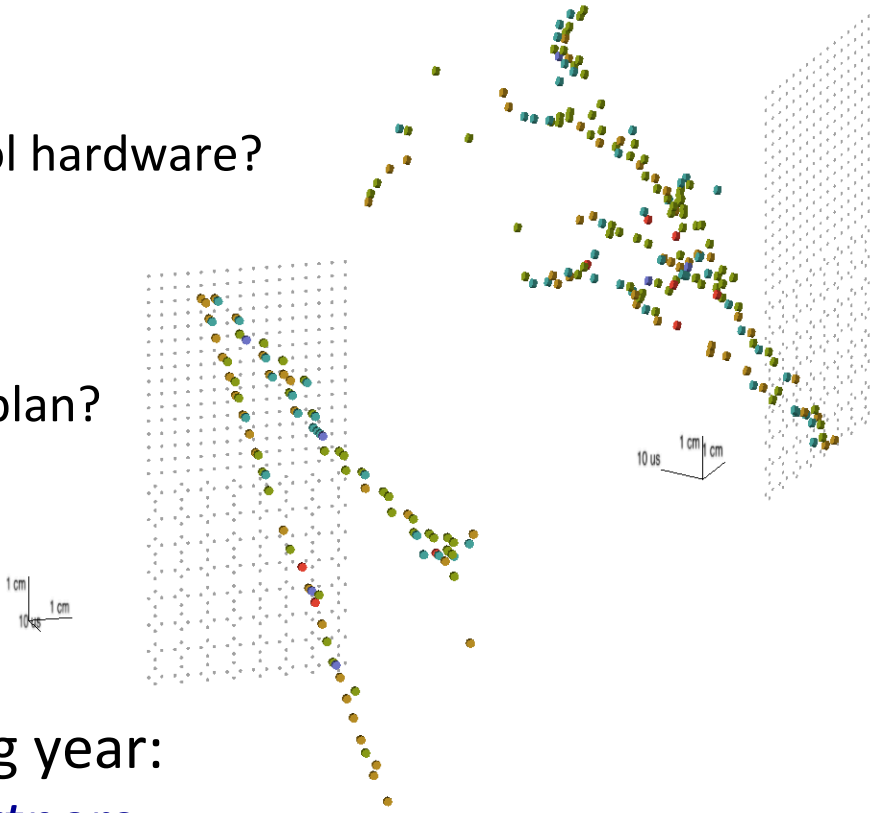
1) Is the current data sufficient to answer major questions:
   - Optimal pixel type for v2 readout?
   - Define targets for v2 ASIC design?
2) Do we aim for another near-term run @ Bern?
3) Schedule of joint publication on pixel readout performance?

Scalable Control Hardware:

1) Plan and schedule for joint effort on scalable control hardware?

Readout for ArgonCube 2x2 Demonstrator:

1) Clear definition of scope and interfaces?
2) Detailed production schedule, integrated with 2x2 plan?
3) Complete end-to-end cost estimate?



Much work needs to be done over the coming year:

→ *Glad to work with any other interested partners*

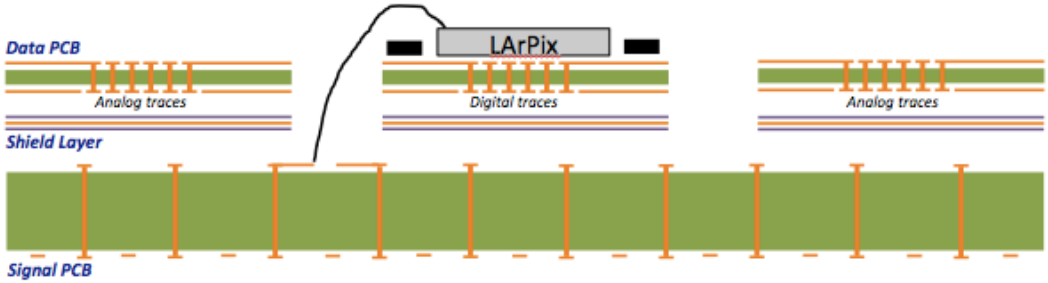
Backup

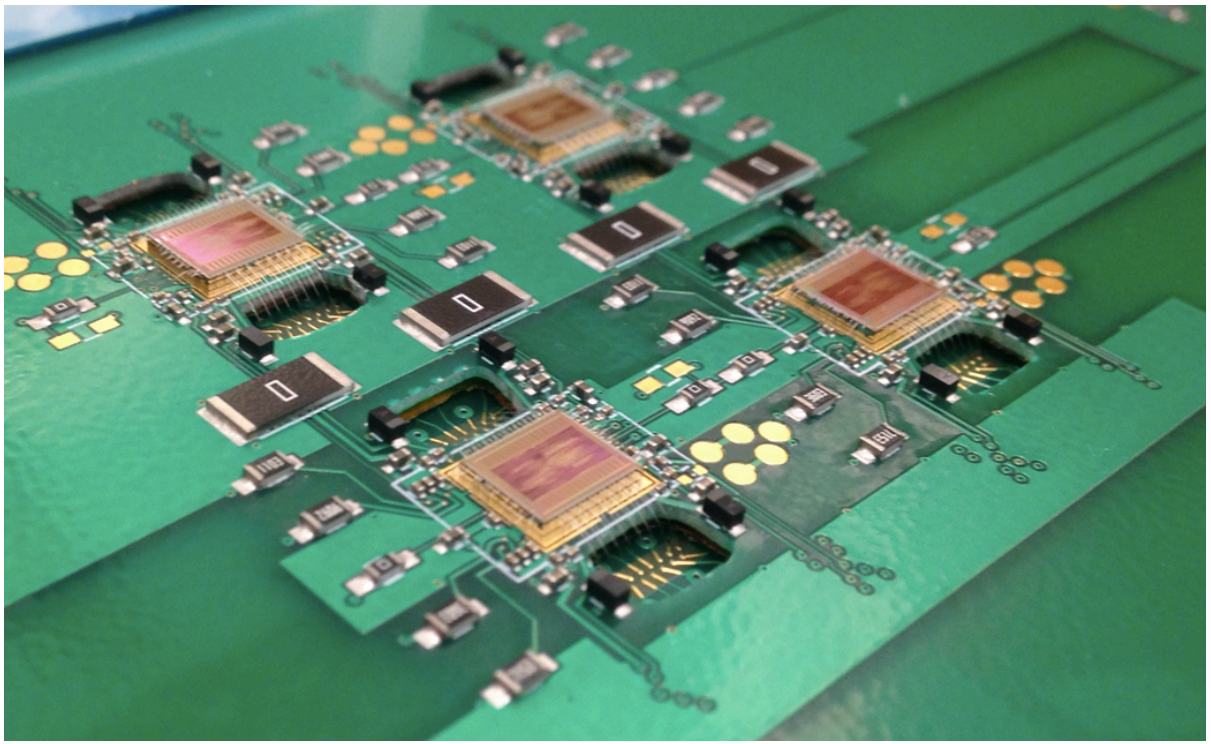
LArPix-v1: Sensor Assembly

LArPix data board attached to sensor board

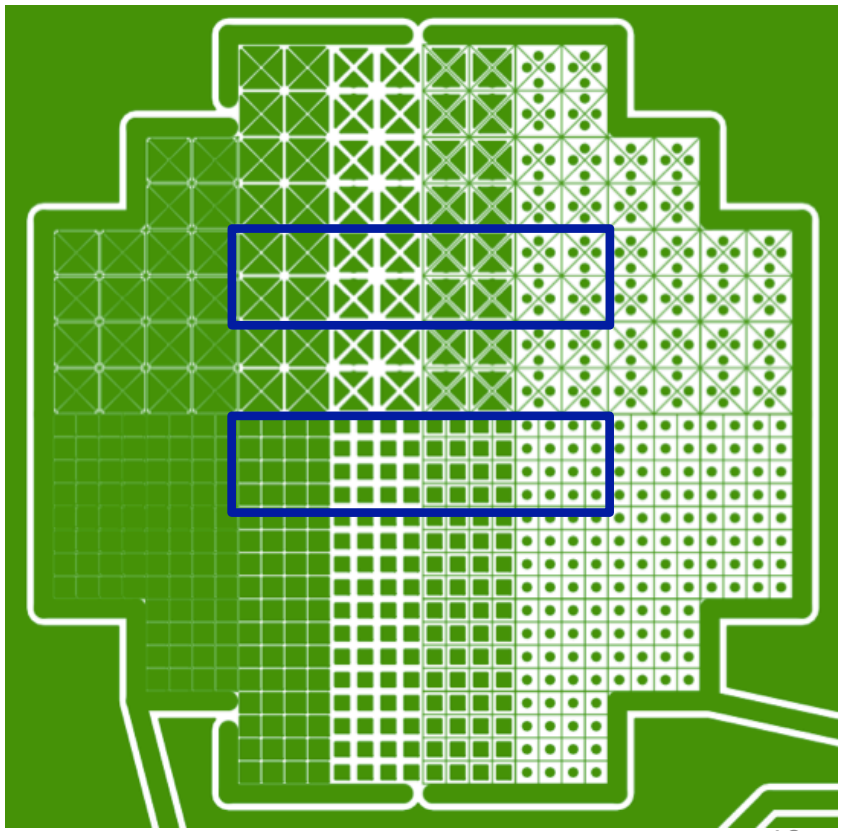
Careful consideration of system grounding and routing for low-noise operation

First test: 128-chip data board used to partially instrument pixel readout plane





Instrumented regions

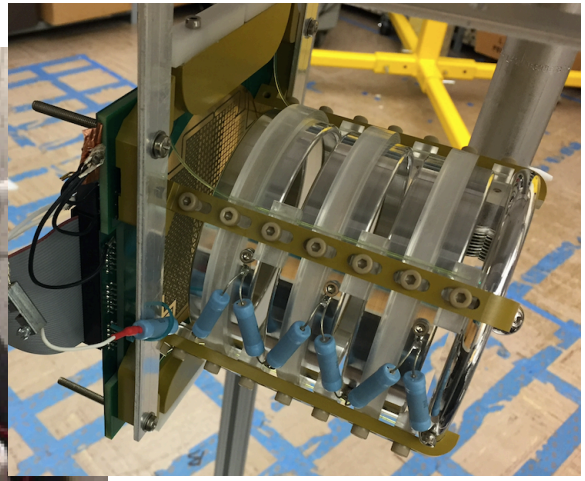


LArPix-v1: TPC Integration

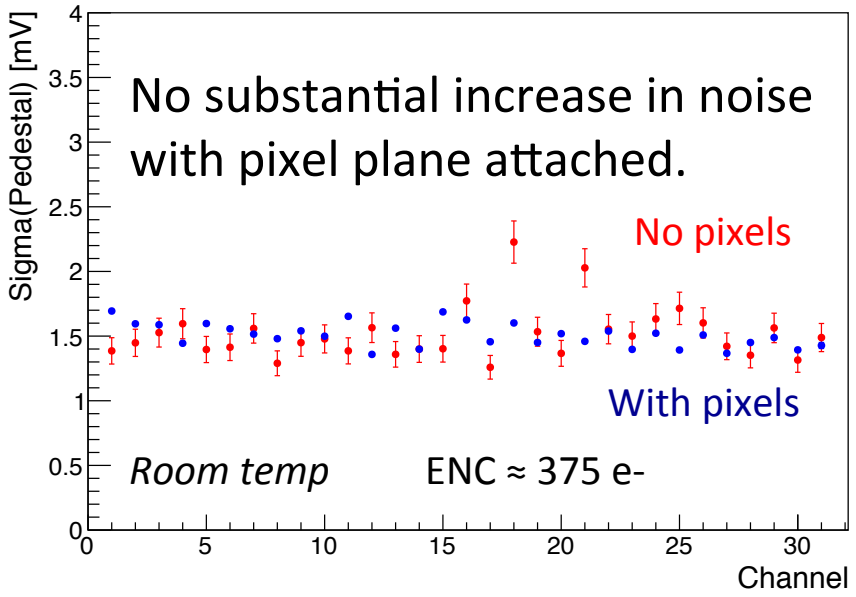
Initial LArTPC operation:

Borrowed LUX/LZ high-purity argon system

Using 10-cm-drift TPC from Bern



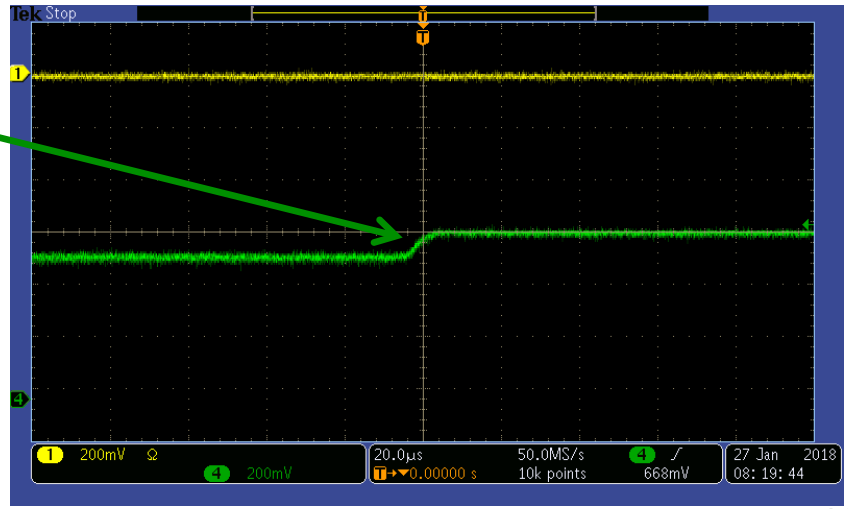
Readout assembly successful:



First cool-down: Jan. 26, 2018

Observed pulses consistent with expectations

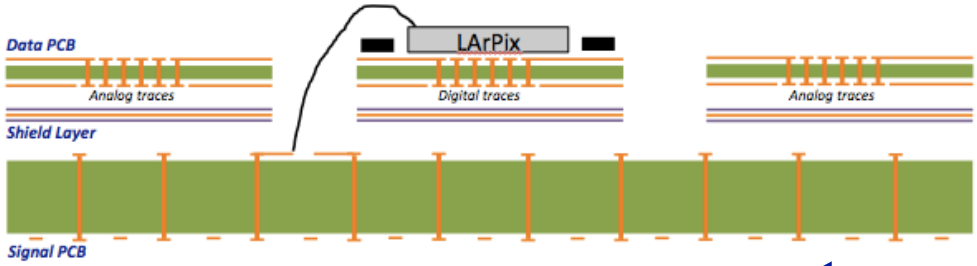
Example pulse consistent with ~25k e- signal (using integrated analog monitor)

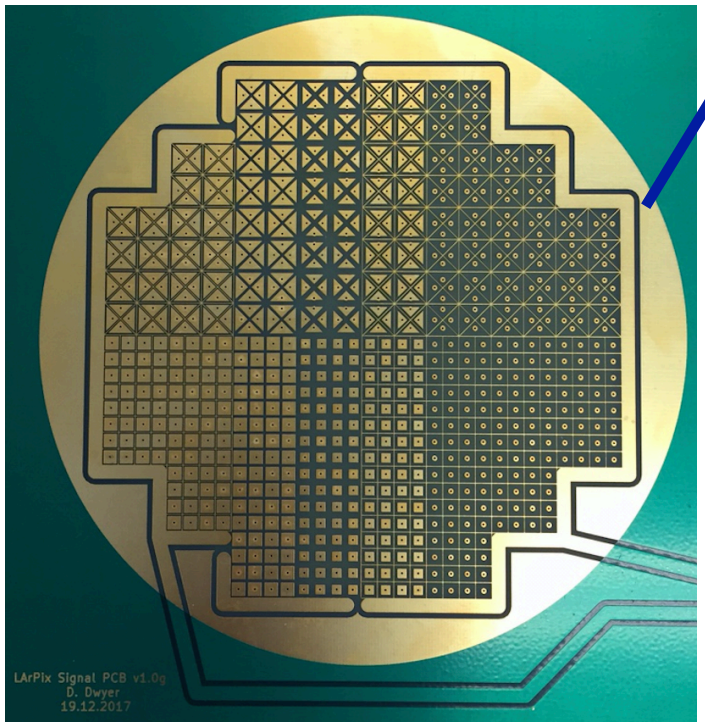


Prototype Scalable Readout

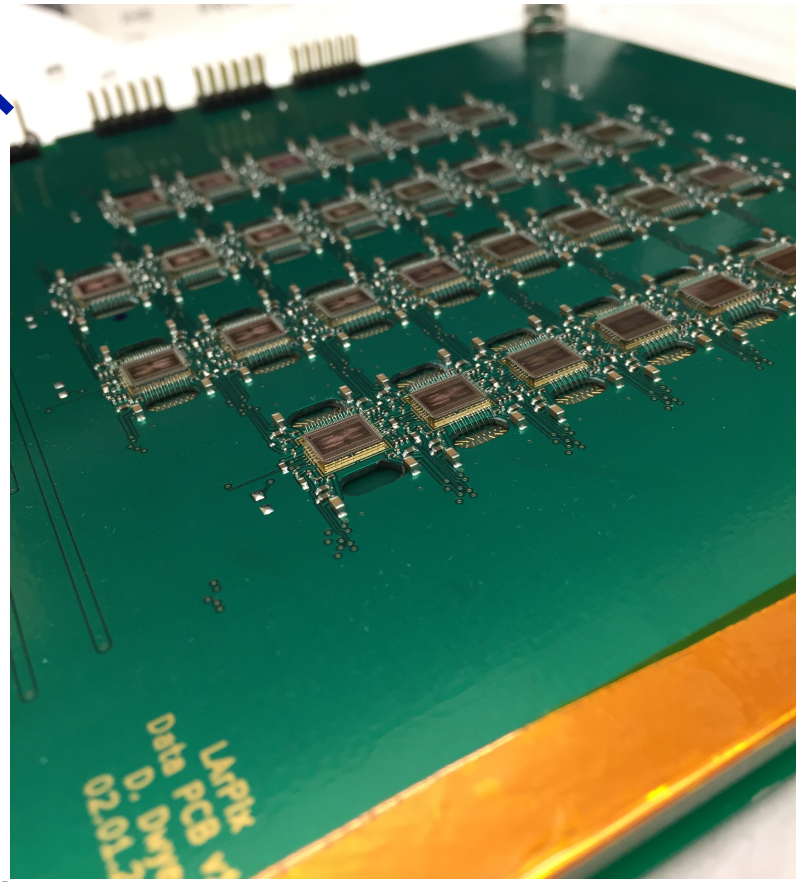
New Readout System:

- Designed new digital data board for scalable pixel readout (dense packing)
- Coupled to 10-cm diameter prototype pixel PCB board
  → Designed to fit both 10-cm-drift TPC (@LBNL) and 60-cm drift TPC (@Bern).





- 832 pixels
- 28 Chips



Scale-test at Bern

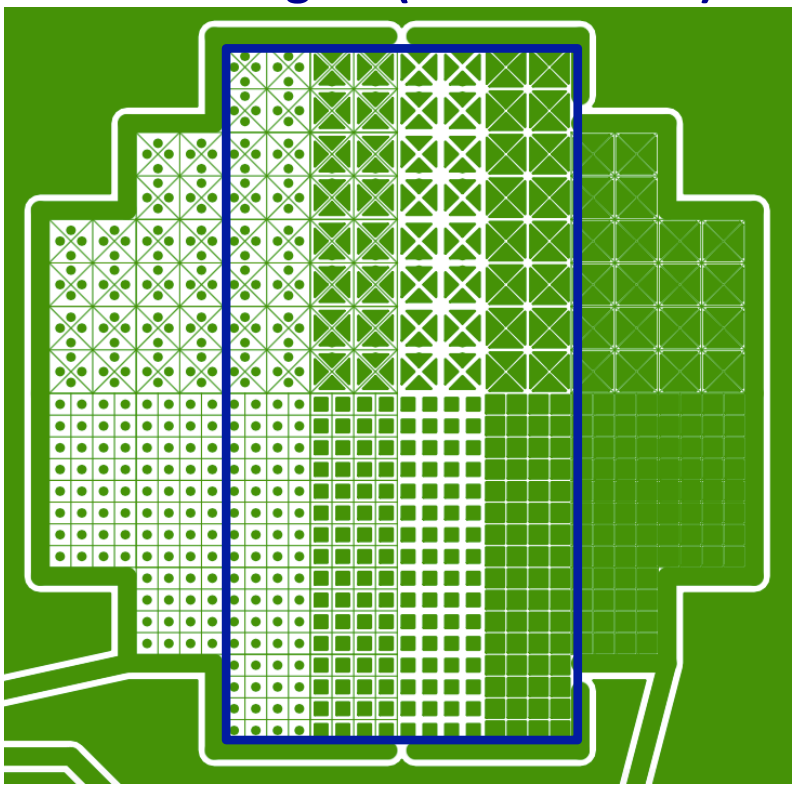
Summary of recent work

- Apr. 5: Wire bonder finished loading 28-chip readout board
  → *Found one chip not functional (DOA); insufficient time to replace, bypassed column 1.*
- Apr. 5 (evening): Tested and tuned readout at room temperature.
- Apr. 6: Operated in LAr to confirm cryo-functionality
- Apr. 7: Actively heated cryo-system to room temp, extracted readout, packed for Bern
- Apr. 8-9: Hand-carried readout and control to Bern
- Apr. 10: Warm test and debugging
  → *Found one chip damaged in transit or testing, bypassed column 4.*
- Apr. 10 (evening): Installed in 60-cm-drift TPC
- Apr. 11: Cooled, filled TPC with liquid argon
- Apr. 12-Apr. 19: TPC operation

Thanks to Sam Kohn, Peter Madigan for long hours preparing system for operation.

Thanks to entire Bern group for effective, round-the-clock TPC operation.

Active region (512 channels)

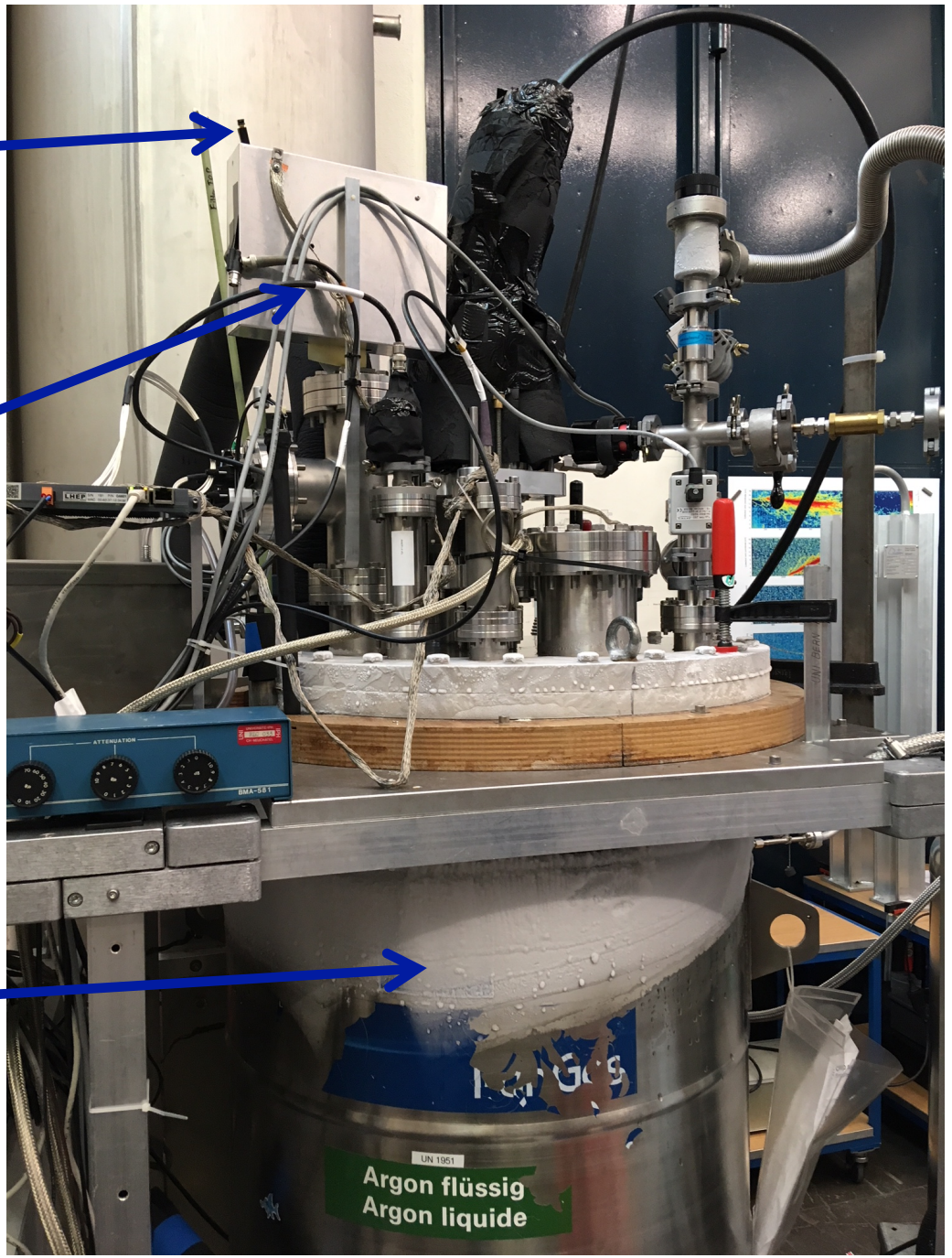


Installation

LArPix WiFi Antenna

LArPix Control System

TPC Installed in LAr Cryostat



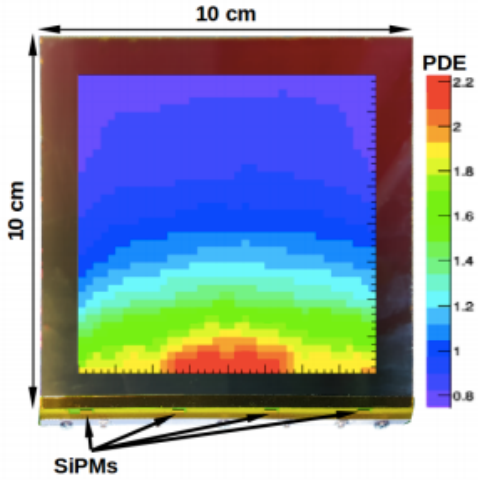
Description of LAr System: (TPC, Cyrostat, HV, etc.)
arXiv:1801.08884

Bern LArTPC System

ArCLight Photon Detection System:

- Independent DAQ
- Triggers on SiPM coincidences (8 SiPMs total)
- Issues trigger output signal, 1pps output signal

ArCLight: arXiv:1711.11409



Muon Telescope:

- Identifies muons oriented along 60-cm drift.
- 4 large scintillator paddles (two above, two below cryostat)
- Issues trigger output signal on 4-fold coincidence of all paddles

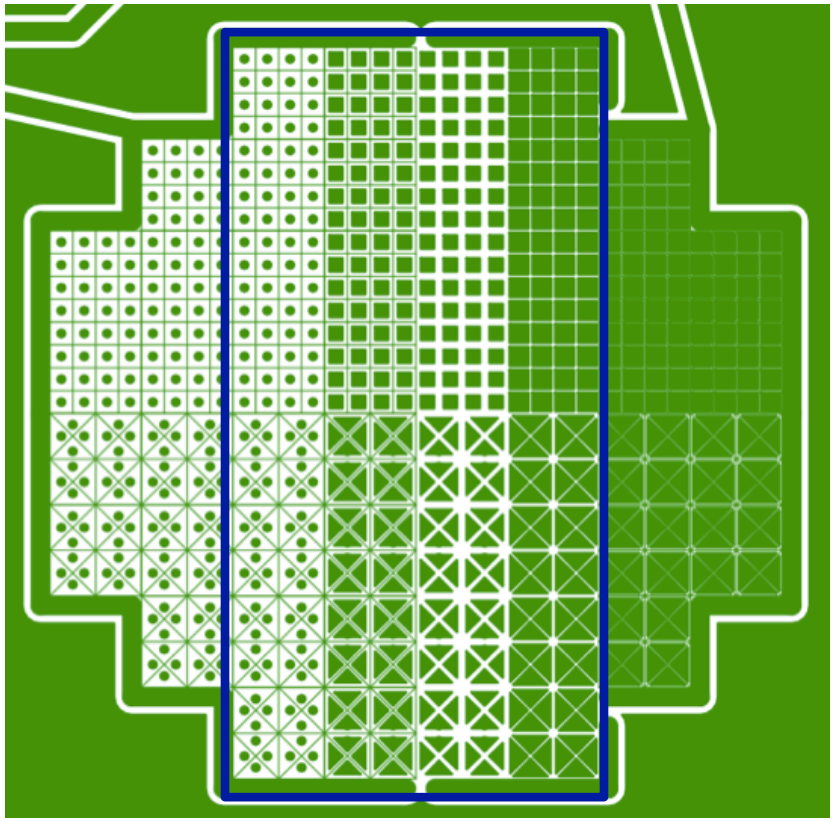
LArPix Charge Detection:

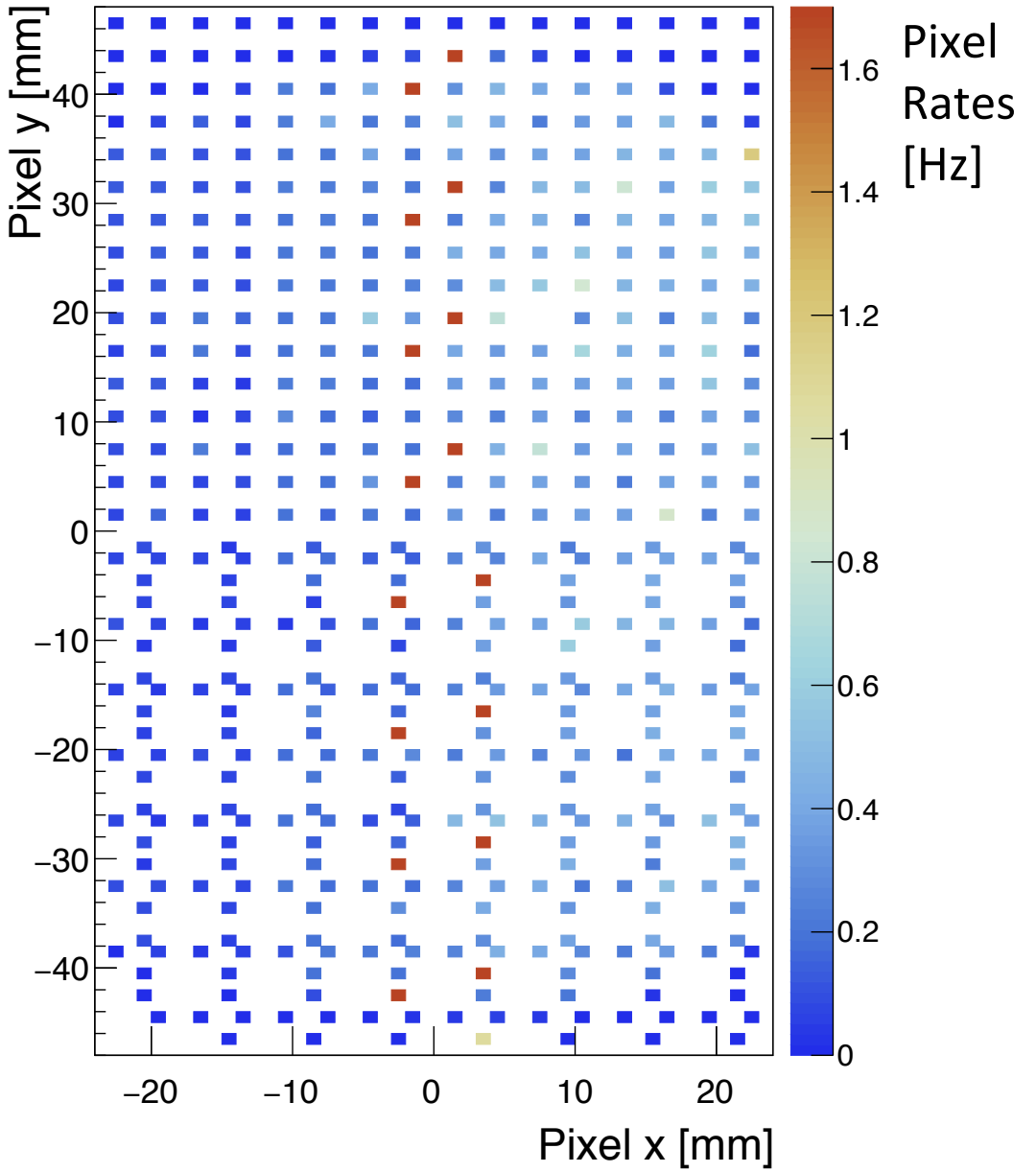
- Self-triggers on charge signal incident on any pixel
- Accepts ArCLight trigger, 1pps, Muon Telescope trigger output signals, and uses to imbed t_0 marker in LArPix data stream.

Pixel Trigger Rates

Observations:

- Red pixels: t_0 marker
- Top, bottom edges: lower rates due to TPC drift field non-uniformity
- Right side higher rate than left: Combination of pad size and focusing grid (grid currently not biased)
- One pixel disabled due to high rate





System ran stably, continuously for entire week of LArTPC operation.