LVDS Driver & Receiver:

The LVDS Driver & Receiver circuits are used for fast Off-Chip communication and implement the functionality described in the Low Voltage Differential Signal standard ANSI (EIA)–644-1995 as far as the restrictions of the chosen technology allow.

The LVDS driver works like a switched current source that drains/sinks the output current through the termination resistor. The output current is configurable and can be also switched-off completely giving rise to a high impedance state at the output (tristate version).

The LVDS receiver detects the differential signal and converts it to a CMOS signal for on-chip use. The LVDS receiver has a rail-to-rail input stage which allows operation in a wide common-mode range of the input signal. The rail-to-rail input state has been implemented by a NMOS and a PMOS differential input pair operating in parallel. A failsafe feature is implmented by applying a dedicated bias to the receiver input and assuring a nonzero differential voltage

Because of the use of thin-gate core transistors, the maximum supply voltage is limited to small values which as a result limits the possible input common-mode range to values lower than defined in the standard.

LVDS driver specification:

$f_{transmission}$=320 MHz (640Mbit)
V_{supply}=1.2-1.5V
I_{out}=600u-3m A
Power Consumption: (I_{out} + 660uA)* V_{supply} (Static)

LVDS receiver specification:

$f_{reception}$=160 MHz (320Mbit)
V_{supply}=1.2-1.5V
Power Consumption: 140uA * V_{supply} (Static)

LVDS circuits schematics:

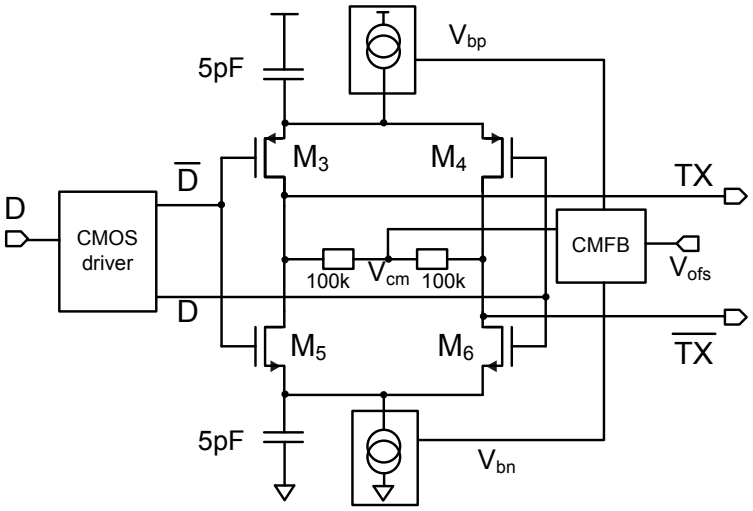

Fig 1: LVDS driver block diagram

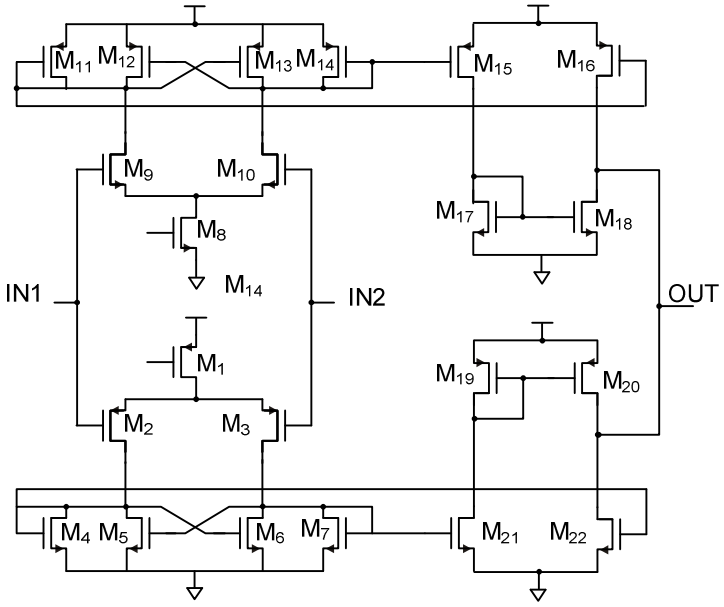

Fig 2: LVDS receiver circuit

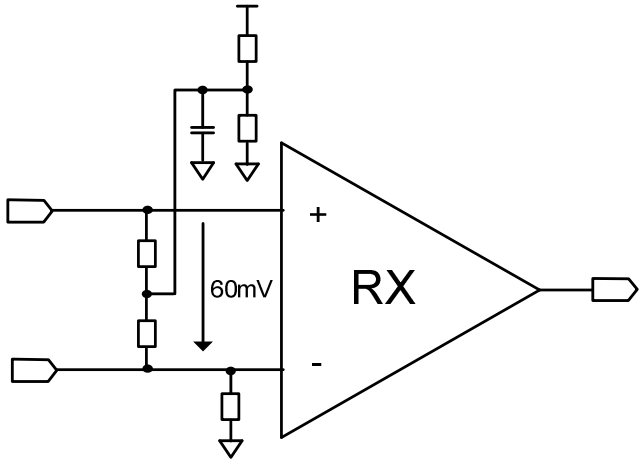

Fig 3: LVDS receiver failsafe & AC couple bias circuit

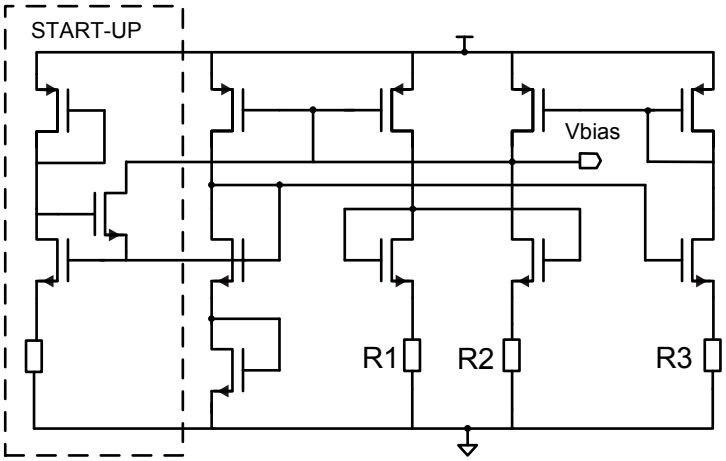

Fig 4: LVDS receiver failsafe & AC couple bias circuit

VDS driver Interface:

Pin Name	Input From	Output TO	INOUT?	Description	Specifications if any	Comments and requests
Iref				Bias Current controlling the output current level	60uA	
Vos				Output common-mode voltage	half of supply voltage	Generated internally can be overwritten
DIN				CMOS input signal for off-chip communication	max. 320 MHz	
EN				output current enable, gives high impedance output state if set to LOW		Only with tristate version
SET06				Sets output current to 600uA		
SET12				Sets output current to 1.2mA if SET06 is also set		
SET30				Sets output current to 3mA if SET06 is also set		
TX		Off-Chip		LVDS non-inverting output signal		
TXn		Off-Chip		LVDS inverting output signal		

Table 1.0. LVDS driver interface

Pin Name	Input From	Output TO	INOUT?	Description	Specifications if any	Comments and requests
Ibn				Bias Current for NMOS input pair	35uA (flowing in)	
Ibp				Bias Current for NMOS input pair	- 35uA (flowing out)	
OÚT				CMOS output signal	max. 320 MHz	
RX	Off-Chip			LVDS non-inverting input signal		
RXn	Off-Chip			LVDS inverting input signal		

Table 2.0 LVDS receiver interface

LVDS driver status:

Two versions available (one with and one without tristate output option), produced and tested Translation into new OA database is performed. Transfer to DM metalization and T3 substrate isolation has been done. It might be worth to adapt the layout to the FE-I4 bond pad pitch of 150um and make use of technology options like T3 and MimCaps.

LVDS receiver status:

Ported to OA, DM metalization and T3 substrate isolation, Failsafe feature added & biasing developed