RD53A: a large scale prototype for HL-LHC silicon pixel detector phase 2 upgrades

ABSTRACT (max 100 words)

The Phase 2 upgrades of silicon pixel detectors at HL-LHC experiments feature extreme requirements, such as: 50x50 µm pixels, high rate (3 GHz/cm^2), unprecedented radiation levels (1 Grad), high readout speed, serial powering. As a consequence a new readout chip is required.
In this framework the RD53 collaboration submitted RD53A, a large scale chip demonstrator designed in 65 nm CMOS technology, integrating a matrix of 400x192 pixels. It features design variations in the analog and digital pixel matrix for testing purposes. An overview of the building blocks will be given together with comprehensive test results on single chips and modules.

SUMMARY (max 500 words)

The High Luminosity Large Hadron Collider (HL-LHC), starting its operation in 2026, will constitute a new frontier for particle physics. Major experimental challenge resides in inner tracking detectors: here the dimension of the sensitive area (pixel) has to be scaled down with respect to LHC detectors. In order to cope with the extreme requirements in terms of particle rate and radiation hardness, a new generation pixel readout chip has to be designed. The RD53 collaboration was founded at CERN for this purpose. Twenty-four institutions are involved.

The goals of the collaboration include the comprehensive understanding of radiation effects in the 65 nm technology together with the development of tools and methodology to efficiently design large complex mixed signal chips. Lately, its purpose is the development of a full sized readout chip featuring a 400x400 pixel array with 50 um pitch capable to operate with serial powering.

As an intermediate step towards the final implementation the RD53A demonstrator chip has been designed. The chip size is 20.0mm by 11.8 mm. RD53A is not intended to be a production IC for use in an experiment, and contains design variations for testing purposes, making the pixel matrix non-uniform. The 400x192 pixel matrix features in fact three flavors of analog front-ends and two digital readout architectures. The pixel matrix is built up of 8 by 8 pixel cores. In addition the 64 front-ends within a core are organized in 16 so-called analog islands with 4 fronts ends each, which are embedded in a flat digital synthesized sea.

The peripheral circuitry is placed at the bottom of the chip and contains all global analog and digital circuitry needed to bias, configure, monitor and readout the chip. The power and bias distribution have been designed for a larger number of rows in view of the final chip implementation. RD53A is designed for single supply serial powered operation with connections from the bottom of chip only but for testing purposes it is also be possible to power the chip by directly supplying the internal rail voltages, bypassing the regulation.

RD53A has been submitted in August 2017 and is now undergoing a comprehensive characterization phase. Test results on single chips including performance qualification for the three analog front-ends will be presented, together with first tests on modules of RD53A bonded with sensors. In addition, the ongoing activities in view of the final chip implementation for the experiments will be outlined.