Characterization of soft error rate against memory element spacing and clock skew in a Triple Modular Redundancy (TMR) logic using RD53SEU test chip

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Abstract

Single Event Effects introduce soft errors in ASICs designed for particle detector applications as they are operated in an extreme radiation environment. Design methodologies like Triple Modular Redundancy (TMR) with clock skew insertion, a system level redundancy technique is a common practice by designers to mitigate soft error rates. However, at this juncture the optimal spacing between memory elements in a TMR in 65nm technology has not been addressed. RD53SEU is a mini ASIC development under the framework of the CERN RD53 collaboration to characterize the soft error rates against the separation spacing between memory elements in a TMR. These memory elements can be flip-flops or latches. Also, the chip hosts additional test structures such as an e-fuse from the foundry and clock skew based TMR. In all cases, their soft error rate is estimated. This article describes the architecture and design aspects of the RD53SEU test chip.

Summary:

Single Event Effects (SEEs) are very common in ASICs developed for detector electronics as they are exposed to energetic ionizing particles from the particle collisions. SEEs comprise of Single Event Upsets (SEUs) and Single Event Transients (SETs) and manifest themselves as bit flips in sequential elements and glitches in combinational gates. A Single Event Upset (SEU) in data path register results in incorrect data packets from the serial links, where as an SEU in global configuration registers can make the chip non-functional.

In a joint effort between Atlas/CMS groups for RD53B pixel chip, the estimated bit flips due to SEUs in global configuration registers is one-bit flip per ~20 seconds per chip, whereas in pixel registers is ~60 bit flips per second per pixel per chip. Hence SEE tolerant design is unavoidable for RD53B at pixel configuration registers, global configuration registers and data path registers in digital chip bottom. Triple Modular Redundancy with clock skew is a system level redundancy technique to counter single event effects.

Before resorting to Triple Modular Redundancy (TMR), the common design related questions or designer guidelines must be addressed. One of them is, what should be the spacing between memory elements and how does this impact soft error rate and layout efficiency. Characterizing soft error rate as a function of memory spacing in a TMR helps designers to choose optimal spacing for their applications. An optimal spacing also determines the area of the design. A similar question arises with latch based TMR as well. Study of soft error rates on latch based TMR is also crucial as they are often used to measure the TOT in a pixelated integrated circuit. It is also understood that by introducing clock skew between memory elements in a TMR logic, designers can mitigate single event transients. Clock skewing affects the timing margin of the designs and

the optimal clock skew to mitigate SEE hasn't been addressed. All these designer guidelines can be addressed through a test chip RD53SEU, it's architecture and the design of various test structures is presented in this article. The chip is expected to be submitted in August 2018.