Radiation-induced effects on data integrity and -link stability of RD53A

M. Vogt, M. Daas, T. Hemperek, F. Hügging, J. Janssen, H. Krüger,
D.-L. Pohl, P. Rymaszewski, T. Wang and J. Dingfelder, N. Wermes (Bonn)
L. M. Jara Casas (CERN), M. Menouni (CPPM)

Abstract (max. 100 words):

The RD53 collaboration is currently designing a second large-scale prototype pixel readout chip in 65 nm CMOS technology for the phase-2 upgrade at the HL-LHC.

During the lifetime of the new pixel readout chip, it will be exposed to a Total Ionizing Dose of approximately 500 Mrad. Irradiation studies of the first prototype chip RD53A revealed a limiting radiation tolerance concerning the clocking- and communication periphery, which has to be understood before the submission of the next prototype chip RD53B.

Details of the performance after irradiation will be presented and strategies for mitigation of the radiation effects will be discussed.

Summary (max. 500 words):

The phase-2 upgrade of the LHC will substantially increase the instantaneous luminosity. This requires novel pixel readout chips with highly complex digital architectures, which deliver hit information at drastically increased data rates and unprecedented radiation tolerance, especially close to the interaction point. The RD53 collaboration was formed to approach these challenges by designing a prototype pixel readout chip in 65 nm CMOS technology, which is suitable for the innermost layers of the pixel detector in the ATLAS and CMS experiments.

The large scale prototype chip RD53A has been produced and is available since December 2017. The locking behavior and the stability of the high speed Aurora links of un-irradiated RD53A chips have been investigated in lab environments with different cables, powering schemes, PLL configurations and synchronization patterns. Performance characterization measurements of the output line drivers are ongoing.

The readout system BDAQ53A has been developed to perform characterization- and test beam measurements. It consists of an FPGA-based readout board and a Python-based data acquisition and analysis framework. For data reception from the RD53A chip at rates of up 1.28 Gbit/s, high speed GTX hardware transceivers are used. They offer various configuration options, which will allow dynamic optimization of the data link during operation, and feature Integrated Bit Error Ratio Test capacities to analyze the link quality.

First irradiation studies up to 500 Mrad at room temperature have shown that the data link fails after ~300 Mrad and can be recovered only partially after annealing. In order to understand the degradation of the clocking- and communication periphery of RD53A, further investigation are necessary.

During the upcoming irradiation campaigns, the chip will partially be operated in a non-default bypass mode, in which the integrated PLL and Command Data Recovery units are not used. This allows to operate the chip at a much wider digital frequency- and supply voltages range. Various scan routines will monitor the chip performance during the campaigns. The digital logic of the chip will be monitored by continuously writing and reading global and in-pixel registers to identify Single Event Upsets. Variations in the threshold distribution and noise of the analog front-ends will be analyzed as a function of the Total Ionizing Dose.

Based on the results, methods to improve the operating parameters and design changes for the upcoming RD53B chip submission will be evaluated and discussed.