System level serial powering studies of RD53A chip

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Abstract:

Serial powering is the baseline choice for low mass power distribution for the CMS and ATLAS HL-LHC pixel detectors. The RD53A prototype chip (65 nm CMOS) integrates 2 shunt-LDO (SLDO) regulators that allows providing constant voltage to each power domain (analog and digital) within a serial power chain with constant current. This paper presents a detailed analysis based on simulations and measurements of the RD53A chip behavior at system level. SLDO performance, system transient behavior (start-up, load changes, parasitic components implications) as well as noise studies are shown.

Summary:

The unprecedented radiation field and hit rate present at the HL-LHC inner trackers poses a very strong requirement on the front-end electronics. To cope with this challenge, the RD53 collaboration was established across the CMS and ATLAS experiments, dedicated to the development of a pixel readout ASIC. The RD53 collaboration has very recently achieved the first major milestone: the submission of the RD53A large-area, full-fledged prototype readout chip (ROC) based on a 65 nm CMOS technology.

The extreme high rate operation of the ROC requires the use of a modern high density low power CMOS technology with low supply voltage (1.2V), resulting in a pixel chip that must be supplied with significant current levels (~2A per chip). During the last years, extensive studies have shown that a serial power distribution system is the only feasible scheme to supply the pixel detector with the required power within an acceptable material budget and power cable losses. Small-scale system tests based on the FEI4 pixel chip (developed for ATLAS IBL upgrade) have demonstrated that serial powering is a viable powering scheme, when using specially developed on-chip serial power regulators.

The baseline design contains serial power chains of eight pixel modules on average with several chips (1 to 4) per module connected in parallel. Locally, a shunt–LDO (Low Drop Output) regulator on the pixel chip assures that power/current consumption is kept constant independently of chip consumption. The pixel chip itself is powered with two independent SLDOs: one for the analogue circuitry and one for the digital logic. The serial chains will be powered remotely by primary current sources.

Serial powering topology has never been used in any high-energy physics experiment, and so it is being exhaustively simulated and tested using different prototypes such as the RD53A chip, and

dedicated SLDO prototype chips. With the aim of optimizing and testing the reliability of serial powering, several studies are being carried out. So far, it has been proven a stable and reliable solution during preliminary tests, although, there are still some concerns and issues to be addressed and optimized for the final systems and chips.

This paper presents a general overview of the RD53A chip behavior at system level. Aspects such as transient response of the chip due to start-up, load changes as well as parasitic components effects are presented. These extensive studies have allowed defining and optimizing the configuration parameters of the SLDO. In addition, noise immunity analyses will be presented and used to define the correct filtering and grounding design of the High Density Interconnect flex boards (HDI). All these studies have been carried out based on simulations and tests performed with the first prototypes of the RD53A chip.