# Design and characterization of a high speed transmitter circuit for the ATLAS/CMS HL-LHC pixel readout chip

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## Abstract (max. 100)

In order to satisfy the high output bandwidth requirement imposed by the HL-LHC, a high speed transmitter circuit was designed and integrated into the RD53A demonstrator chip for the HL-LHC pixel detector. A CDR/PLL circuit recovers clock from the 160 Mbps incoming data, and provides high speed clock to the serializer, where the 1.28 Gbps output stream is formed. The output stage employs a three-tap current-mode logic driver with adjustable tap coefficient for optimal pre-emphasis. Each RD53A chip includes four output lanes, offering in total 5.12 Gbps output bandwidth. The circuit topology as well as measurement results will be presented.

## Summary (max. 500)

The substantially increased instantaneous luminosity after the phase-2 upgrade of LHC (HL-LHC), together with a higher trigger rate (1 - 4 MHz), calls for much higher output bandwidth for the pixel front-end chip. Therefore, a high speed transmitter circuit, running at the nominal speed of 1.28 Gbps, has been designed and integrated into the RD53A demonstrator chip for the ATLAS/CMS HL-LHC pixel detector, which has been fabricated in a 65 nm CMOS technology. By combing four output data lanes, each RD53A chip offers the maximum output data rate of 5.12 Gbps. This work focuses on the design and characterization of the high speed transmitter circuit of the RD53A chip.

The transmitter circuit uses the 1.28 GHz clock provided by a clock and data recovery (CDR) circuit, which recovers the clock from the 160 MHz incoming chip command stream and its internal PLL produces all the clocks required for the chip operation. Using this high speed clock, a serializer circuit produces a 1.28 Gbps bit stream out of the 20-bit parallel data provided by the data encoding block. The output stage of the transmitter employs a current-mode logic (CML) driver. In order to compensate for the high frequency signal loss over a low mass cable, a three-tap finite impulse response (FIR) filter was implemented at the output stage. Each tap is delayed by one unit interval with respect to the previous, and the weight of each tap can be adjusted by a 10-bit DAC. The maximum current driving capability for each tap is ~ 15 mA. In addition, the enabling and output polarity of the two later taps can be fully controlled, offering the flexibility to have different pre-emphasis configurations.

First measurements show that the quality of the output data given by the transmitter

is strongly influenced by the chip activity. The rms jitter is 25.9 ps when having the full chip running, and decreased to 13.5 ps after disabling the pixel matrix activity. Further studies revealed that the lack of additional buffering stages for the VCO (Voltage Controlled Oscillator) bias control signal has caused the noise from the global digital power domain coupled into the VCO circuit, and therefore degrades the clock quality produced by the CDR/PLL. This was later confirmed by editing a chip sample with focused ion beam. In the edited chip, the connection of these VCO bias control signals was redirected to the CDR/PLL local power domain, thus isolating the noise from the global digital power domain. The dependency of jitter performance on the chip activity was no longer observed for the edited chip. The next step includes characterizing in detail the performance of the CML driver. A new CDR prototype is also under development, with several design improvements to reduce the clock jitter produced by the PLL.

In this contribution, the circuit design as implemented in the RD53A will be presented, together with the discussion of measurement results.