ESD Diode protection integration on chamber design

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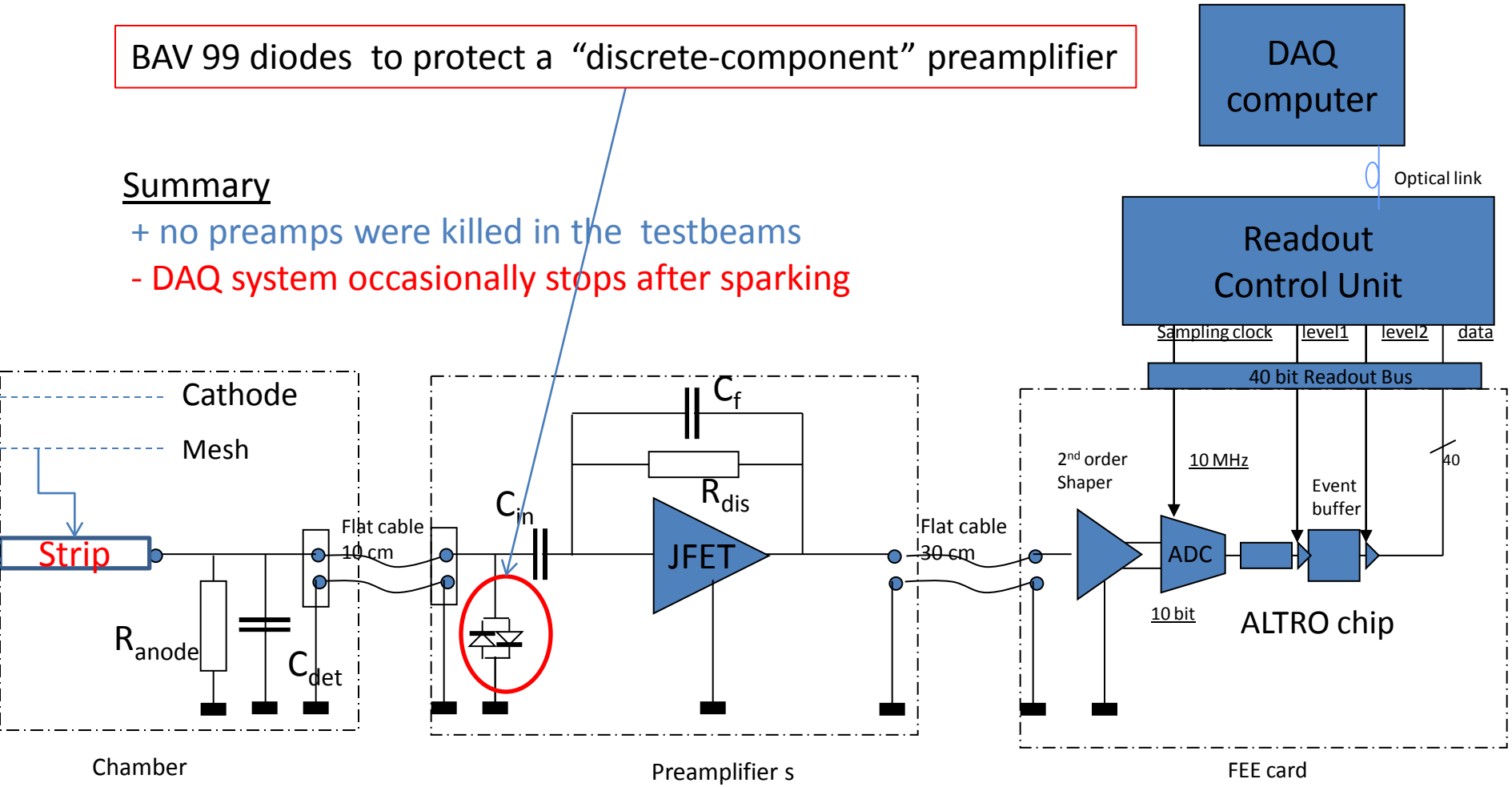
MM ATLAS 2008/9 Test setup

BAV 99 diodes to protect a "discrete-component" preamplifier



Summary

+ no preamps were killed in the testbeams

- DAQ system occasionally stops after sparking

Lessons learnt from the 2008/9 system

A.) VITAL for commissionable operation

- Sparc protection: does it reliably protect chip-resident preamp inputs ?
- Spark protection to include readout immunity
- Crosstalk to be reduced
- Detector capacitance not to me altered by sparc protection
- real estate is a problem for discrete diodes

Proposed solution: ESD diodes on chamber +

➔ Capacitive coupling to preamp
➔ low impedance common grounding to chamber GND
➔ no signal cables to pre-amps
➔ chamber and pre-amp ground connected via low impedance plug
➔ new Industry ESD diodes made for sparc protection of Gigabit chips
➔ ESD diode ground must be quasi inductance-free to chamber ground
➔ reverse biased ESD diodes do not add more than ~1pF

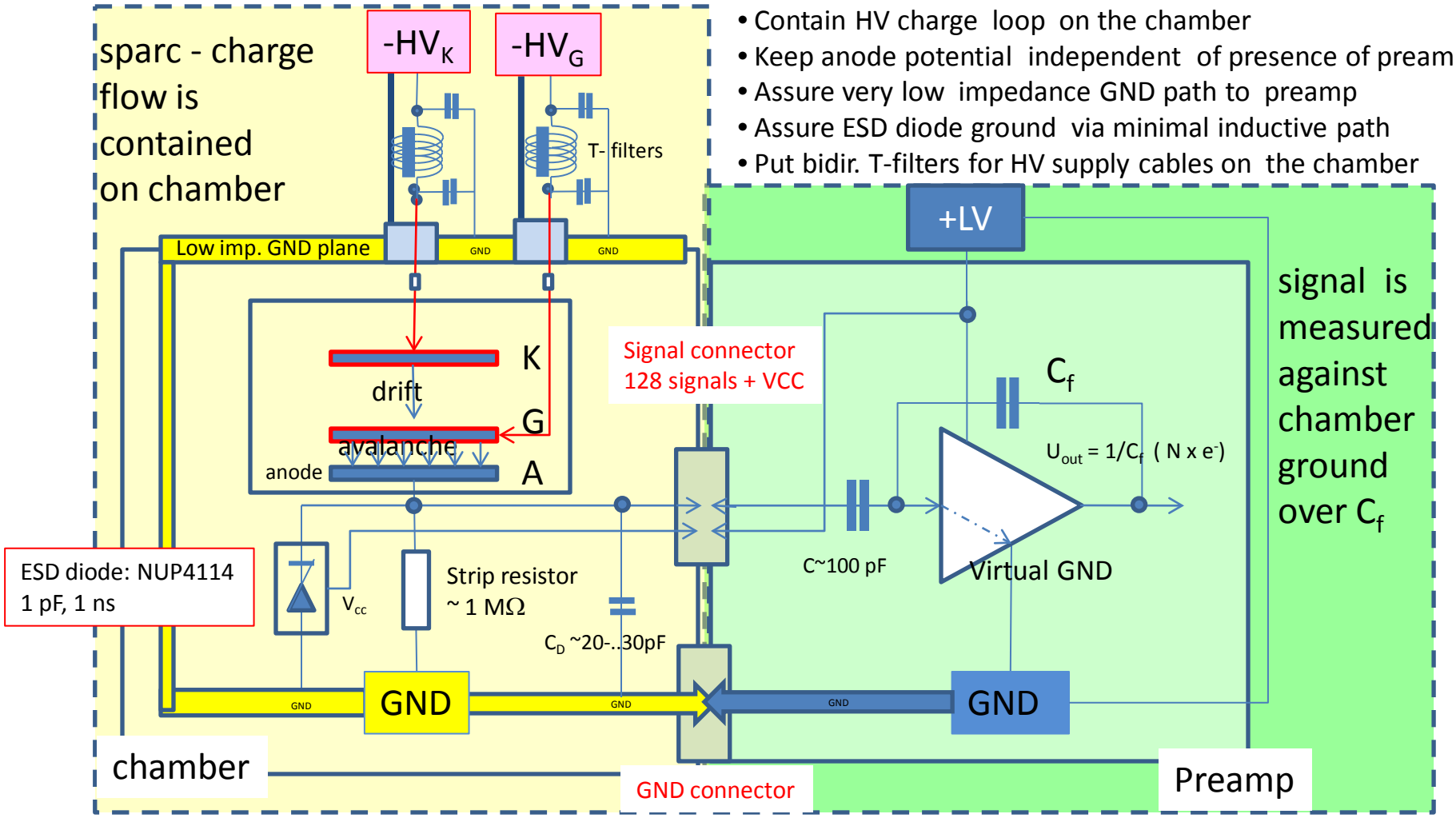
B.) DESIRABLE for smooth operation

- Spark monitoring channel
- Test pulse for all channels

Proposed solution: pickup strip

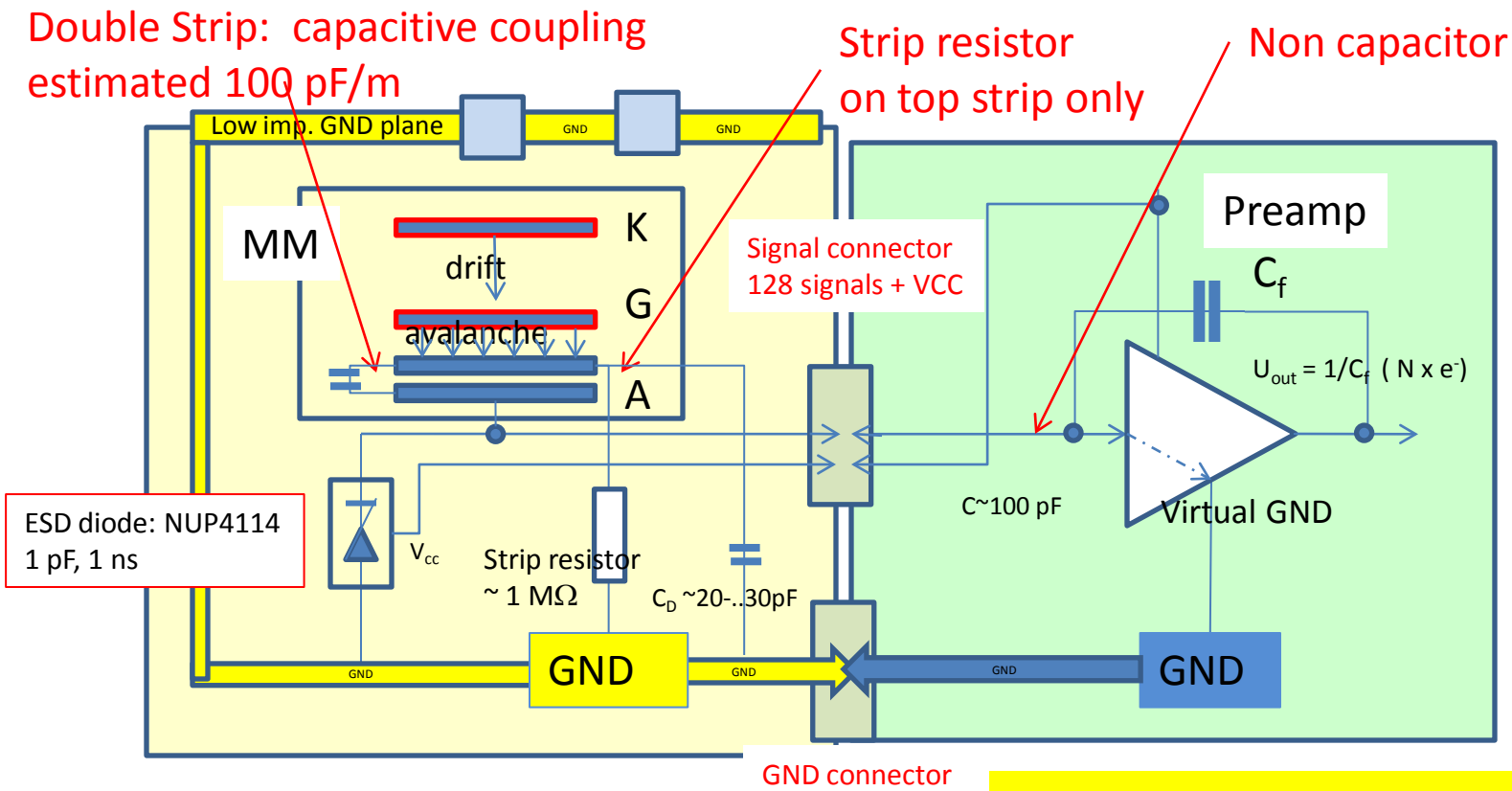
➔ capacitive coupled common pickup strip for groups of strips
➔ pulse injection either via pickup strip or via Chip test feature

Equivalent circuit for an optimized protection



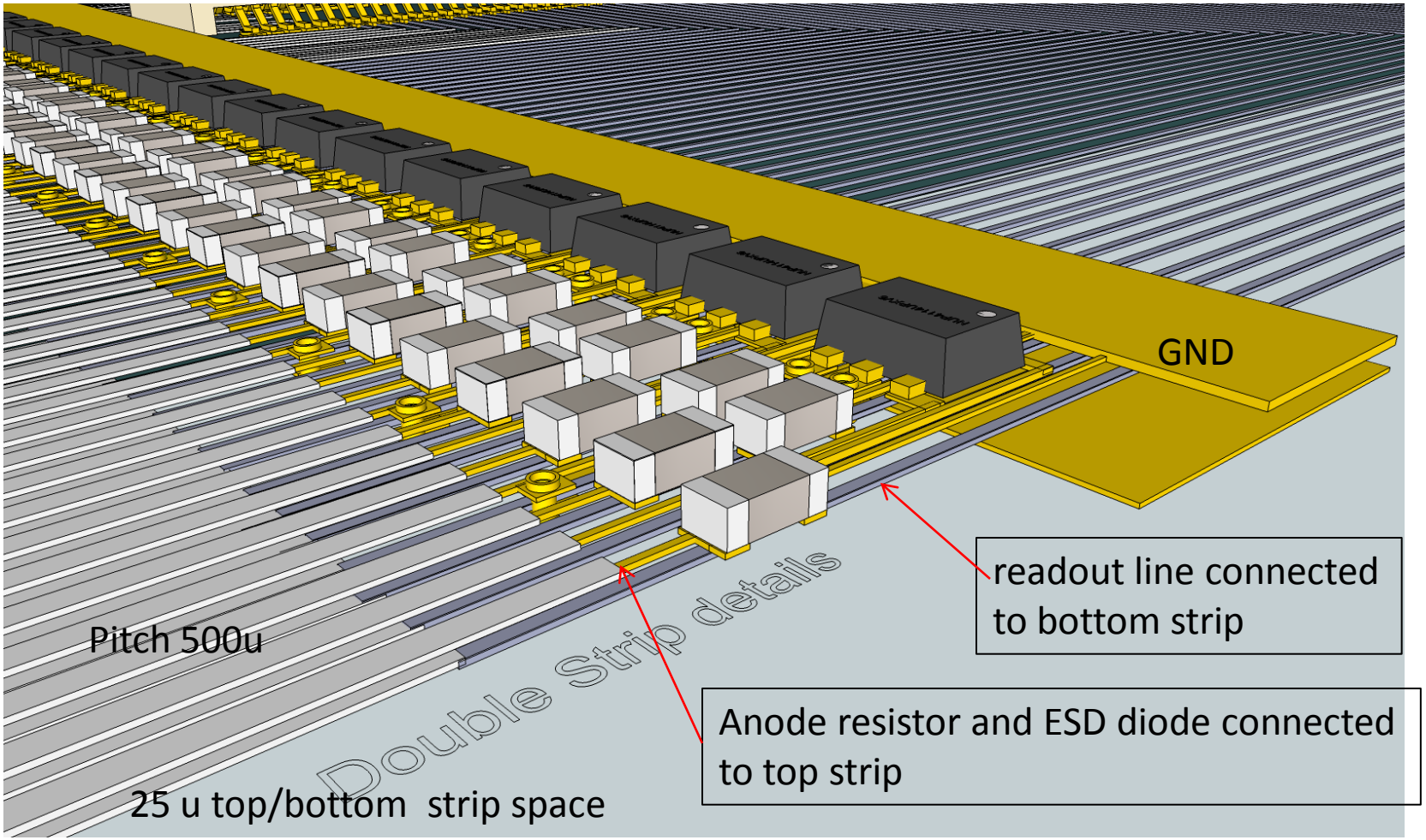
- Contain HV charge loop on the chamber
- Keep anode potential independent of presence of preamps
- Assure very low impedance GND path to preamp
- Assure ESD diode ground via minimal inductive path
- Put bidir. T-filters for HV supply cables on the chamber

MM chamber: Integrate coupling capacitor in double strip design



High sparc immunity expected:
Sparc-charge contained on chamber
Capacitively induced charge clipped by ESD diode on chamber

Model for Dual Strip MM chamber

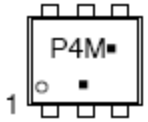


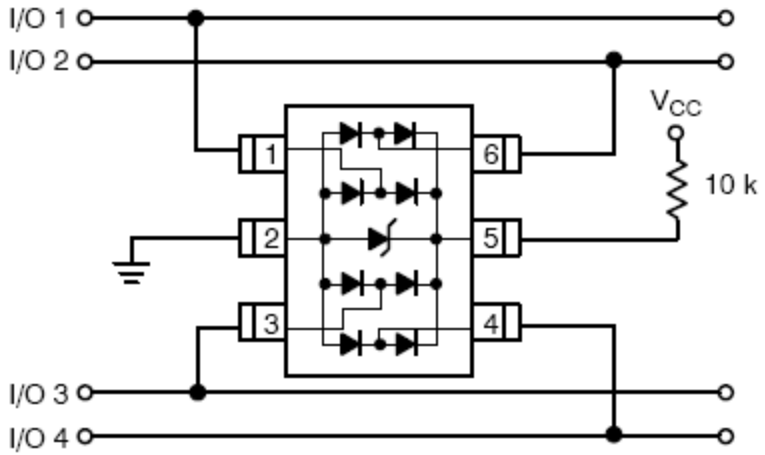
ESD diode arrays

NUP4114UPXV6

SOT–563
CASE 463A

MARKING DIAGRAM



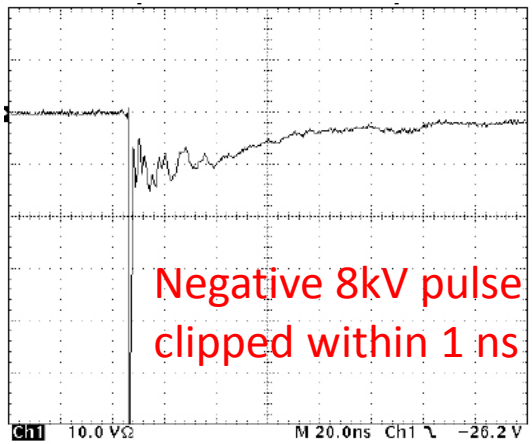


4 channels in 1.6 x 1.6 mm²

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

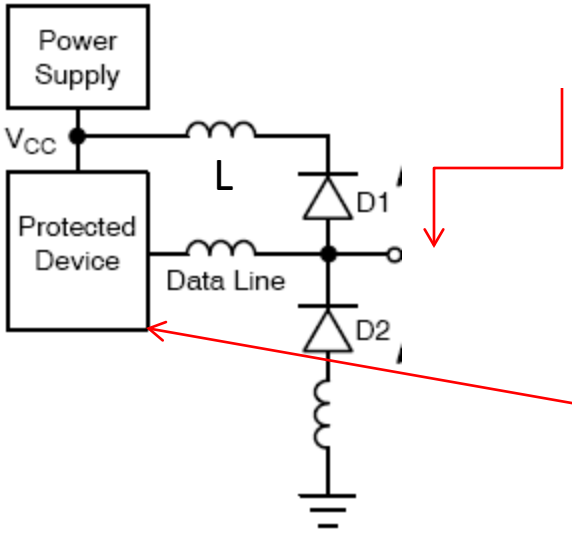
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 1)			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, (Note 2)	6.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5 V			1.0	μA
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.8	1.0	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins		0.4	0.5	pF

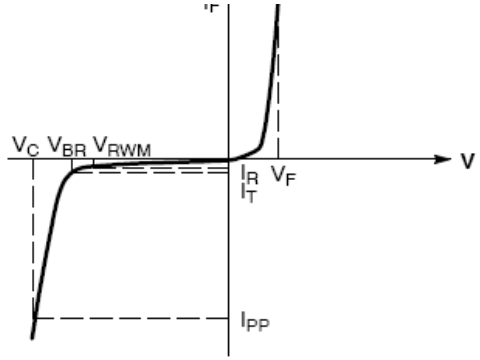
ESD clipping performance



IEC 61000–4–2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



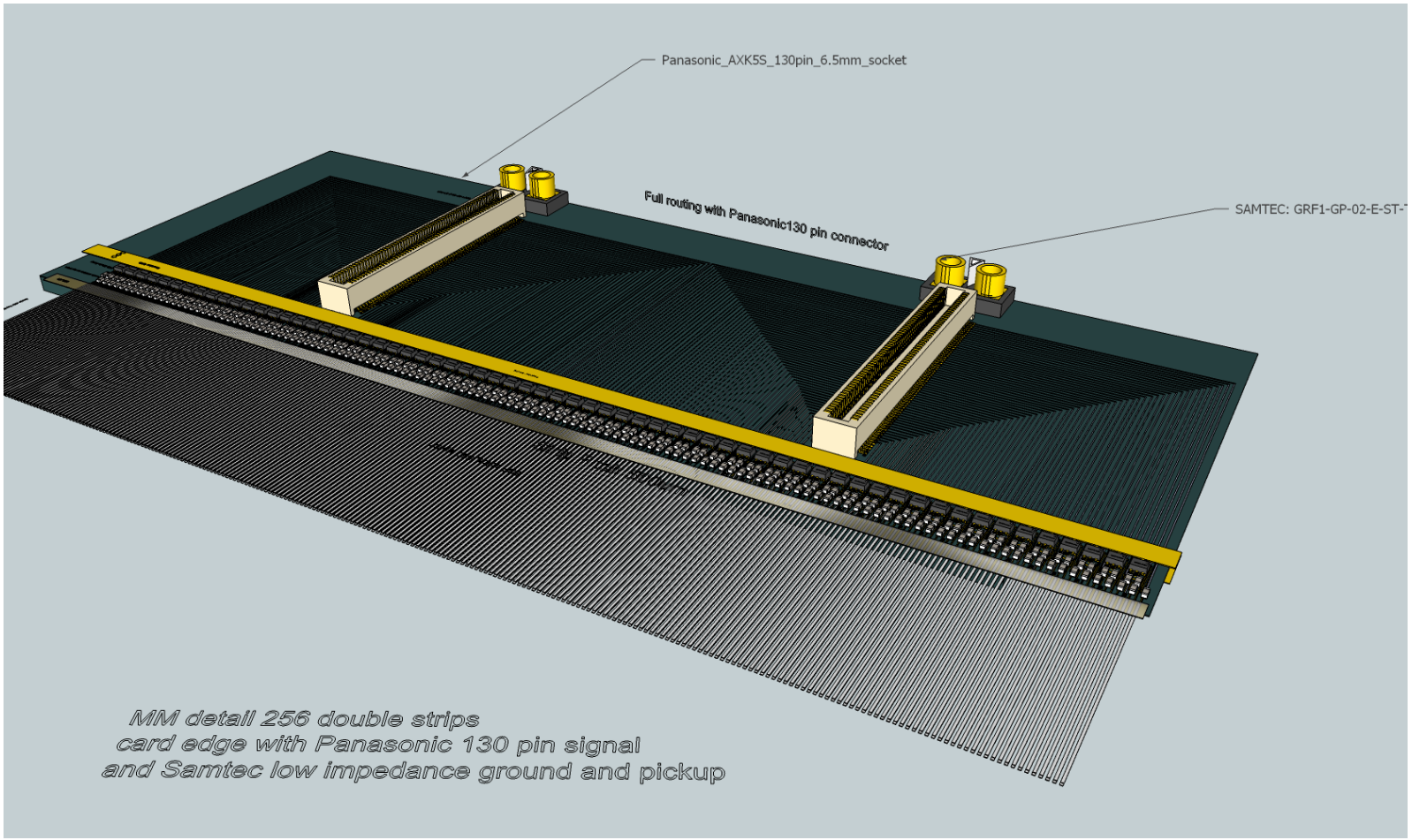


Negative clipped: $V_n = -V_f - L \times dI_{esd}/dt$

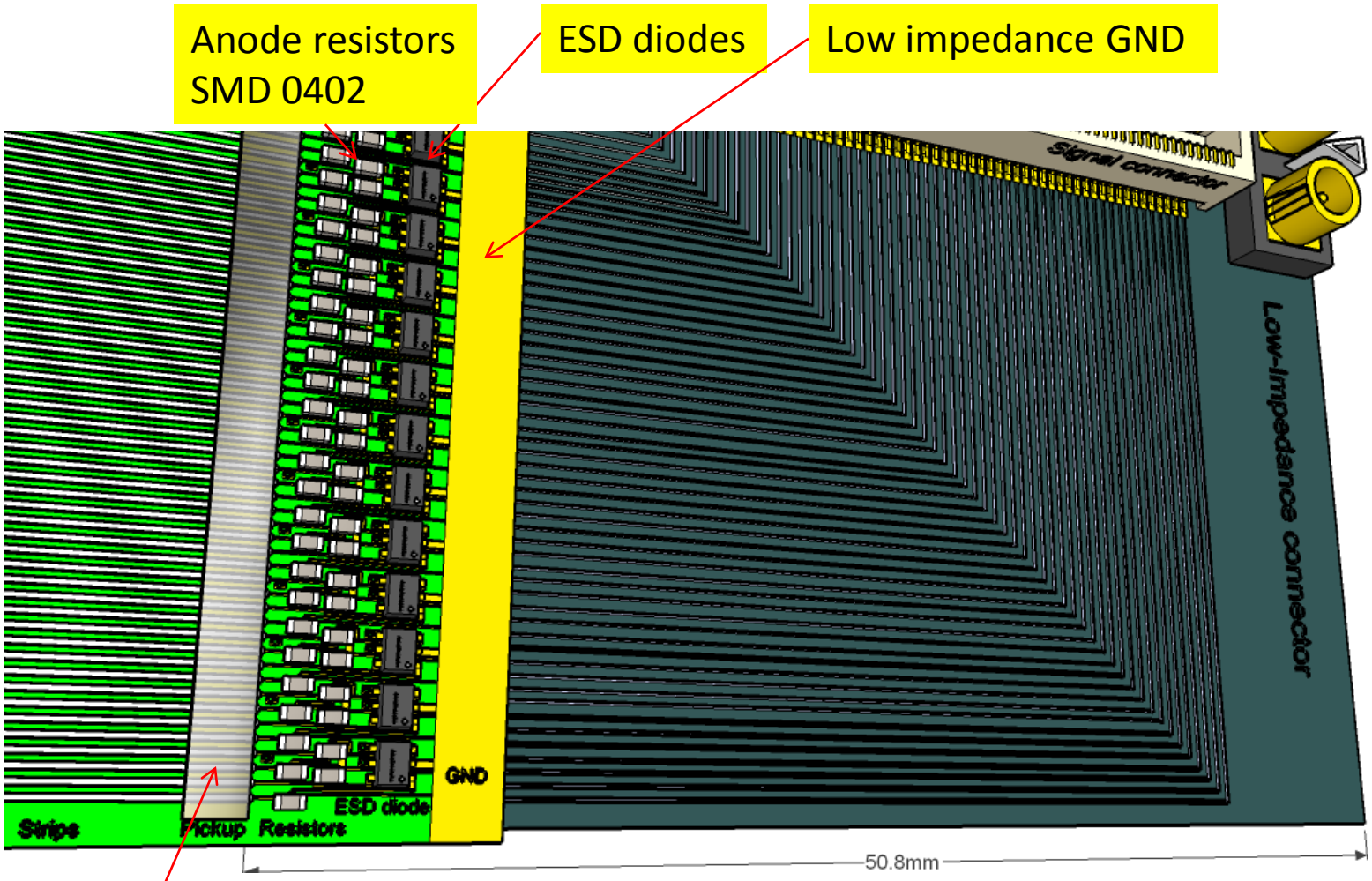
Positive clipped: $V_p = V_{cc} + Vf + L \times dI_{esd}/dt$

Minimize the inductive part L !

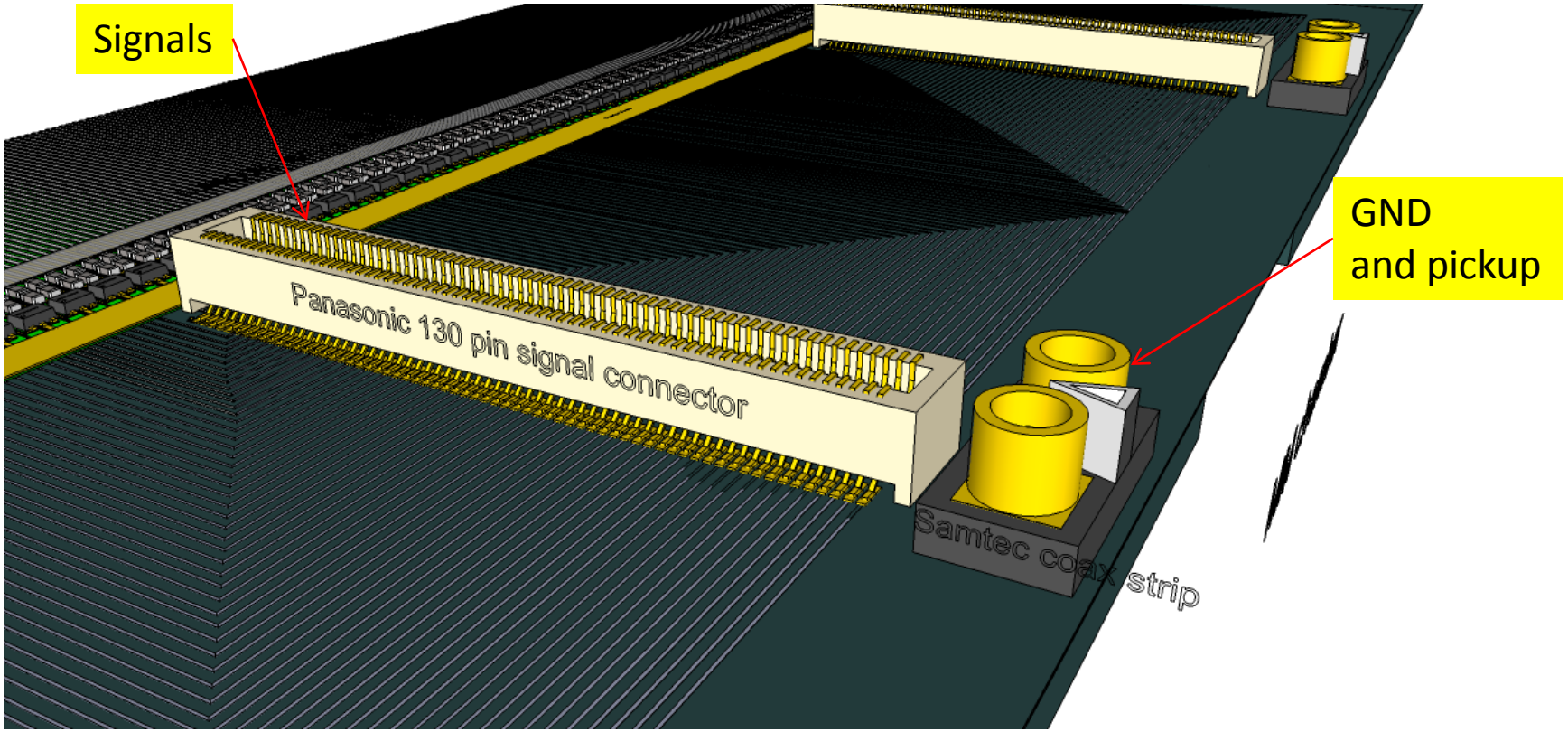
MM chamber edge



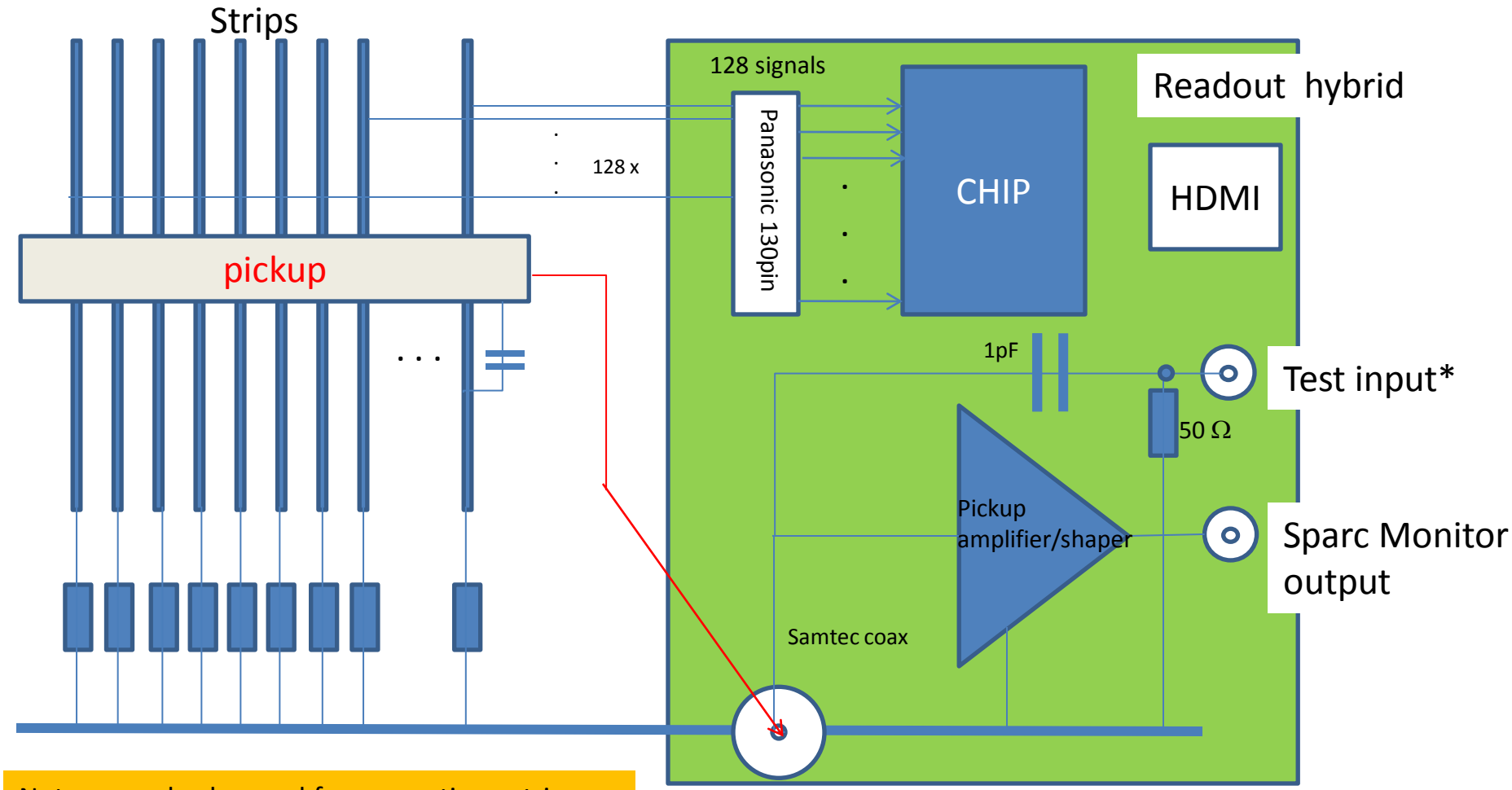
ESD Implementation on chamber



Connectors on chamber



Sparc monitor output and test input (under consideration)



Note: may also be used for generating a trigger
If chamber pulses are sufficiently strong

* Only required if chip has no test feature

Summary

- Vital and Desirable solutions for sparc protection needed

-Component damage protection and readout immunity are vital
-Sparc monitoring and test pulses are desirable

- Discrete protection diodes may work with AC coupling

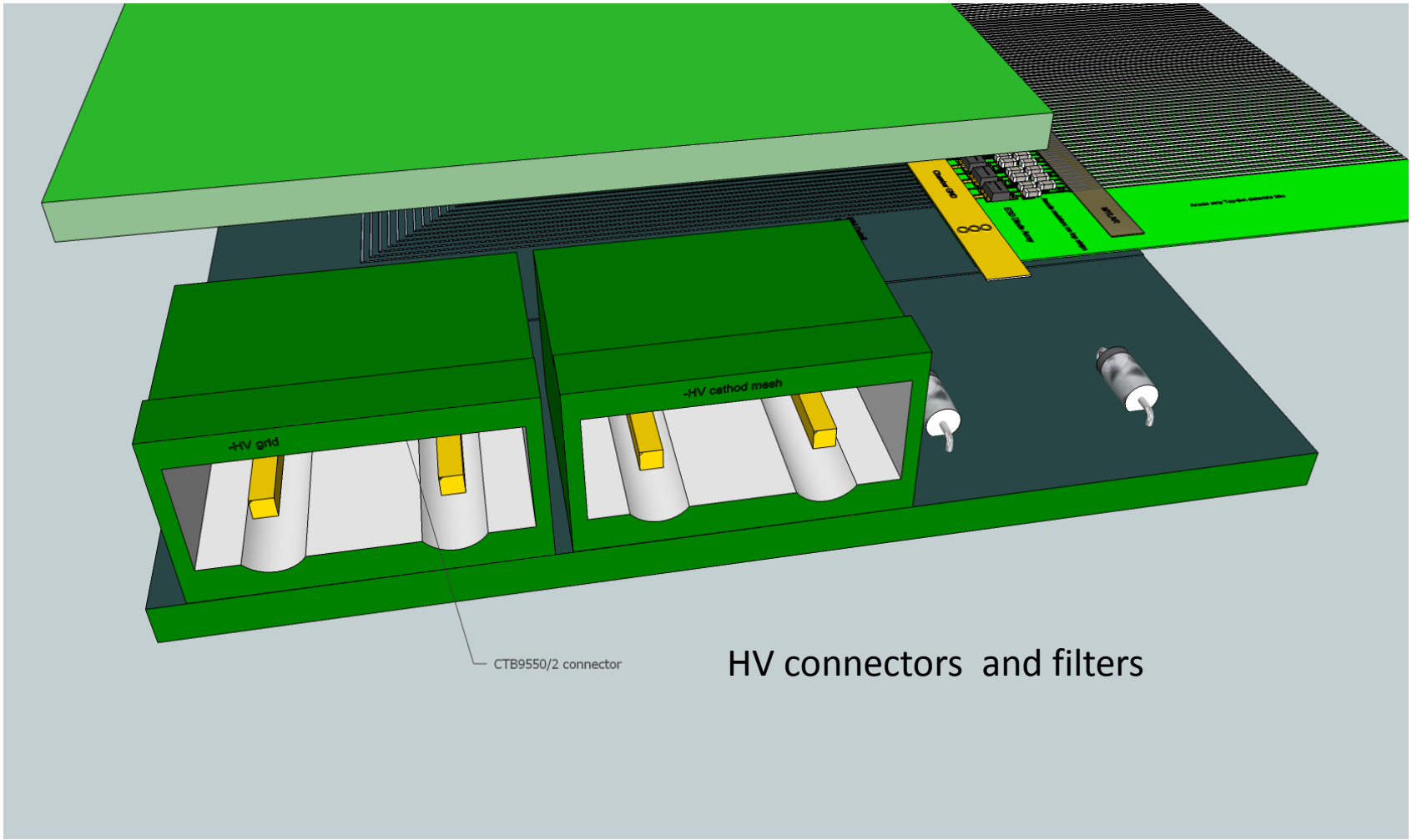
  - but have too much capacitance and reuqire too much space

- New ESD diodes are made for protection and combine a few advantages

  - very low capacitance ~ 1pF
  - very fast ~1ns
  - very small packages ~ 1.5 mm2
  - better than IEC standard ESD protection

- Implementation requires low impedance ground and V_{cc} bias
- MM chamber layout exercise with ESD, R and dual strip looks OK
- Sparc monitoring and test signals look like an easy addition

Backup



HV connectors and filters

X-ray though MM edge and carrier