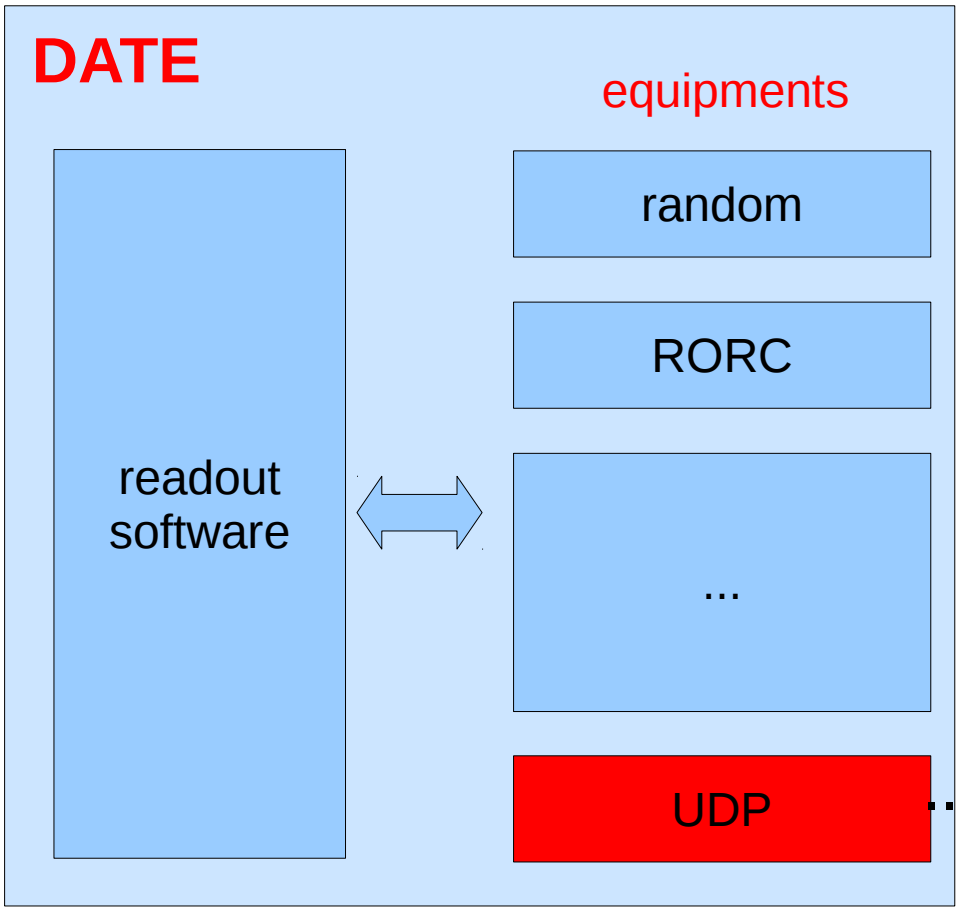
Porting the DATE detector readout to GbE

Filippo Costa

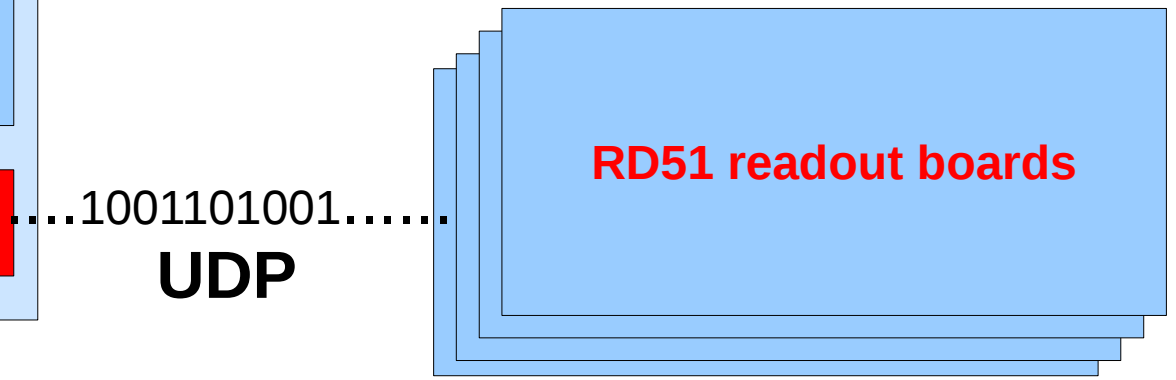
OUTLINE

- ✗ DATE and the UDP readout.
- ✗ Data format.
- ✗ Test with the UDP using a software generator.
- ✗ Test with the UDP using a readout board prototype.
- ✗ SLOW control, first ideas.
- ✗ To be done.

Between DATE and RD51 there are a lot of UDP packets

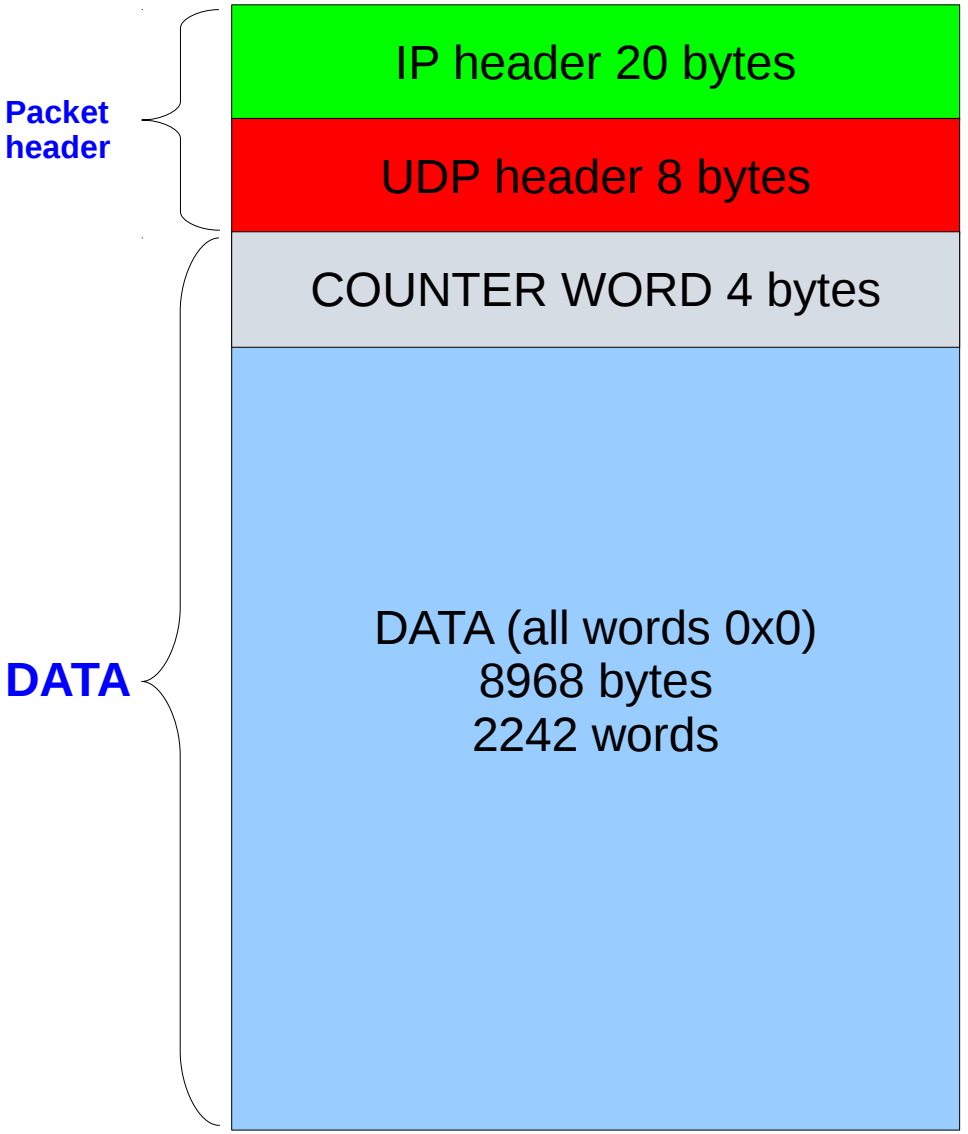


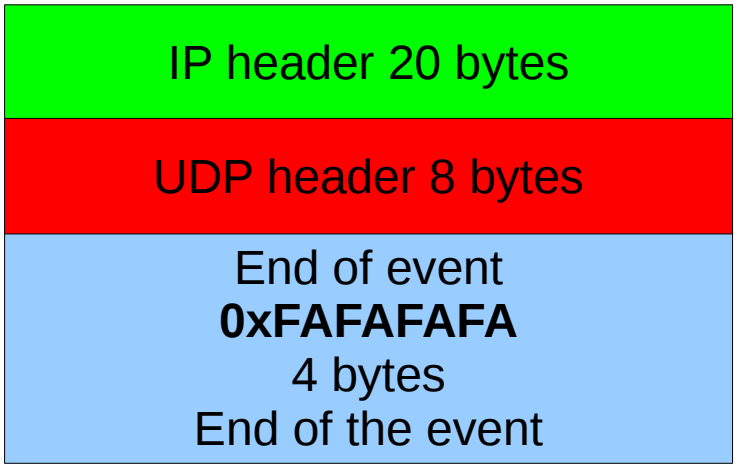
- **DATE** will receive data from the **RD51 readout boards** using an **Ethernet socket**.
- A new **equipment** for **DATE** has been developed to receive data through the Ethernet socket.
- The data will be prepared and sent as **UDP packets**.



DATA FORMAT

UDP datagram of 9KB

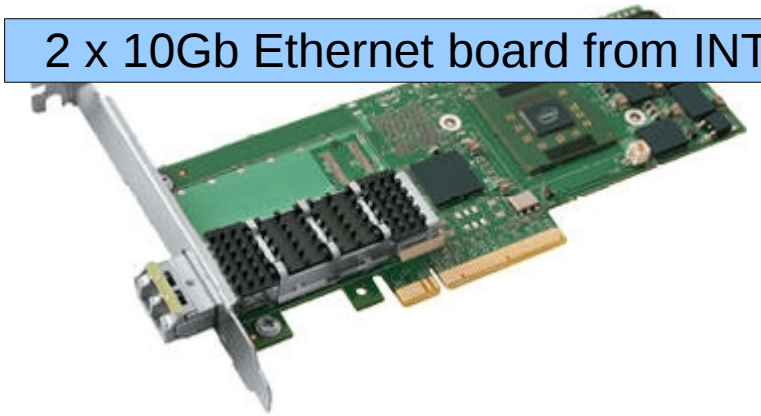


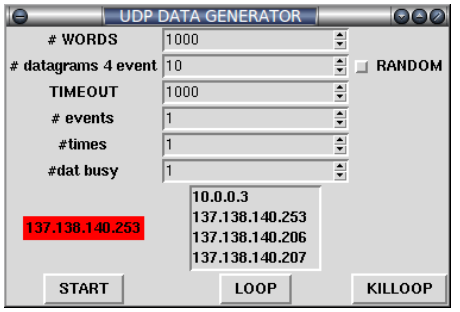


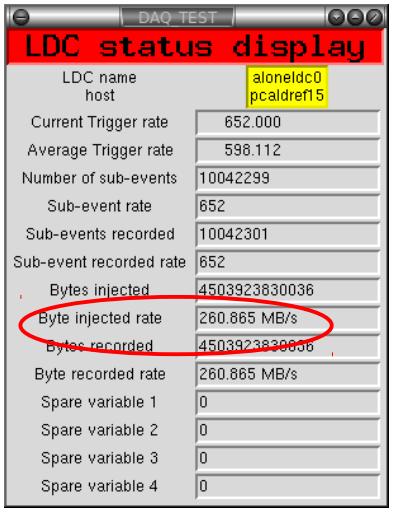
- The **COUNTER WORD** is used to check if during the data transmission there were duplicate or lost packets.
- The event is closed when **DATE** receives and recognizes the word **0xFAFAFAFA**

TEST setup … via software (10Gb Ethernet)

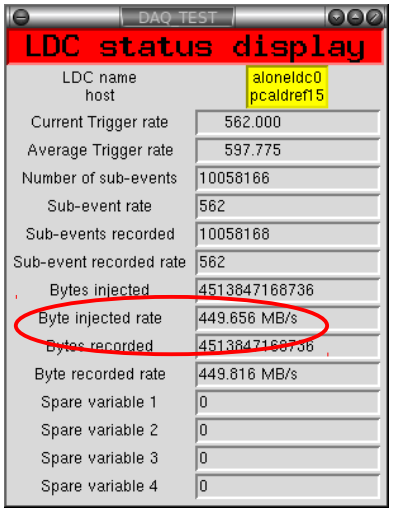
2 x 10Gb Ethernet board from INTEL



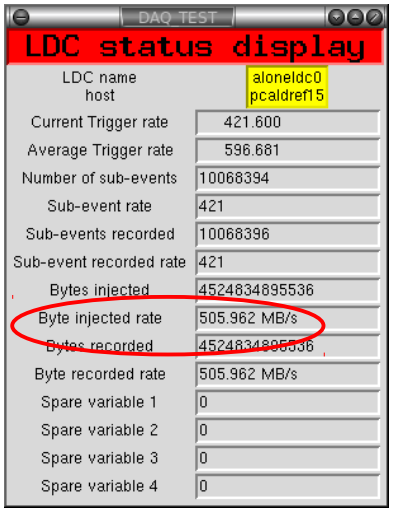




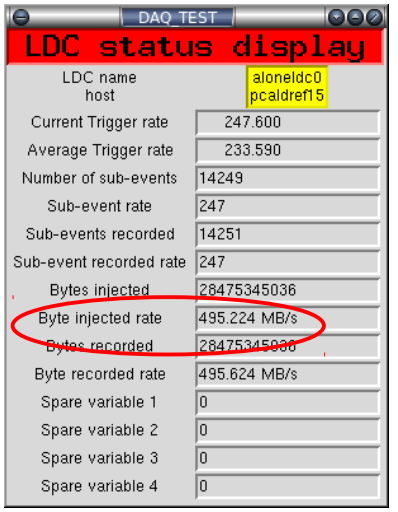
Using UDP packet of 8000 byte
Event size 400100 Bytes



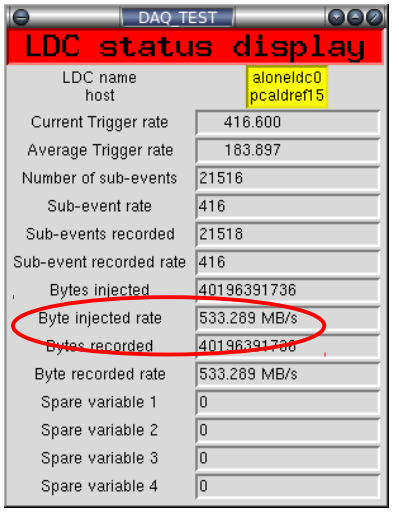
Using UDP packet of 16000 byte
Event size 800100 Bytes



Using UDP packet of 24000 byte
Event size 1200100 Bytes



Using UDP packet of 40000 byte
Event size 2100000 Bytes

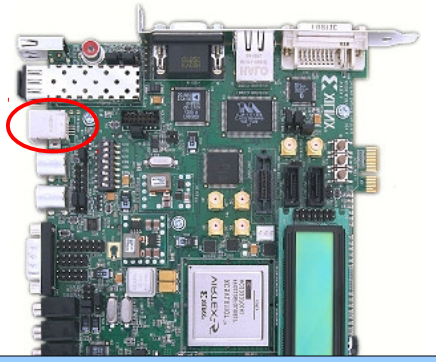


Using UDP packet of 64000 byte
Event size 1280100 Bytes

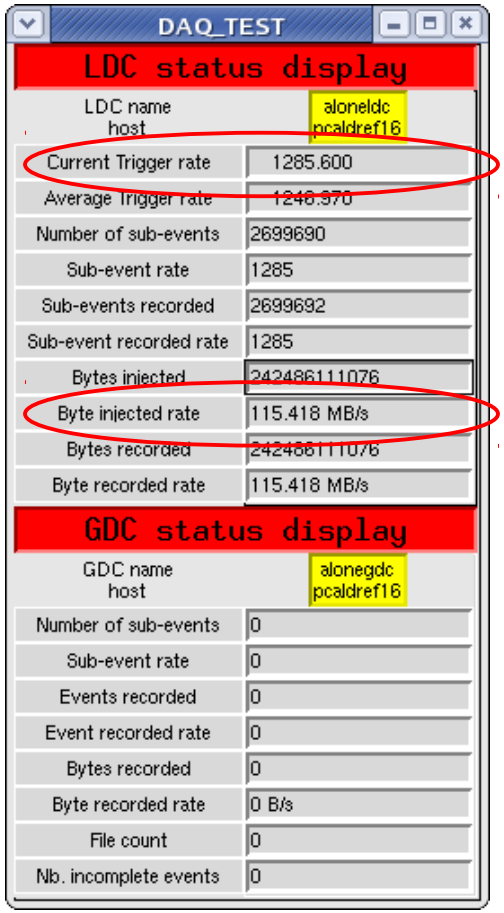
Conclusions : with packets of 9KB I obtained a throughput of ~300 MB/s

Test setup using a prototype readout board

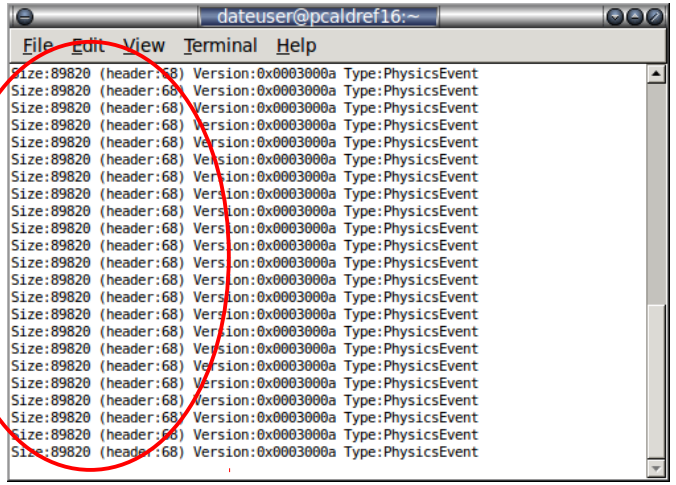
1 Gb



Firmware by
Alfonso Tarazona Martinez

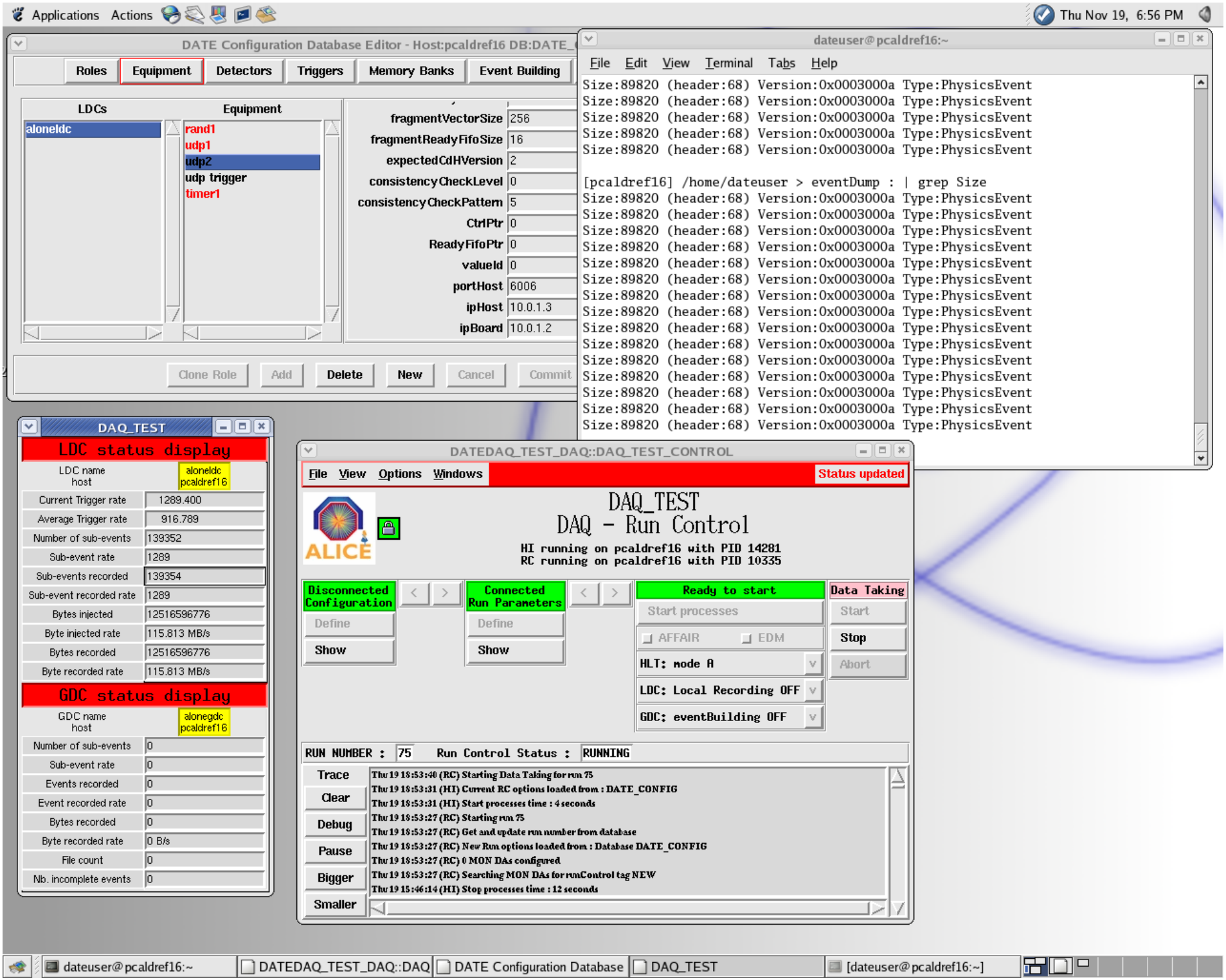


Size of the UDP packets: **9000 bytes**
MTU of the Ethernet card: **9000 bytes**
Event size: **10 packets per events → 89820 bytes**

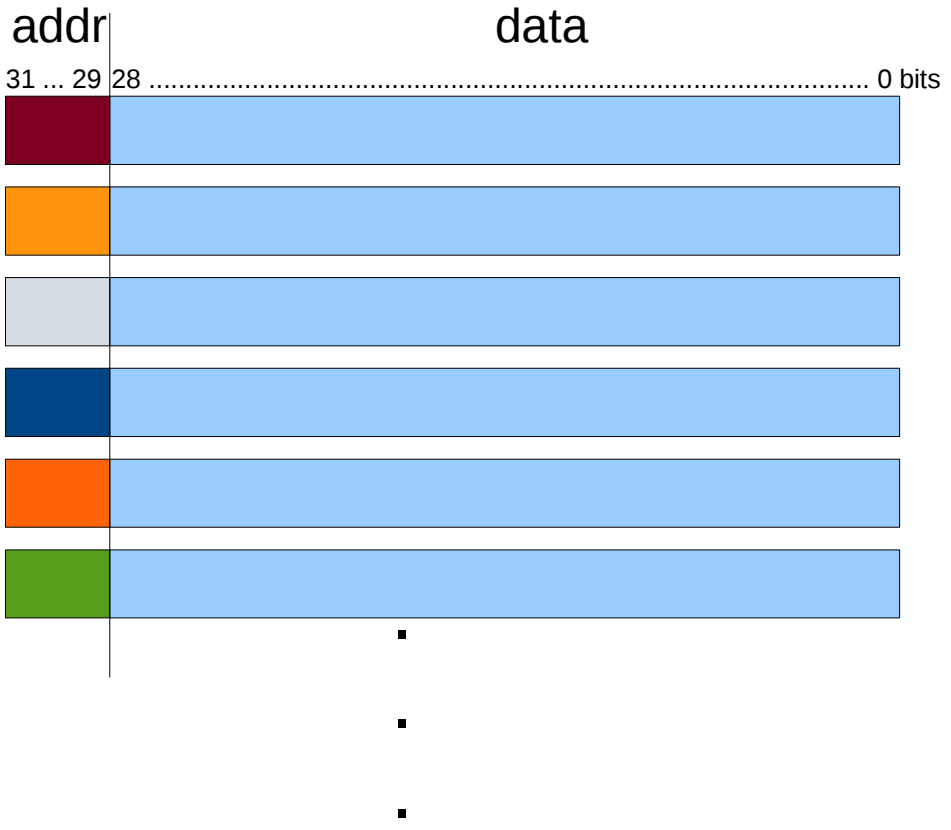


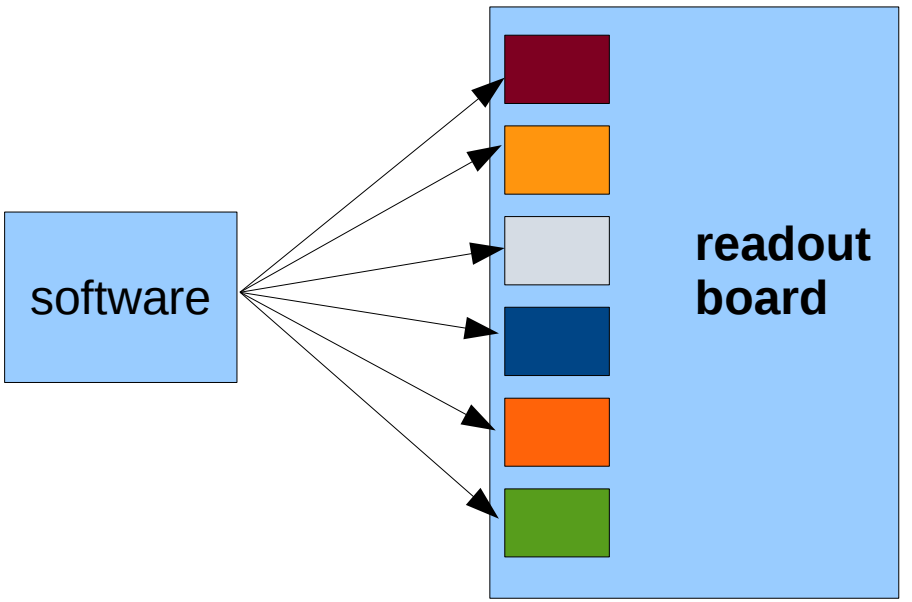
Readout board prototype based on a **Xilinx Virtex5** demo board

Using this configuration we have *tuned* the system to go as fast as possible reaching for the time being **120/124 MB/s** using event size of **89820 bytes (~75 M events – no errors)**


Applications Actions
Thu Nov 19, 6:56 PM
DATE Configuration Database Editor - Host:pcaldref16 DB:DATE_
Roles
Equipment
Detectors
Triggers
Memory Banks
Event Building
LDCs
Equipment
aloneldc
rand1
udp1
udp2
udp trigger
timer1
fragmentVectorSize 256
fragmentReadyFifoSize 16
expectedCdHVersion 2
consistencyCheckLevel 0
consistencyCheckPattern 5
CtrlPtr 0
ReadyFifoPtr 0
valueId 0
portHost 6006
ipHost 10.0.1.3
ipBoard 10.0.1.2
Clone Role
Add
Delete
New
Cancel
Commit
dateuser@pcaldref16:~
File Edit View Terminal Tabs Help
Size:89820 (header:68) Version:0x0003000a Type:PhysicsEvent
[pcaldref16] /home/dateuser > eventDump : | grep Size
DAQ_TEST
LDC status display
LDC name
host
aloneldc
pcaldref16
Current Trigger rate 1289.400
Average Trigger rate 916.789
Number of sub-events 139352
Sub-event rate 1289
Sub-events recorded 139354
Sub-event recorded rate 1289
Bytes injected 12516596776
Byte injected rate 115.813 MB/s
Bytes recorded 12516596776
Byte recorded rate 115.813 MB/s
GDC status display
GDC name
host
alonegdc
pcaldref16
Number of sub-events 0
Sub-event rate 0
Events recorded 0
Event recorded rate 0
Bytes recorded 0
Byte recorded rate 0 B/s
File count 0
Nb. incomplete events 0
DATEDAQ_TEST_DAQ::DAQ_TEST_CONTROL
File View Options Windows
Status updated
ALICE
DAQ_TEST
DAQ - Run Control
HI running on pcaldref16 with PID 14281
RC running on pcaldref16 with PID 10335
Disconnected Configuration
Define
Show
Connected Run Parameters
Define
Show
Ready to start
Start processes
AFFAIR EDM
HLT: mode A
LDC: Local Recording OFF
GDC: eventBuilding OFF
Data Taking
Start
Stop
Abort
RUN NUMBER : 75
Run Control Status : RUNNING
Trace
Clear
Debug
Pause
Bigger
Smaller
Thu 19 18:53:40 (RC) Starting Data Taking for run 75
Thu 19 18:53:31 (HI) Current RC options loaded from : DATE_CONFIG
Thu 19 18:53:31 (HI) Start processes time : 4 seconds
Thu 19 18:53:27 (RC) Starting run 75
Thu 19 18:53:27 (RC) Get and update run number from database
Thu 19 18:53:27 (RC) New Run options loaded from : Database DATE_CONFIG
Thu 19 18:53:27 (RC) 0 MON DAs configured
Thu 19 18:53:27 (RC) Searching MON DAs for runControl tag NEW
Thu 19 15:46:14 (HI) Stop processes time : 12 seconds
dateuser@pcaldref16:~
DATEDAQ_TEST_DAQ::DAQ
DATE Configuration Database
DAQ_TEST
[dateuser@pcaldref16:~]

SLOW CONTROL (work in progress 2 IDEAS)





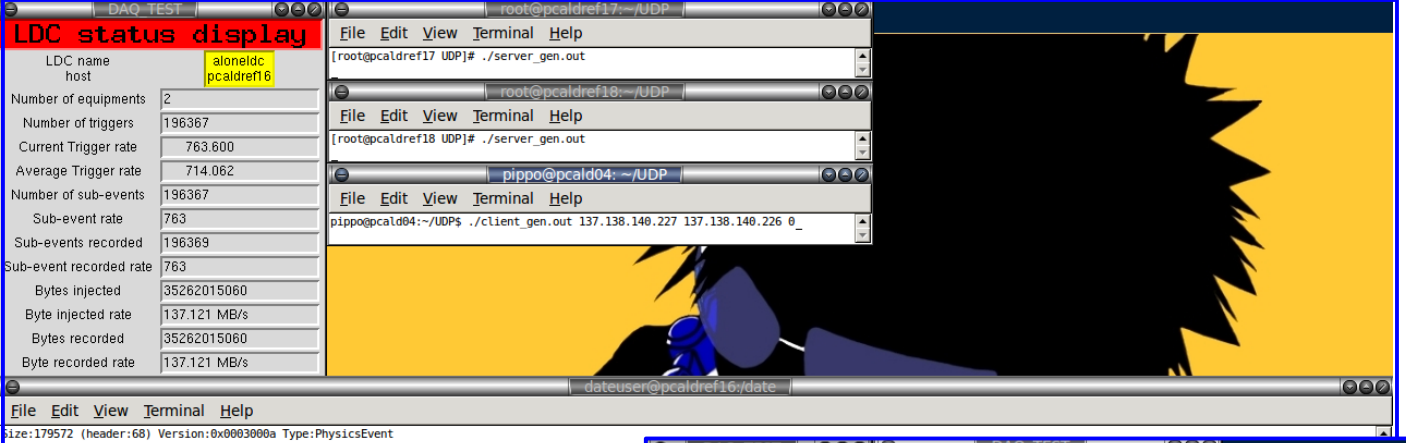
This solution is easy to implement via software but difficult to implement via VHDL. 29 bits of data is not a standard word and the board has to merge the information before analyzing the data.

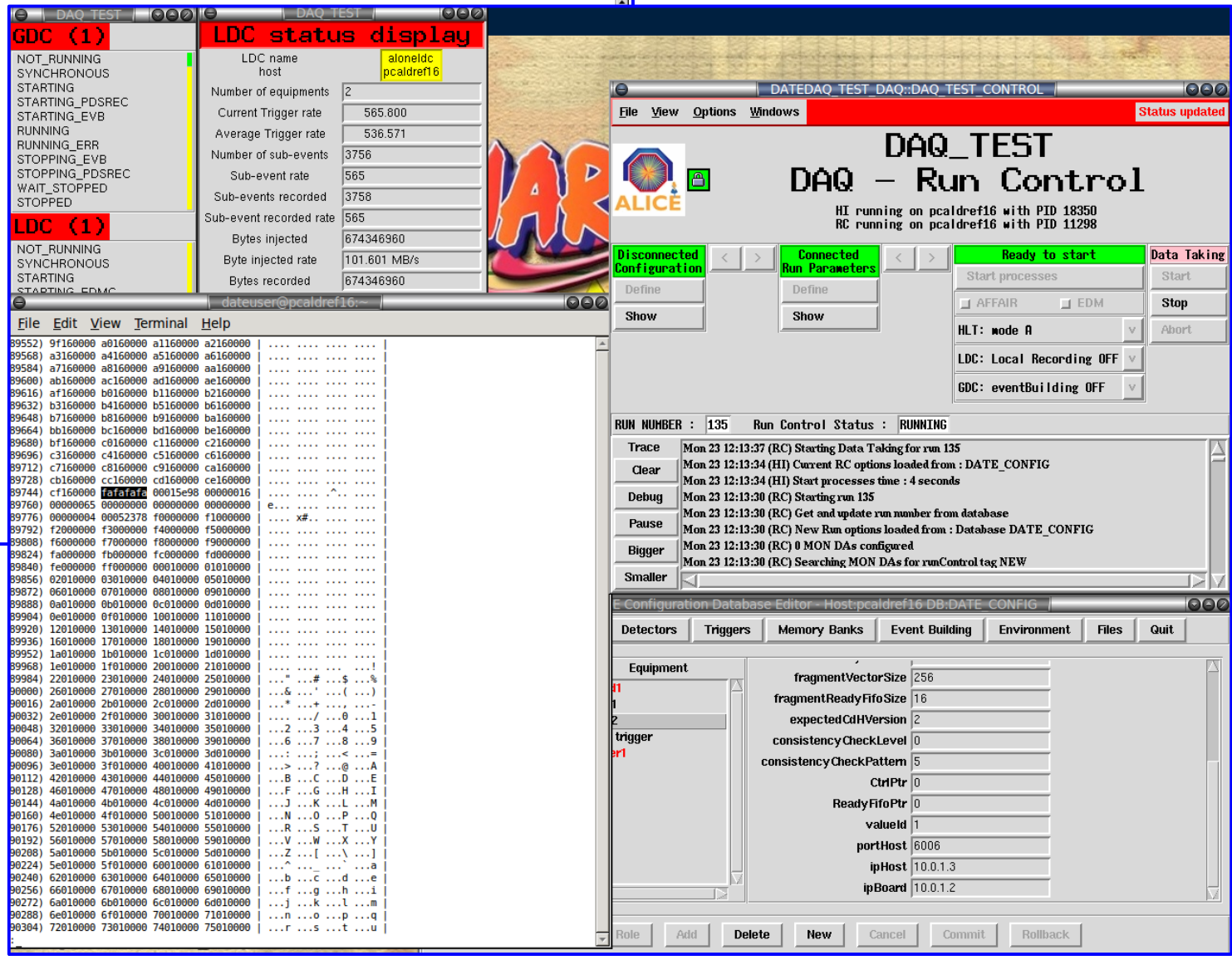
BETTER IDEA?

The readout board can define several ports (one for each service), the software will send 32 bits of data to the different ports. The board as soon as it receives a packet it stores the information in different FIFOs (connected to the ports) and it analyzes them when the communication ends.

What must be TESTED/ DONE next ?

- ✗ Data acquisition with two boards at the same time
  (some tests have been already performed using the software UDP generator … see next slide).
- ✗ Higher throughput using socket with higher bandwidth.
- ✗ Checks, checks and checks for the data quality.
- ✗ …
- ✗ Anything else you want to test.





SOFTWARE
HARDWARE
GENERATOR

THANK YOU