# MSGCROC – an ASIC for high count rate readout of position sensitive gas chambers

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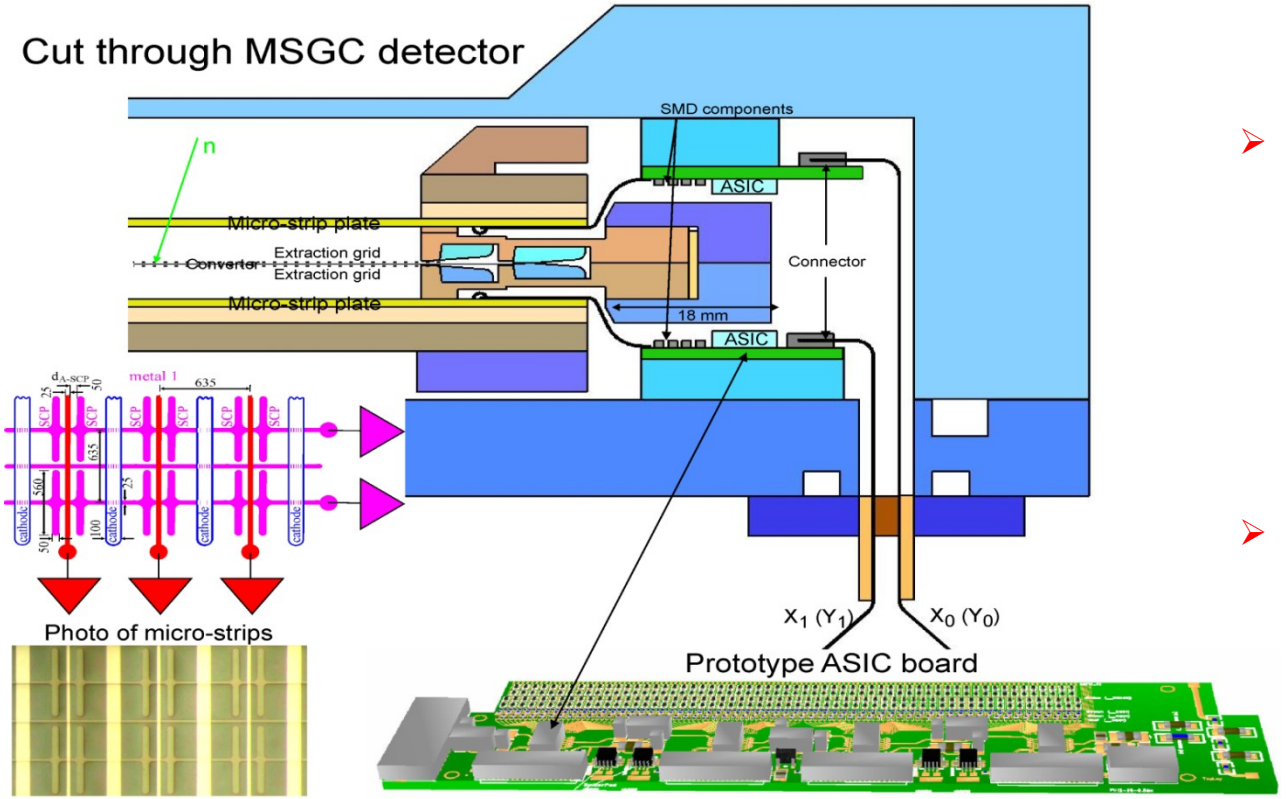
MSGCROC – Micro-Strip Gas Chamber ReadOut Chip

# Outlook

- General overview
  - $^{157}$Gd/CsI MSGC – neutron-sensitive detector
  - MSGCROC chip
  - DAQ System
  - DAQ Software
- Details of MSGCROC chip
  - Requirements concerning the detector and the readout electronics
  - Details of the ASIC circuitry
  - Test measurements
    - Internal calibration
    - Measurements with Si detector

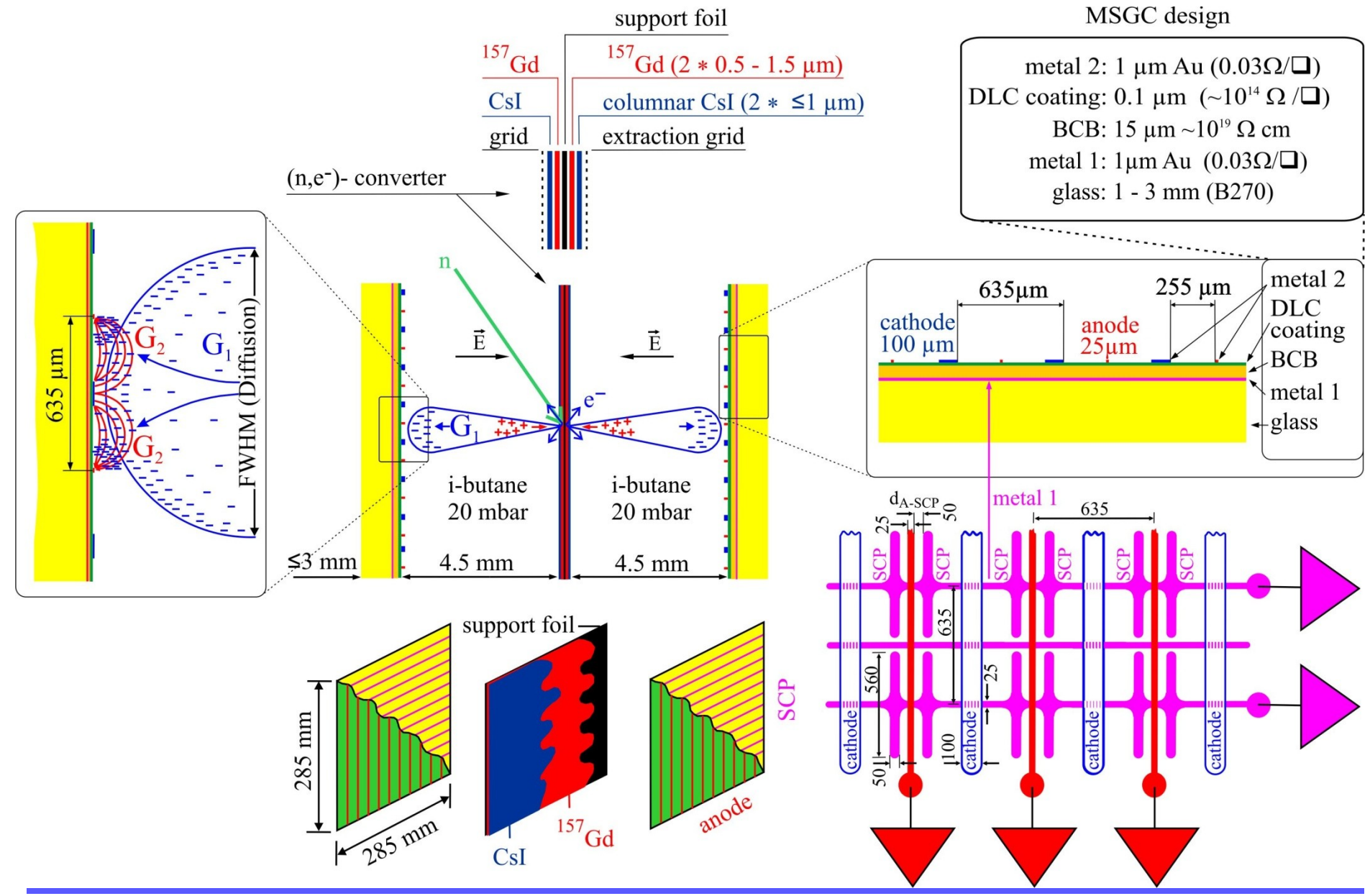
# $^{157}$Gd/CsI hybrid low-pressure 2D MSGC detector

Developed in Berlin by:
S. Alimov, B. Gebauer, Ch. Schulz, T. Wilpert

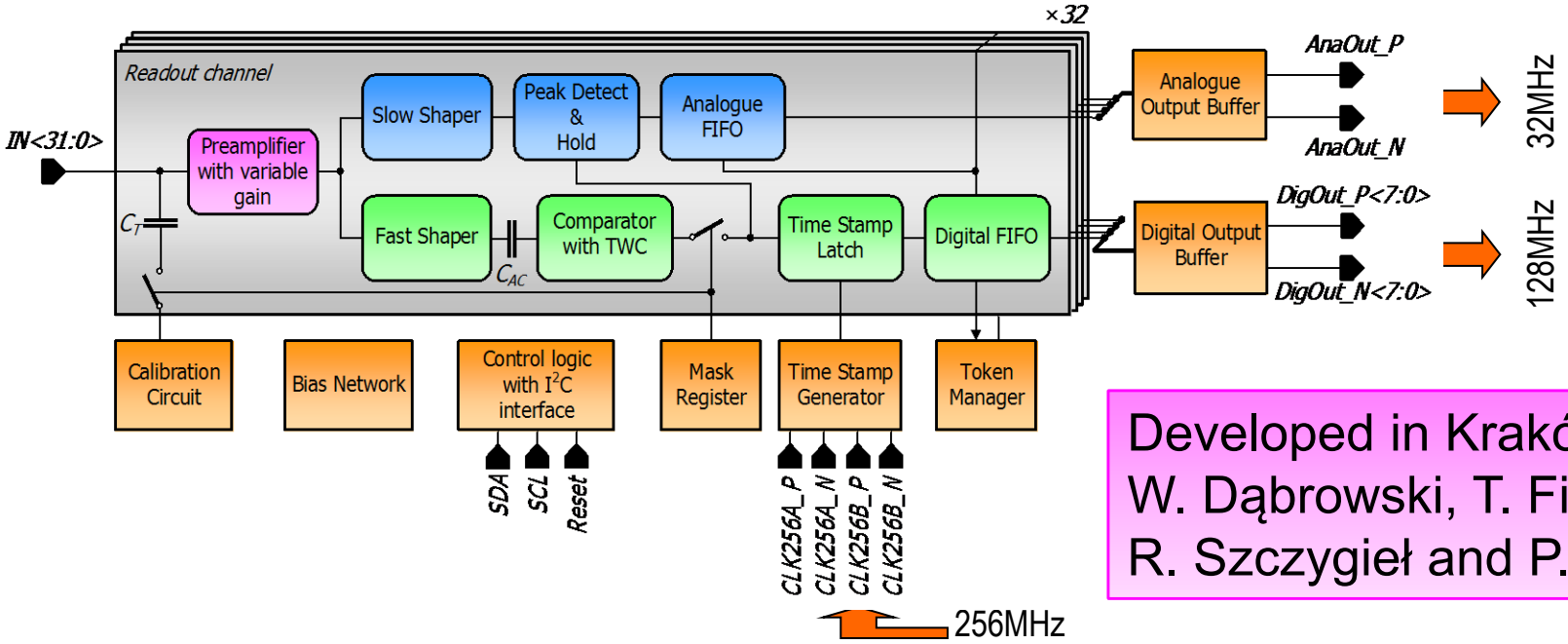



- Composite $^{157}$Gd/CsI neutron converter foil, on negative electrical potential with extraction grids on either side, located in the central detector plane
- Two adjacent low-pressure (p~20mbar) preamplification gas gaps on either side of the converter followed by amplification at constant reduced field strength E/p
- Two micro-strip gas detector planes, which function as third amplification and readout elements (400 stripes per detector module).

# MSGC detector details

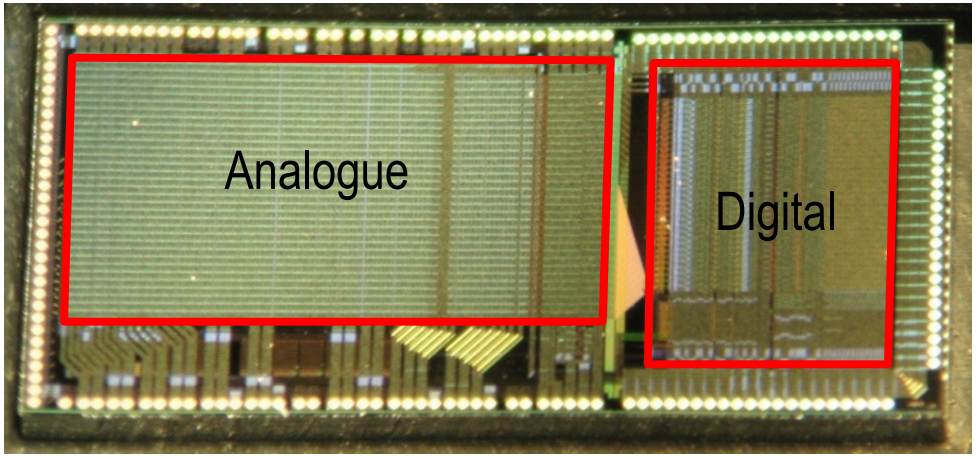


# MSGCROC architecture




Developed in Kraków by:
W. Dąbrowski, T. Fiutowski,
R. Szczygieł and P. Wiącek

3.2x6.7 mm$^2$




0.35 μm CMOS process from Austria Microsystems

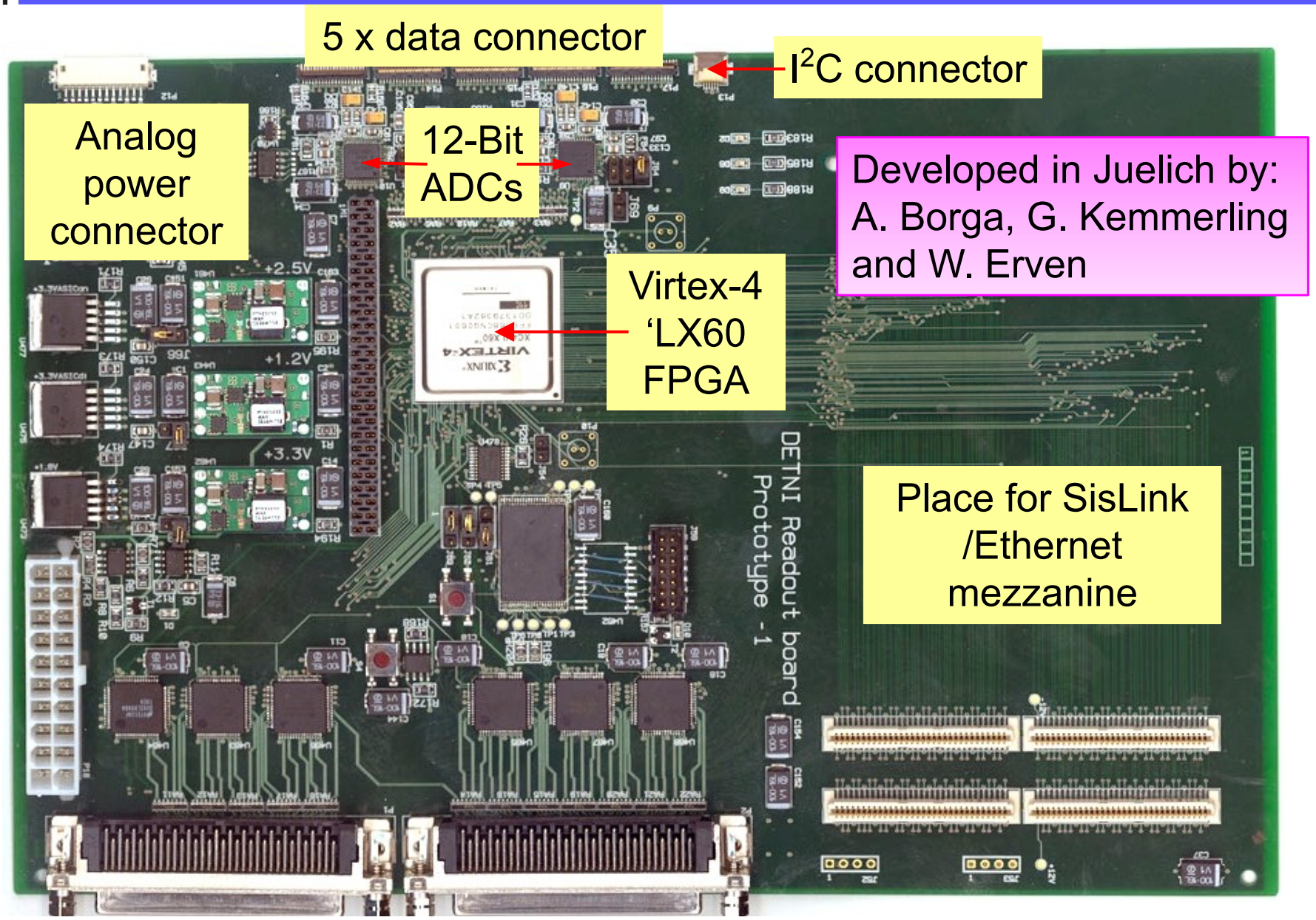
Input device: PMOS 2368μm/0.4 μm

Bias current of the input transistor: 2.36mA (nominal)

Power consumption ~25 mW/channel (@ 3.3 V)

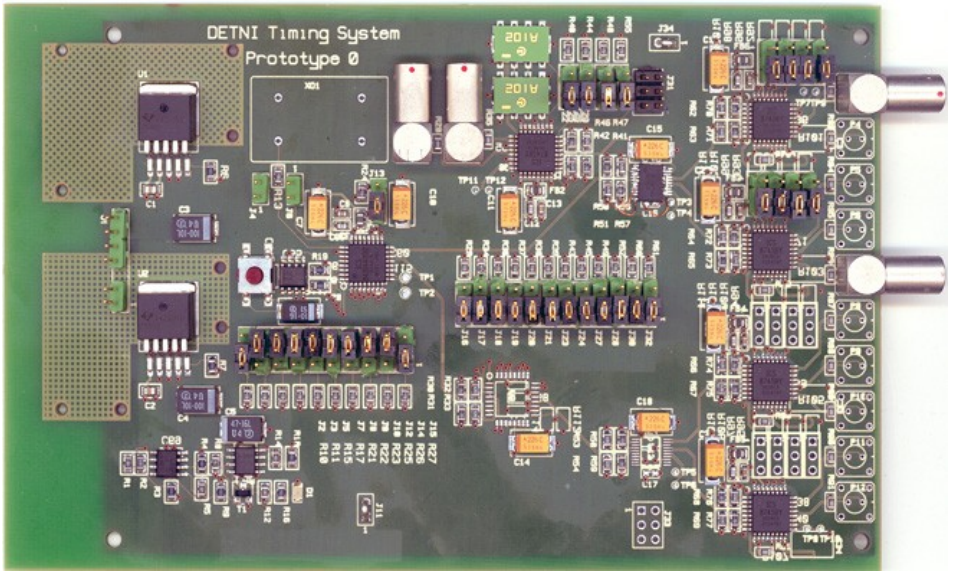
Separated analogue and digital power supply

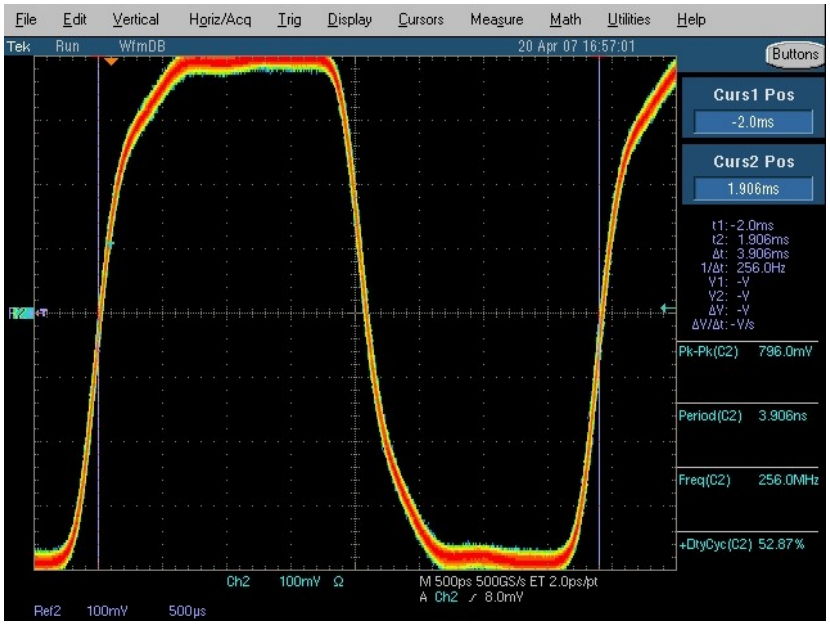
# ADC-FPGA prototype board

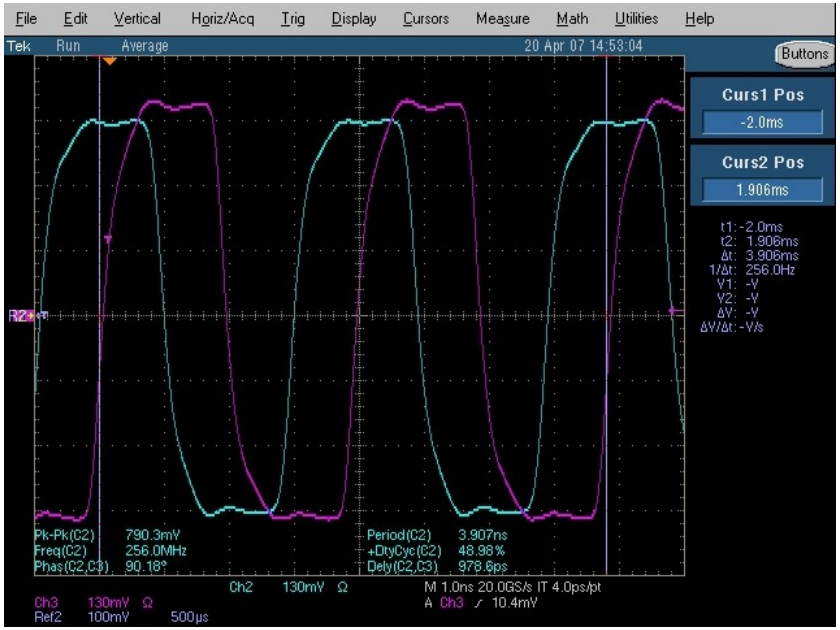


# Prototype of clock distribution board

- Master reference frequency 32 MHz
- Clock outputs:
  - 5 x 256 MHz
  - 5 x 256 MHz 90° phase shifted
- 30 ps max. cycle-to-cycle Jitter

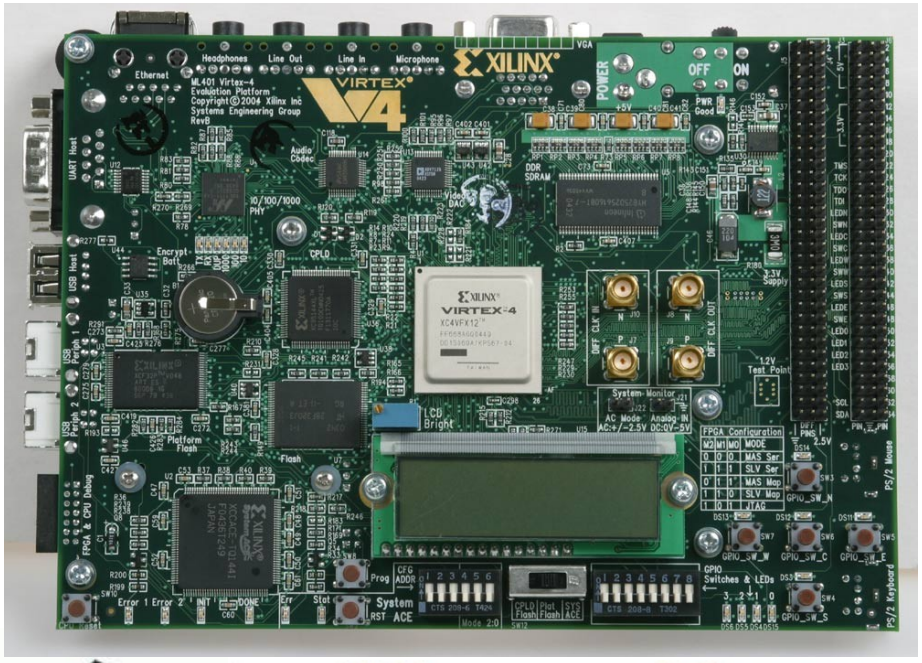


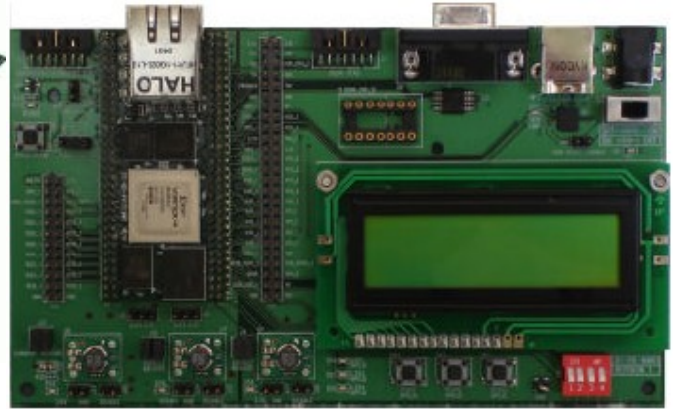



# Ethernet readout

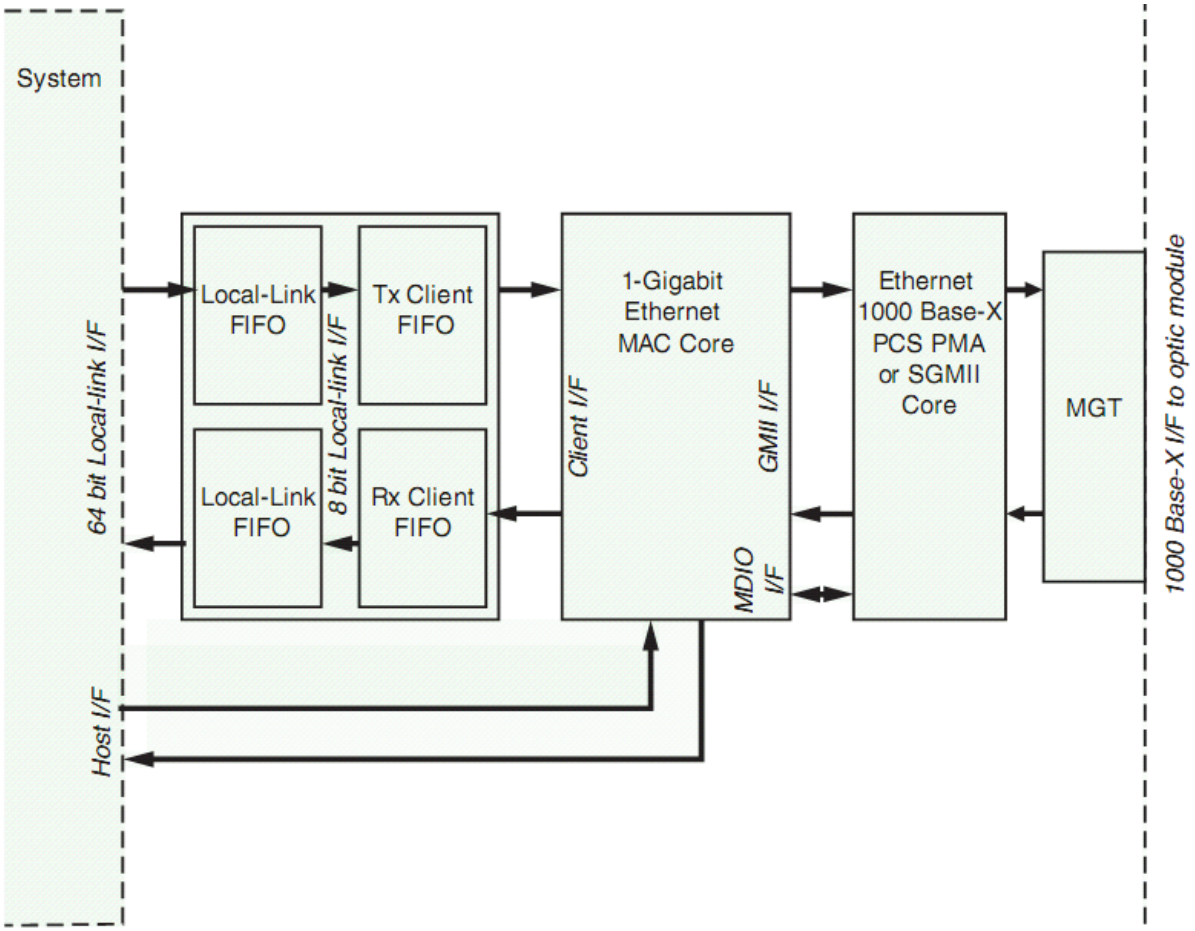
- Xilinx ML403 Evaluation Board
  - Board use for developmetn
  - (top)
- Memec Virtex-4 FX12 Mini-Module
  - Shown with its base board
  - Will be used as replacement of SisLink
  - (bottom right)
- NIC
  - SK-9E21 10/100/1000 Base-T Server Adapter
  - (bottom left)



# Code for Ethernet readout

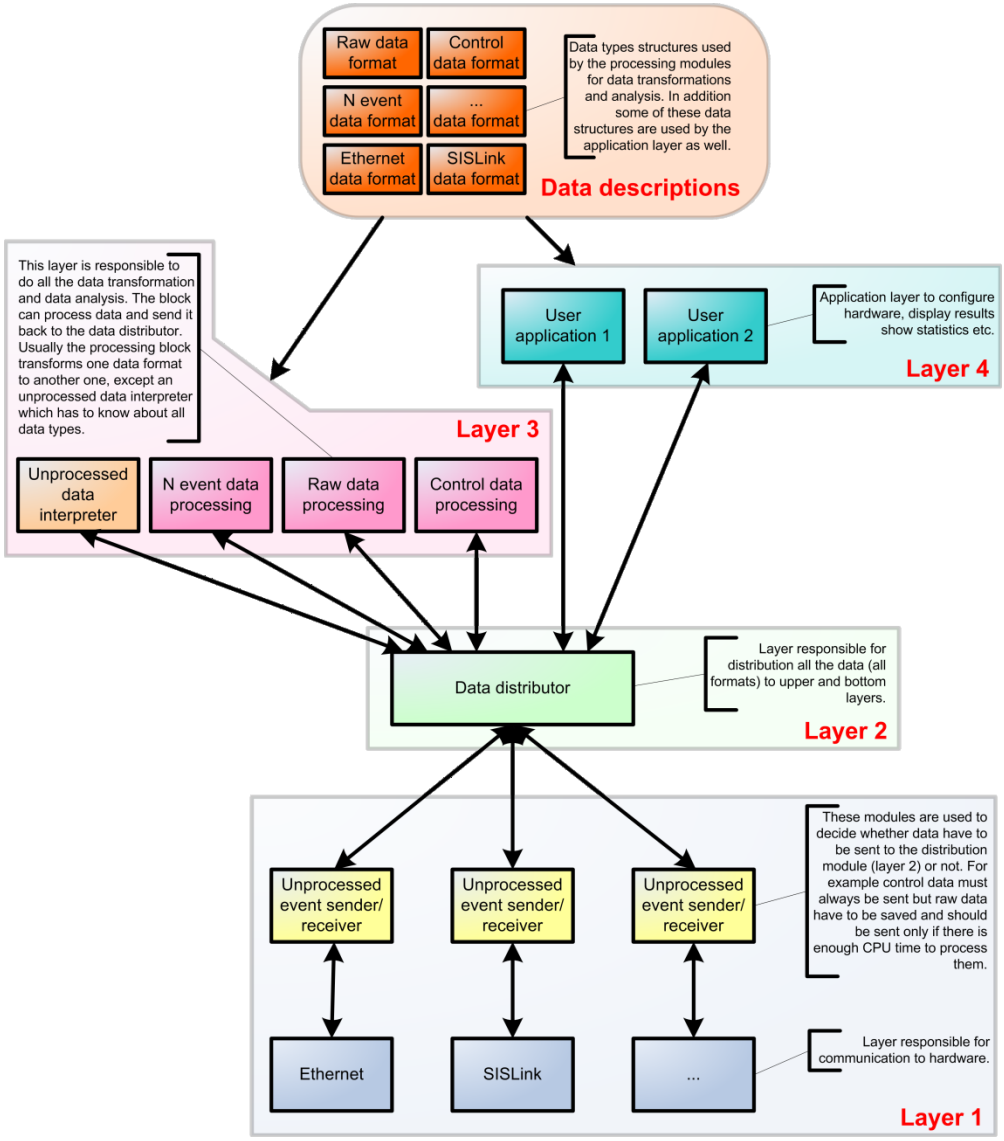
- Built on top of Ethernet Mac Wrapper IP core using Verilog
- Using custom protocol or Raw Ethernet Frames
- Driver for Linux almost ready working with full speed
- Driver for Windows under the development



# DAQ Software – layered concept

DAQ Software is structured in four layers:

- **Layer 1** - connection to the hardware (possible different types)
- **Layer 2** - data distribution to the processing modules
- **Layer 3** – includes data processing modules
- **Layer 4** - data visualization and overall system configuration (application level)

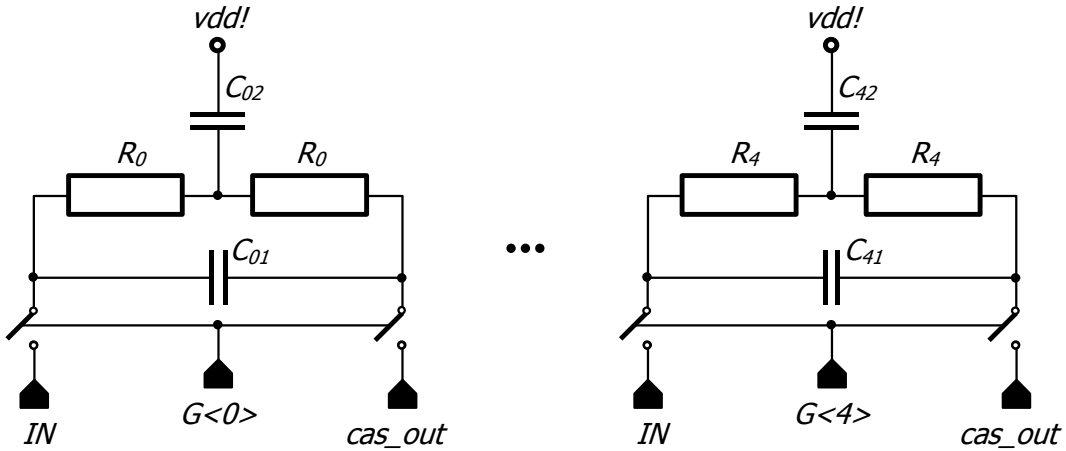


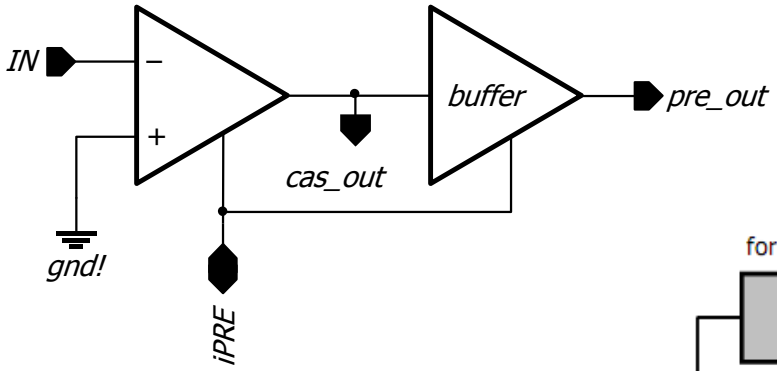
# MSGCROC

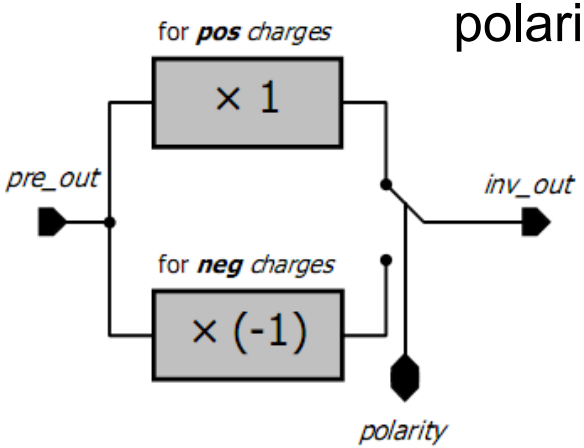
# MSGCROC – requirements

- Signal parameters to be measured:
  - position X/Y, time T, energy (amplitude) EX/EY
- Detector strip capacitance: ~ 23 pF
- The preamp-shaper circuit must be compatible with positive and negative signal polarities
- Input signal charge: $2 \cdot 10^5$ $e^-$ (32fC) - $5 \cdot 10^6$ $e^-$ (800fC) (depending on the detector gas amplification)
- Variable gain in a range 1 - 20 to cope with different detector gas amplification factors
  - Gain factors: ×1, ×2, ×4, ×8, and ×16
- Hit rate per strip: ~ $9 \cdot 10^5$ /s (global count rate: $10^8$ /s)
- X/Y coincidence window 2 ns + (EX = EY)
- Discriminator: time walk < 2 ns, jitter < 2 ns FWHM
- The data must be buffered and derandomized on the ASIC
  - 4 - bit FIFO analogue and digital
- Zero suppression must be performed on the ASIC
- The ASIC must generate a self trigger for each event

# Input stage

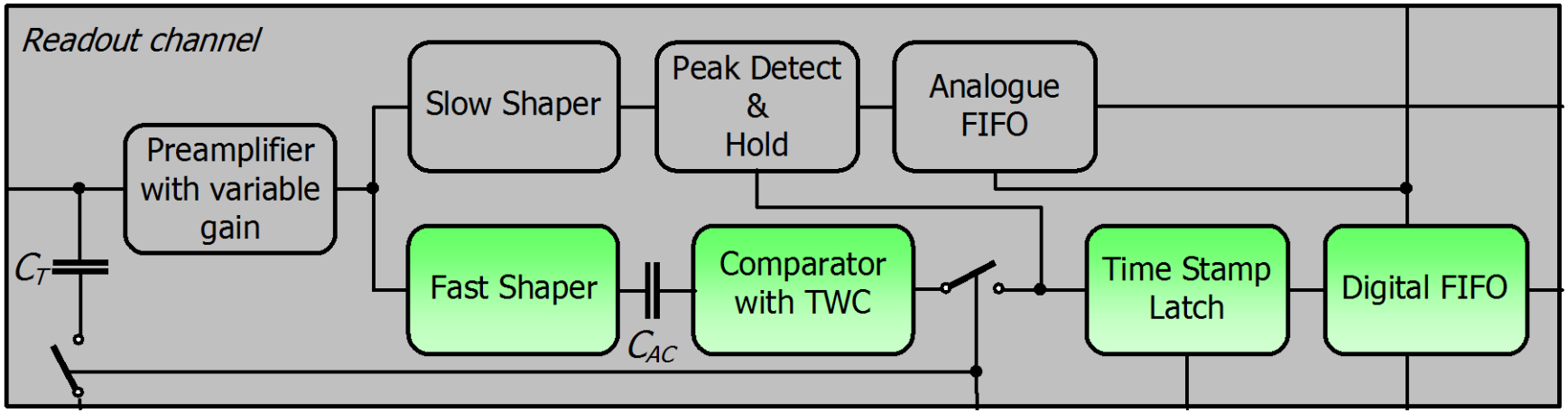


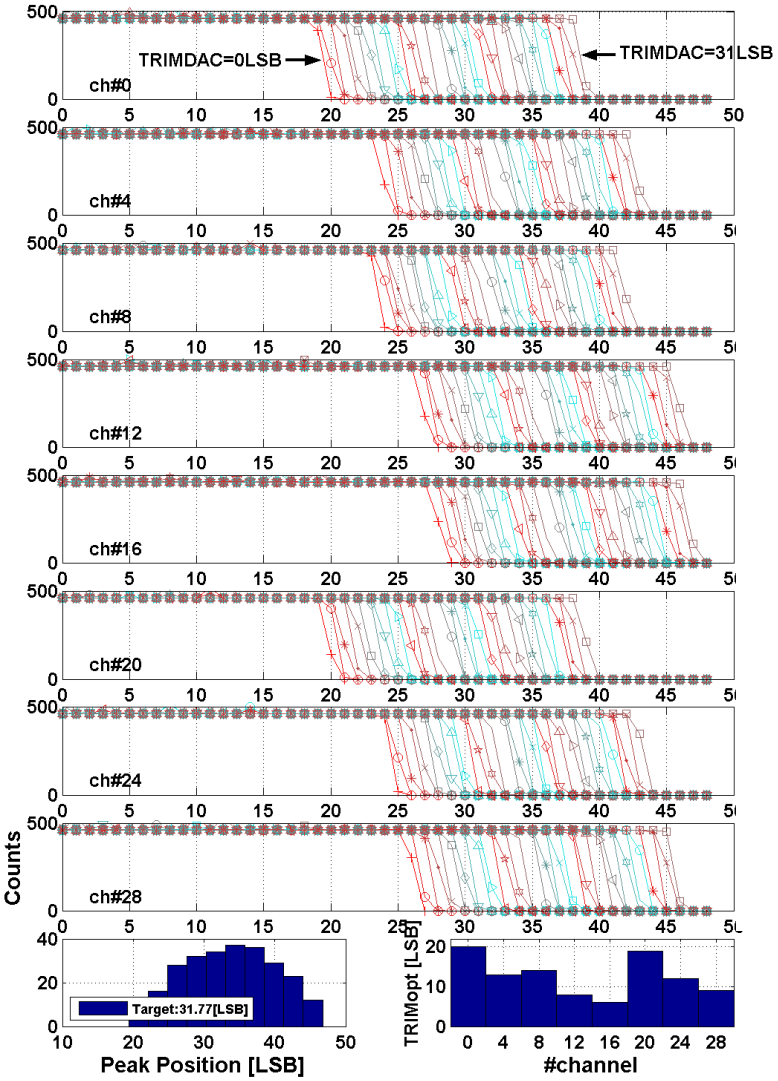

- The input stage is a transimpedance amplifier built around a folded cascode wide band amplifier with a bridged-T low-pass filter in the feedback loop
- Gain factors: ×1, ×2, ×4, ×8, and ×16
- Handles both signal polarities

# Timing channel

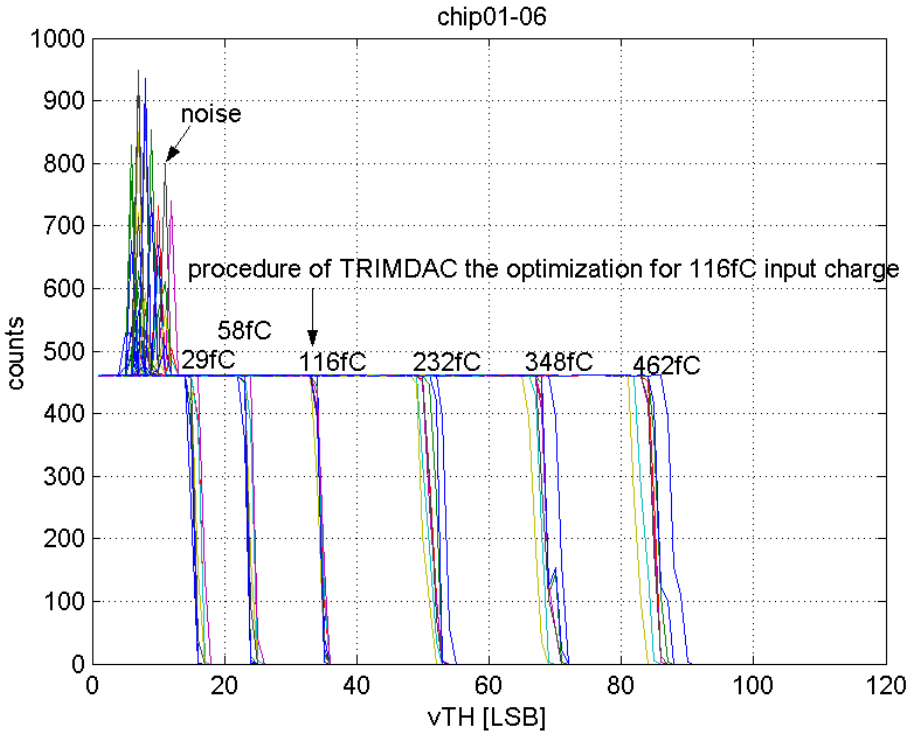



- Fast Shaper - $T_{peak}$ = 25 ns
- Comparator with TWC - $T_{walk}$ < 2 ns
- The output signal from the timing channel is used to latch a 14-bit time stamp of 1 ns resolution and to enable the peak detector and hold (PDH) circuit in the energy channel
- Each comparator is equipped with a 5-bit trimming DAC, which allows to correct the threshold offset on the channel basis with a precision better than 1 LSB in the threshold DAC (8-bit) common for all channels

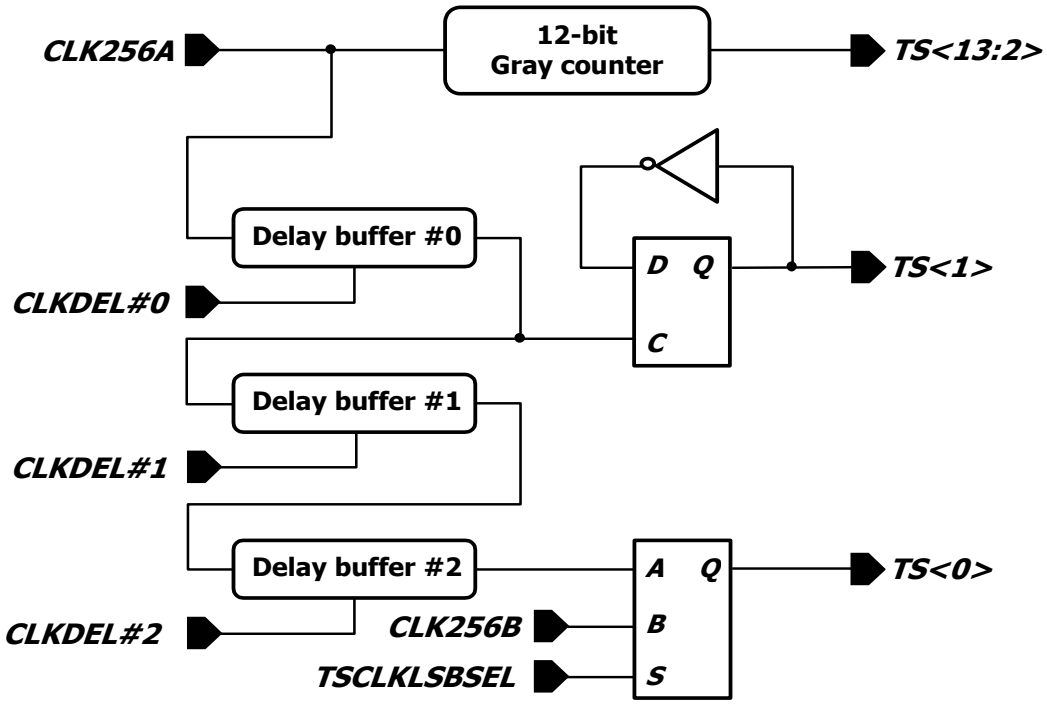
# Timing channel - trimming procedure

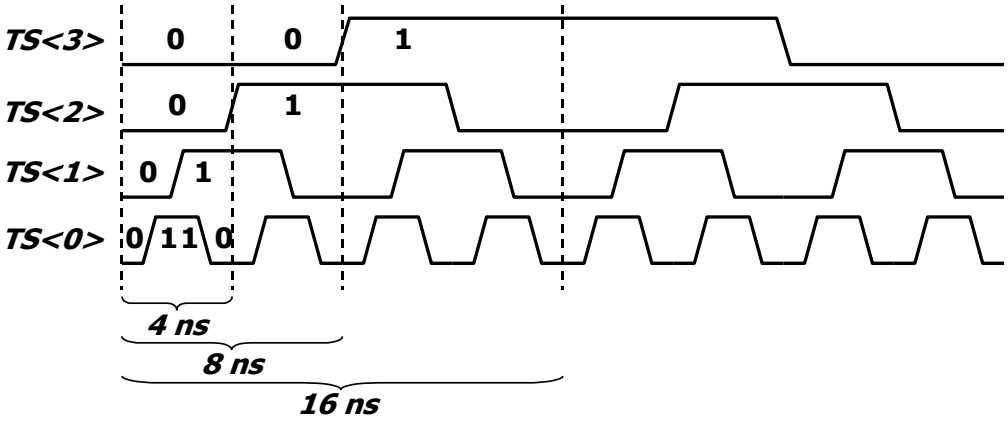



$vTRIM_{LSB} \approx 1.2$ mV ($vTH_{LSB} \approx 2$mV)



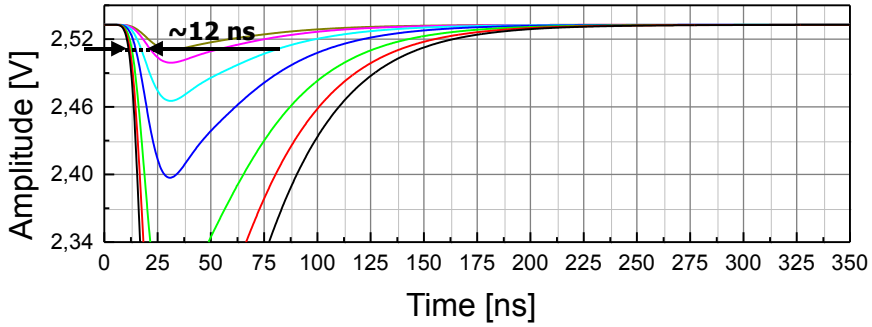
# Timing channel - time stamp generation

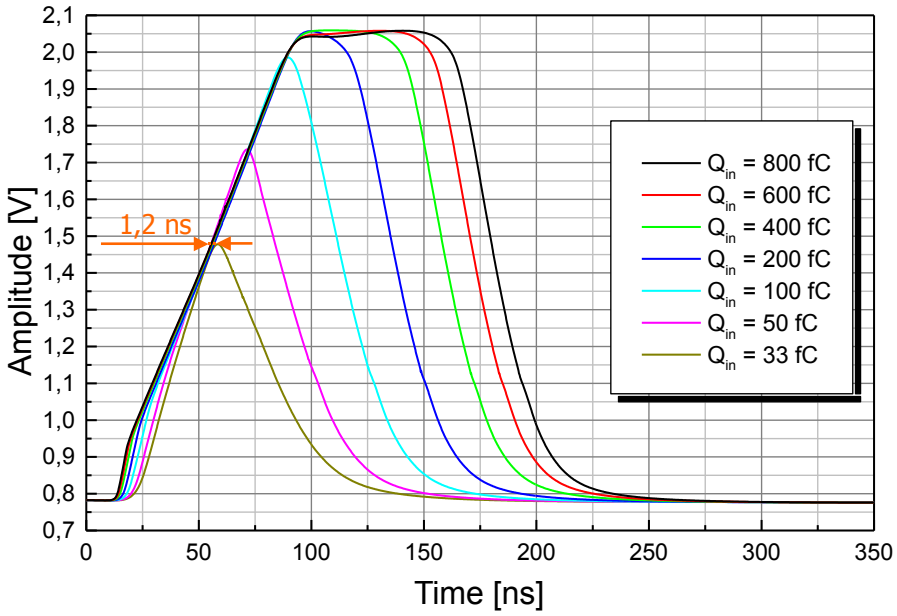



- The 14-bit time stamp signature is combined of:
  - 12-bit Gray-encoded counter,
  - Toggle flip-flops with tunable delays
  - Input clock.
- In this scheme we can achieve 1 ns resolution at 256 MHz input clock frequency

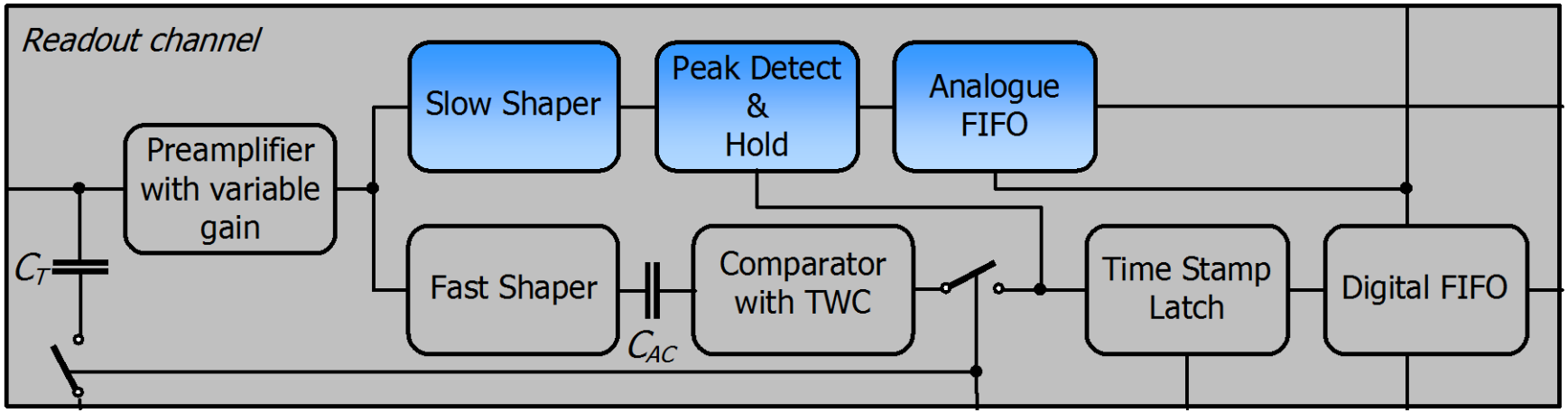
# Time Walk Compensation



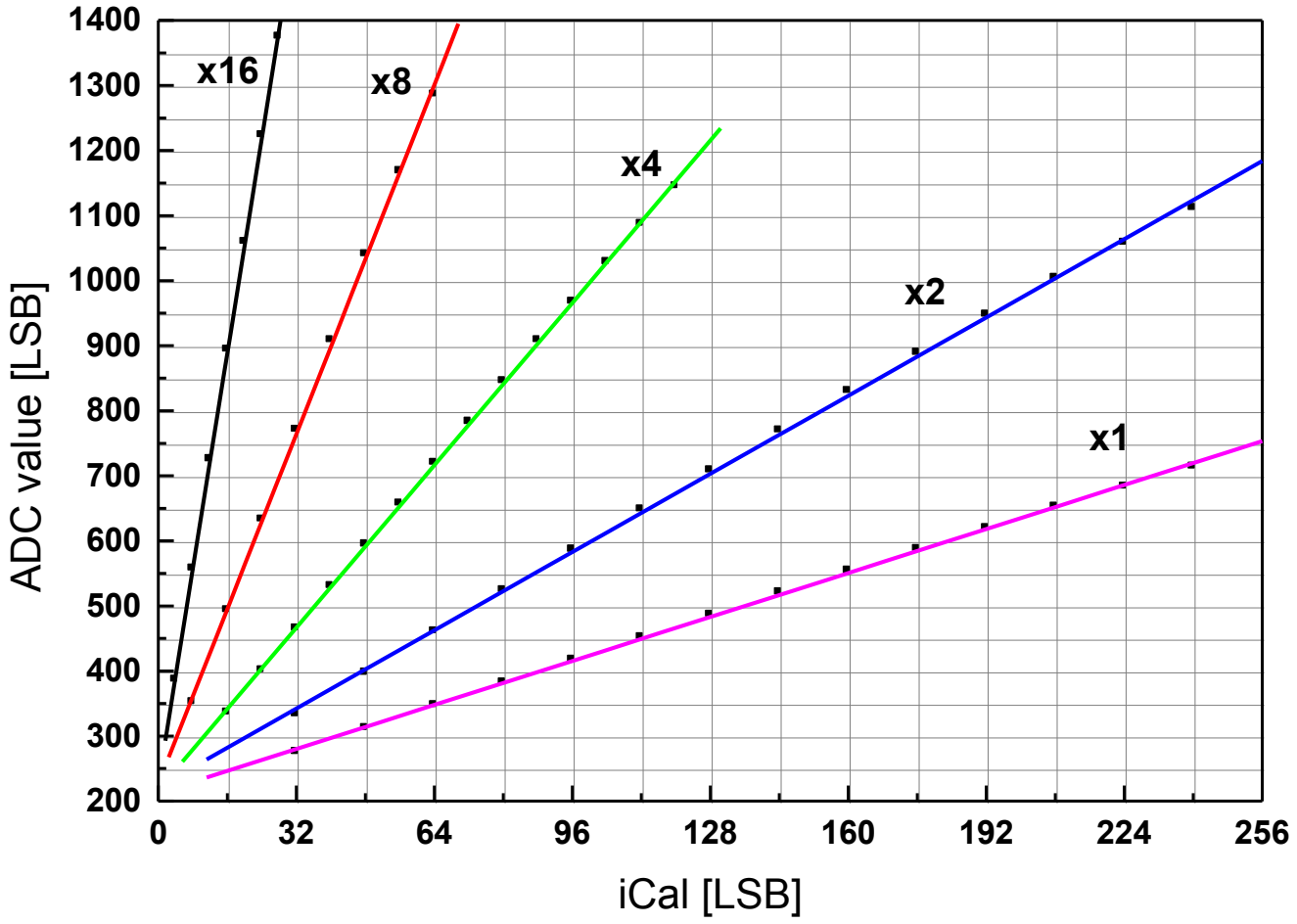

- Crossing of the same threshold level is relatively different in time for small and high signals
  - Gain x1
  - About 12 ns window
  - Compensated by TWC to 1.2 ns

# Energy channel




- Slow Shaper - $T_{peak}$ = 85 ns
- The PDH circuit detects peaks of incoming pulses and holds their values for a given time period controlled with respect to the response of the comparator in the fast timing channel

# Energy channel linearity



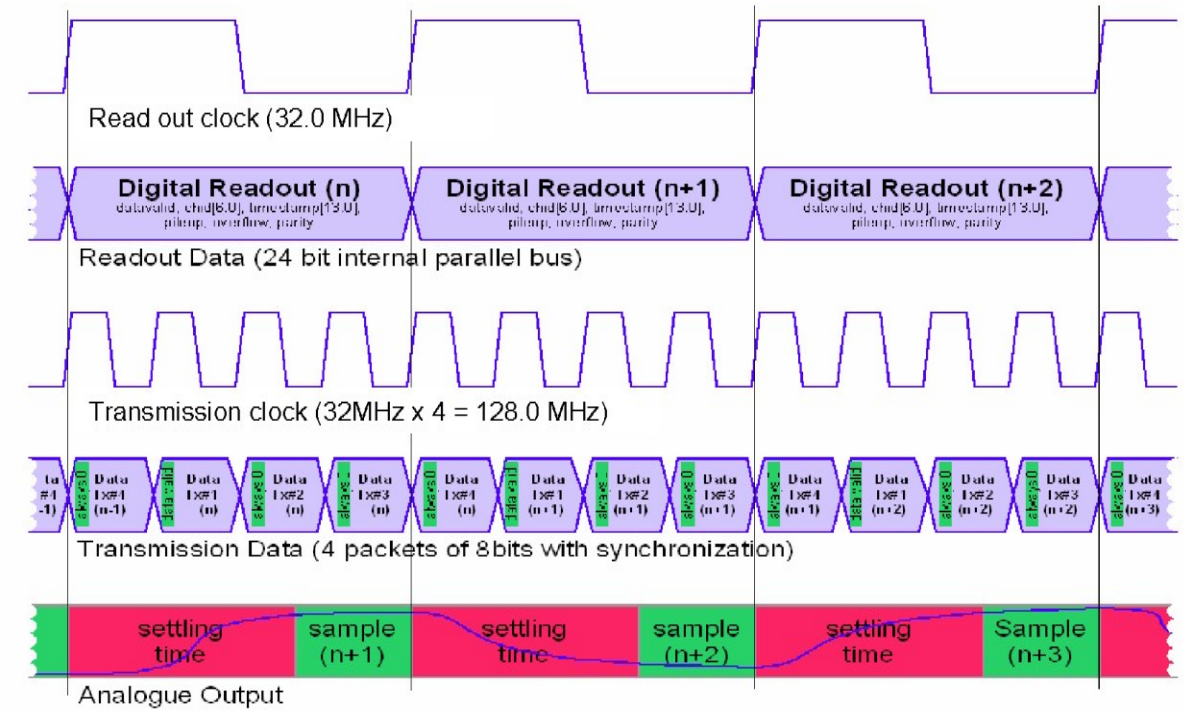

- Measured gain factors: ×1, ×1.78, ×3.70, ×7.94, and ×19.58

# Data format and timing diagram

**ASIC output: 25 bits + analogue information**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | DV | TS13 | TS12 | TS11 | TS10 | TS9 | TS8 | TS7 |
| 1 | 0 | TS6 | TS5 | TS4 | TS3 | TS2 | TS1 | TS0 |
| 2 | 0 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 3 | 0 | 0 | 0 | 0 | 0 | PileUp | OverF | Parity |

data valid TimeStamp channel id




multiplexed readout

digital output

analog output

# Noise level - simulation

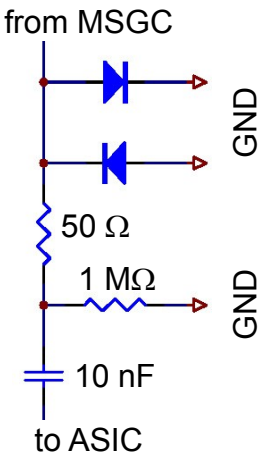
- Noise level for positive signals (33 fC) and $C_D$=23pF

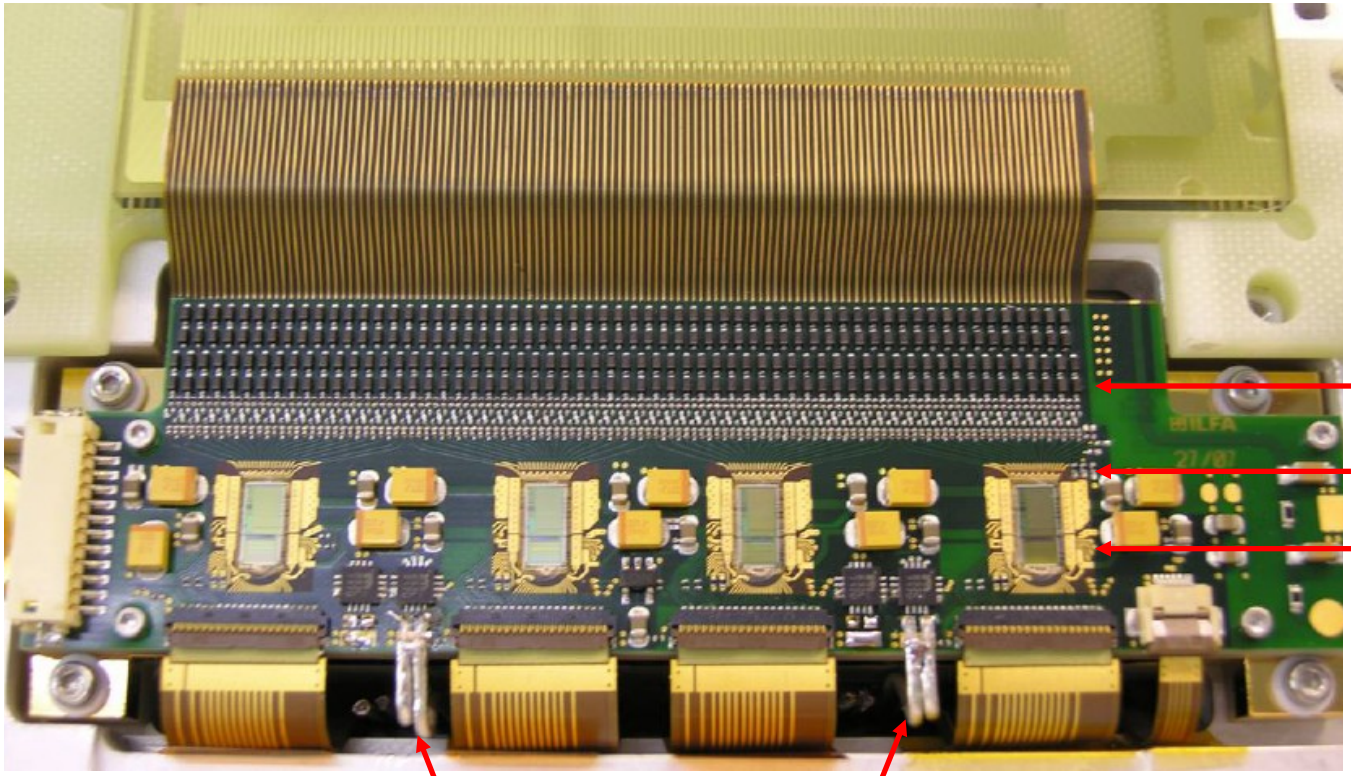
| Gain | ×1 | ×2 | ×4 | ×8 | ×16 |
|---|---|---|---|---|---|
| $ENC_{FSH}$ [$e^-$] | 4148 | 2248 | 1373 | 993 | 794 |
| $SNR_{FSH}$ | 50 | 46 | 37 | 26 | 16 |
| $ENC_{SSH}$ [$e^-$] | 3590 | 2164 | 1300 | 850 | 610 |
| $SNR_{SSH}$ | 57 | 48 | 40 | 30 | 21 |

- Noise level for negative signals (33 fC) and $C_D$=23pF

| Gain | ×1 | ×2 | ×4 | ×8 | ×16 |
|---|---|---|---|---|---|
| $ENC_{FSH}$ [$e^-$] | 5373 | 2815 | 1616 | 1089 | 857 |
| $SNR_{FSH}$ | 38 | 37 | 32 | 24 | 15 |
| $ENC_{SSH}$ [$e^-$] | 4365 | 2579 | 1485 | 918 | 625 |
| $SNR_{SSH}$ | 47 | 40 | 35 | 28 | 21 |

# Prototype ASIC board for MSGC detector



Input protection circuits built of SMD components

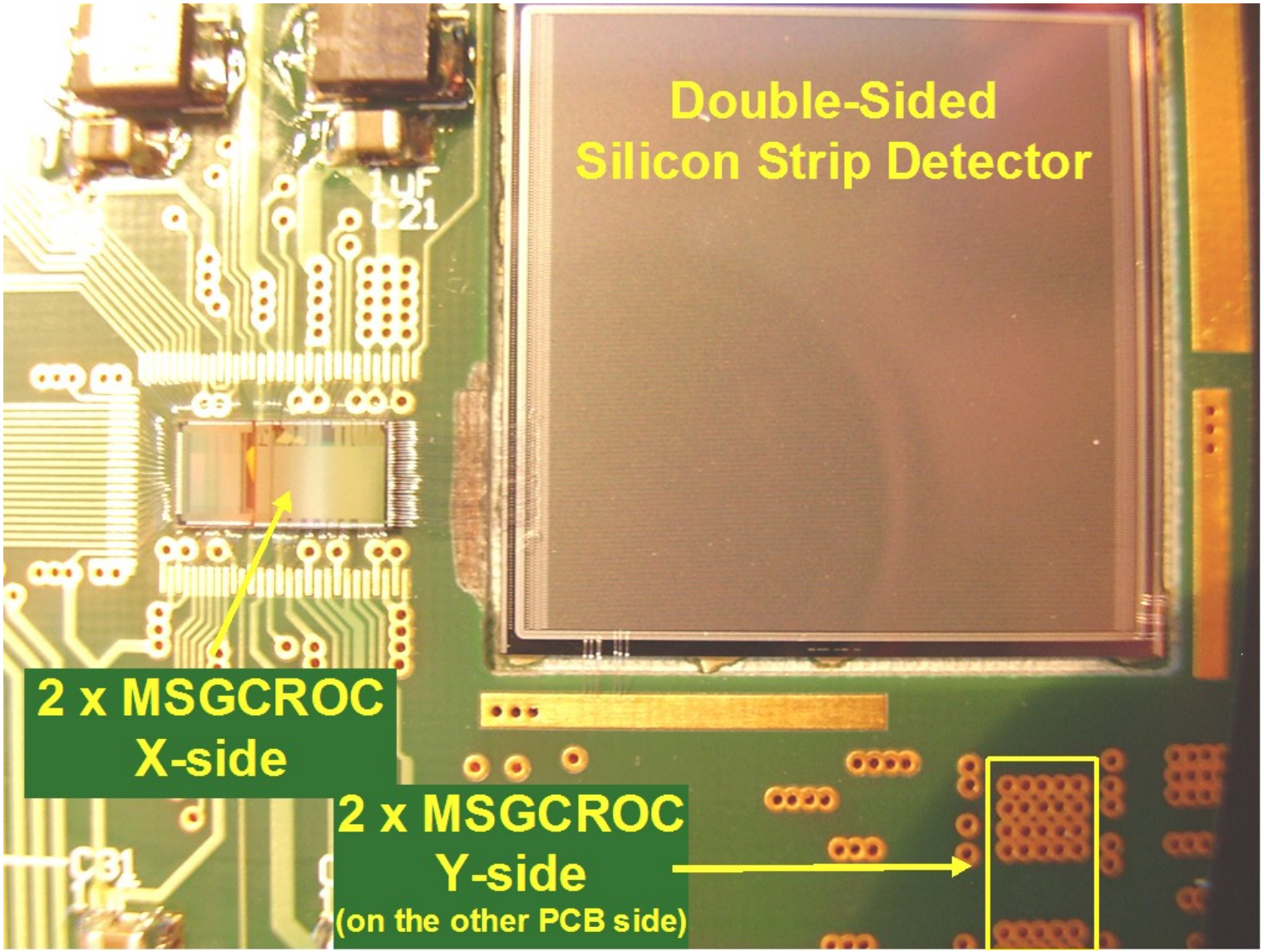
Pitch adaptor

4x MSGCROC ASICs

Distribution of 256 MHz clock - critical

Technology: thickness (0.55mm) multilayer ceramic board by ILFA

# MSGCROC Test Setup

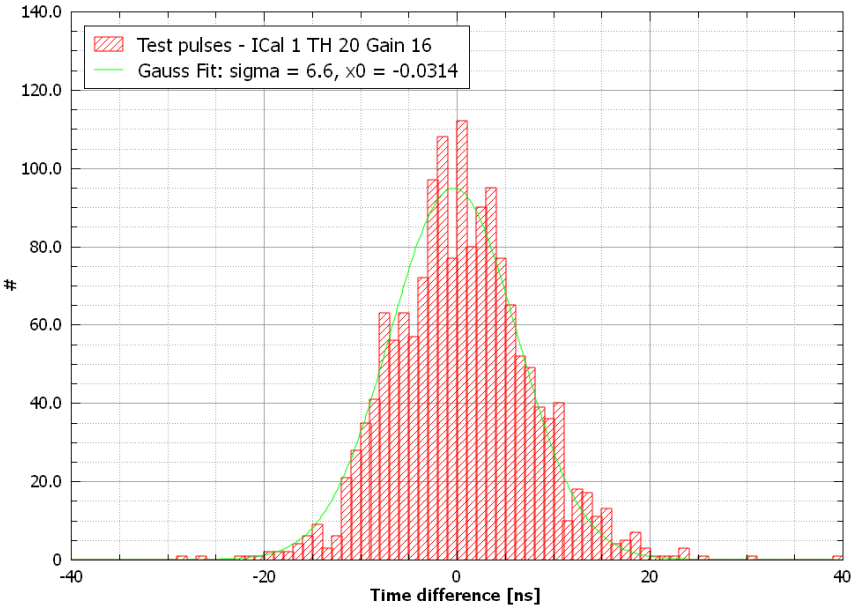


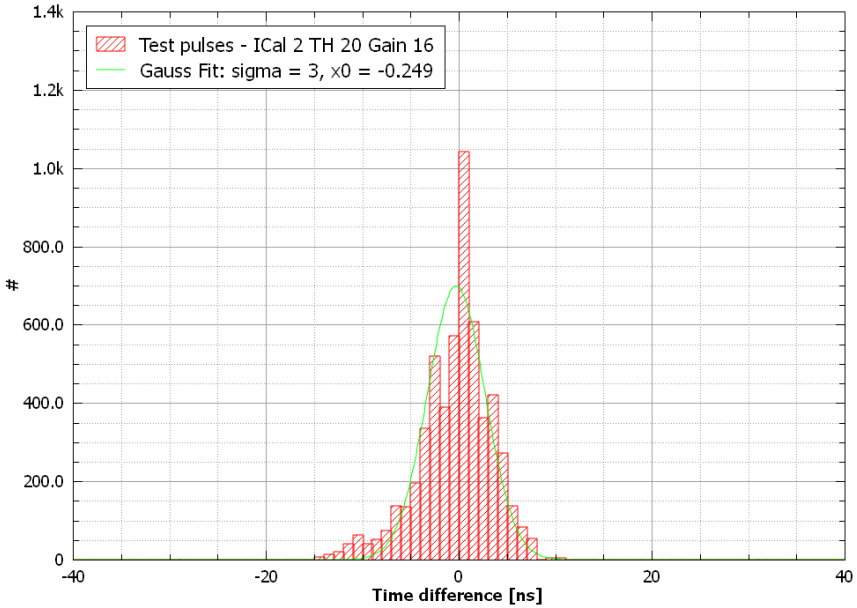
# Noise - measured with Si detector

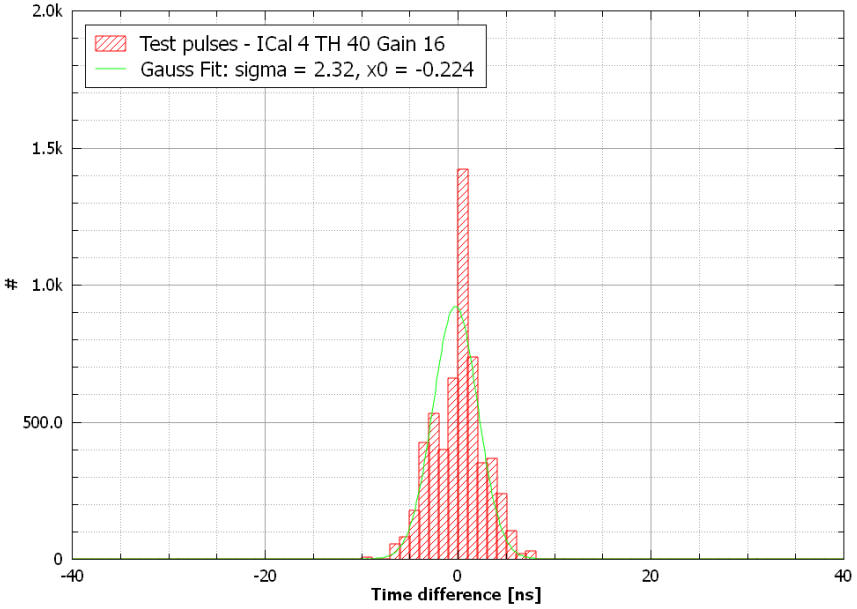
- An average noise level for positive and negative signals for energy channel

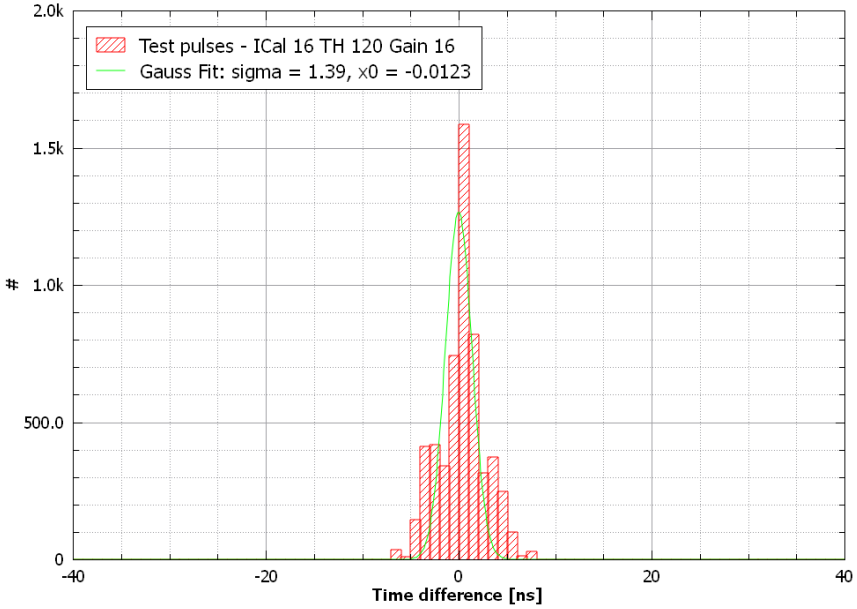
| Gain | ENC positive [$e^-$] | ENC negative [$e^-$] |
|---|---|---|
| x1 | 10984 | 10210 |
| x2 | 6026 | 6073 |
| x4 | 3458 | 3152 |
| x8 | 1888 | 1579 |
| x16 | 1126 | 837 |

# Timing measurement (Test Pulse)

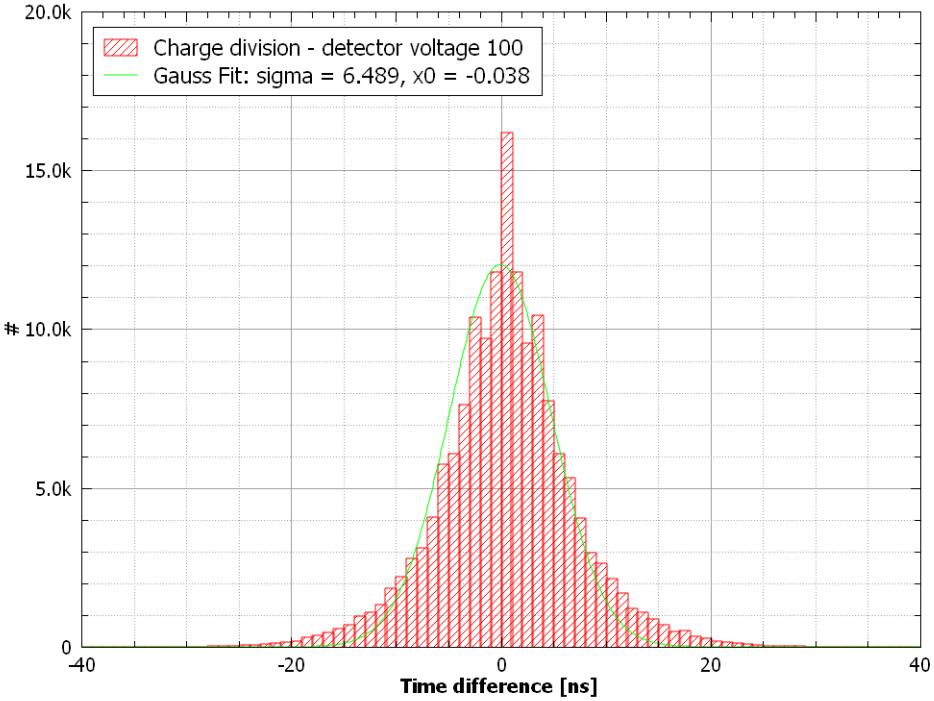


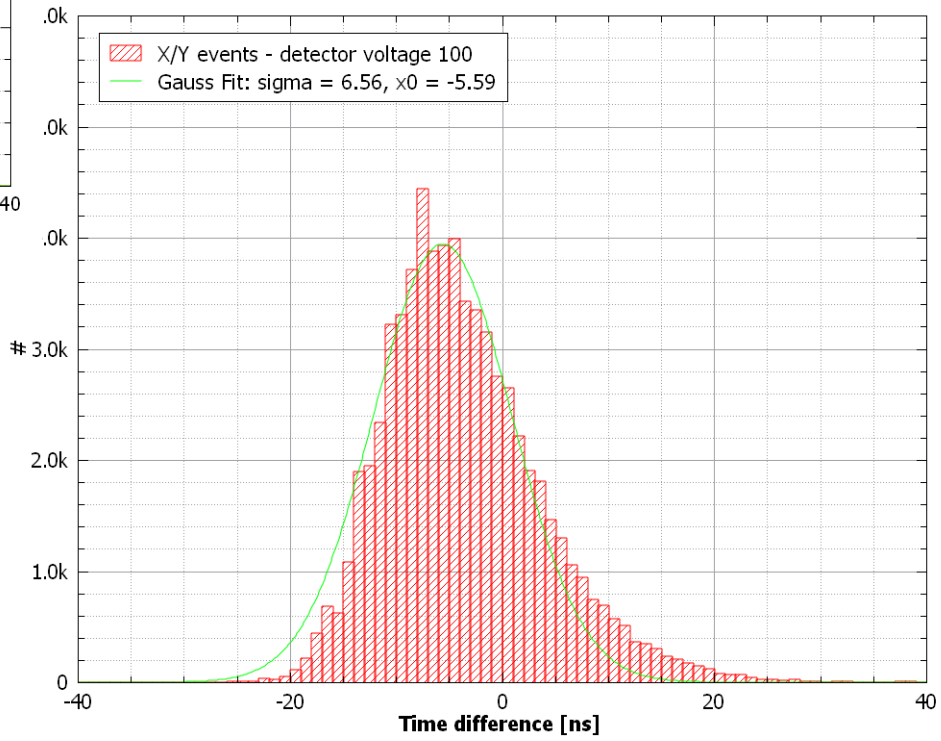



# Timing measurement

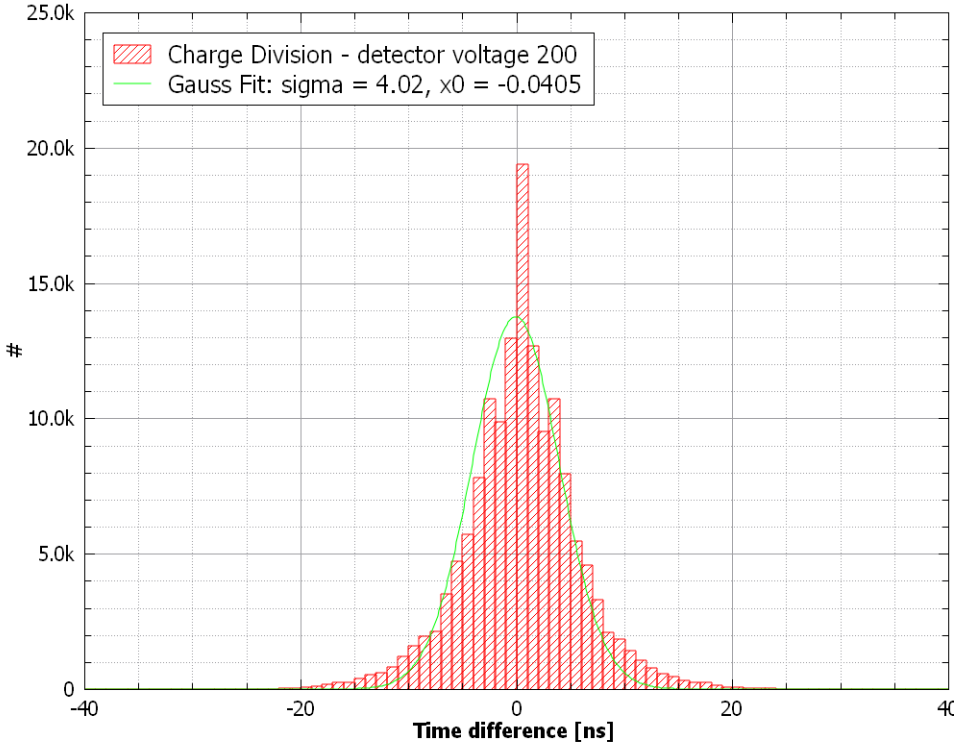



- Charge division between neighboring channels
- Detector voltage 100

- X/Y correlation for 4 ASICs
- Detector voltage 100

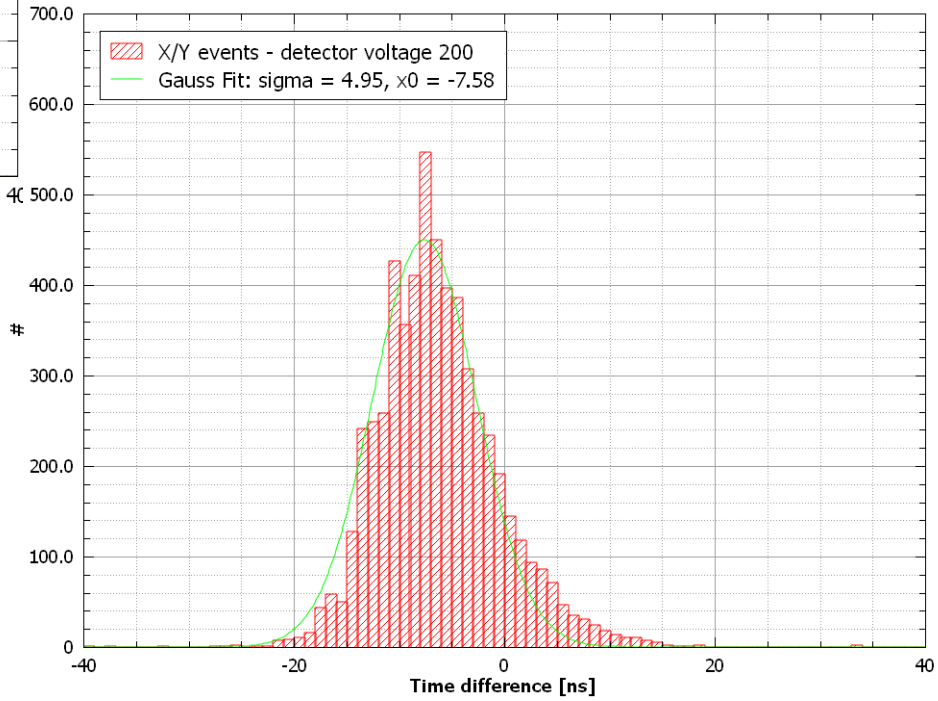


# Timing measurement

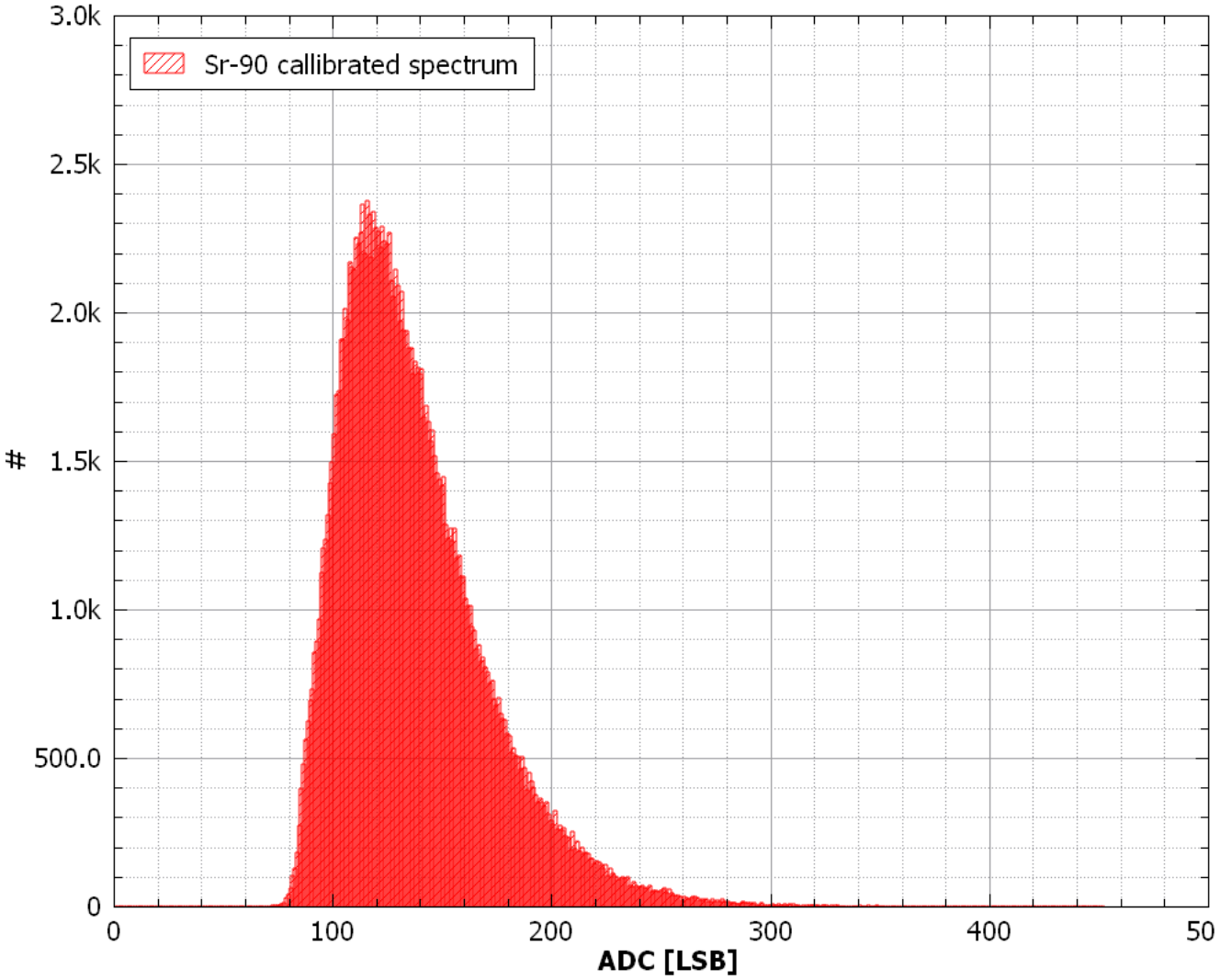



- Charge division between neighboring channels
- Detector voltage 200

- X/Y correlation for 4 ASICs
- Detector voltage 200



# Energy measurement Sr-90



# Summary

- The first prototype of the MSGCROC ASIC has been design and manufactured successfully
- Analogue parameters: gain, offset spread are as expected
  - Final noise analyzes have to be done with proper detector
- Time stamp resolution of a few ns has been achieved
- The full readout system with Si detector is working properly
  - Especially ASICs behave as expected
  - FPGA and timing system work properly
- Future
  - New Ethernet based readout system is under the development
  - Testing the MSGCROC with GEM detector
  - Further ASIC development if needed???

AGH

# Thank you for your attention

# Multi-layer structure and induced signals