RD53 status and plans.

Pixel readout integrated circuits for extreme rate and radiation

1 - RD53A: Status and test results

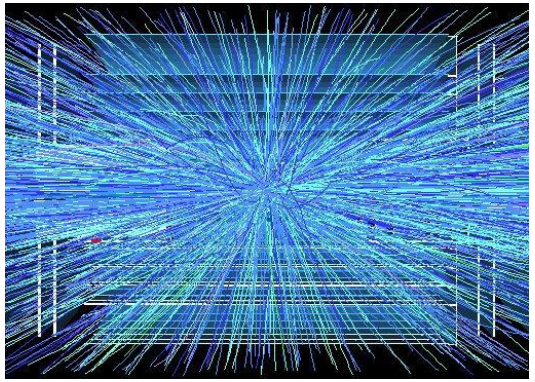
2 – Making final pixel chips

5th LHCC status report

On behalf of the RD53 collaboration

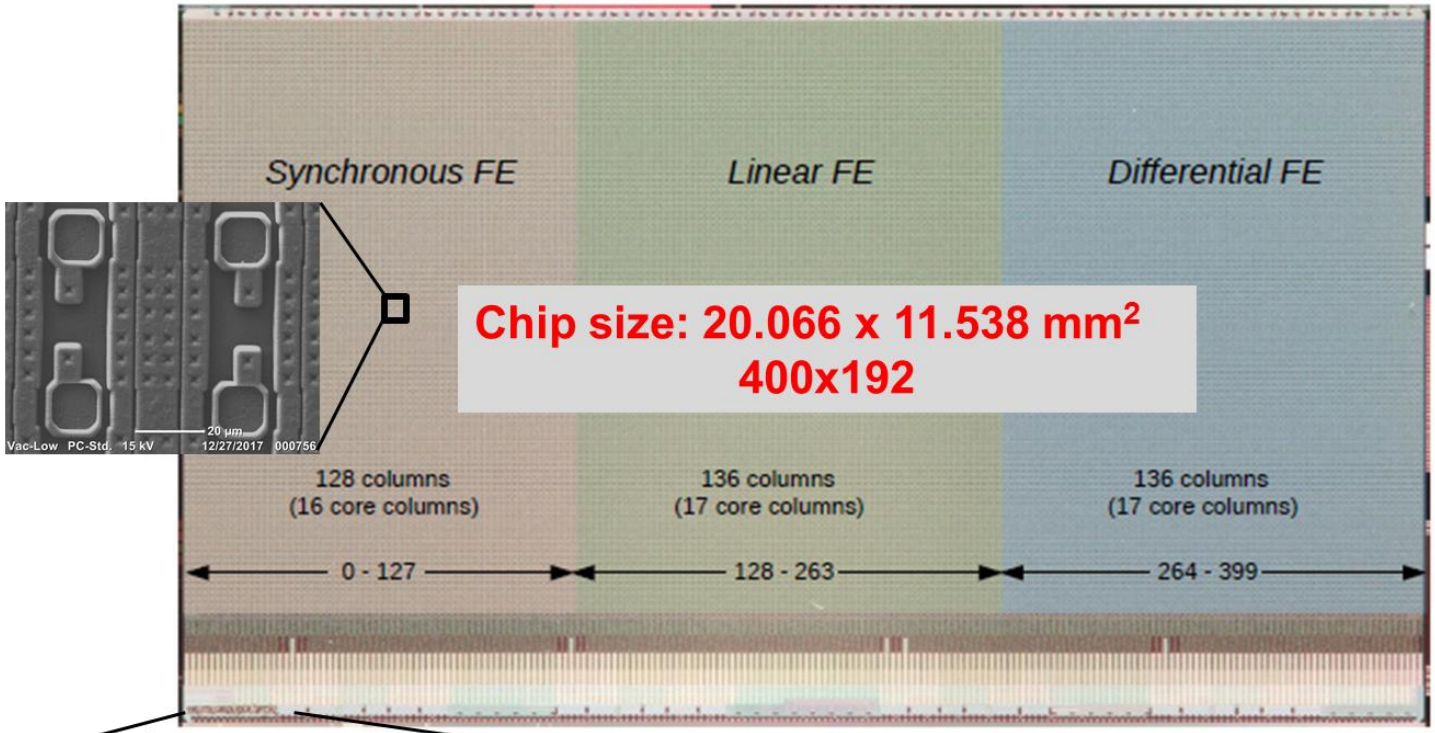
RD53 Introduction and history

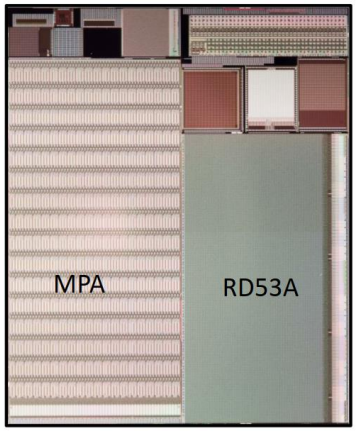
- Focussed R&D developing pixel chips for ATLAS/CMS upgrades
  - Baseline technology: 65nm CMOS
- Extremely challenging requirements for HL-LHC:
  - Small pixels: 50x50um^2 (25x100um^2) and larger pixels
  - Large chips: ~2cm x 2cm (~1 billion transistors)
  - Hit rates: 3 GHz/cm^2
  - Radiation: 1Grad, 2 10^{16} neu/cm^2 over 10 years (unprecedented)
    (500Mrad, changing inner layer after 5 years)
  - Trigger: 1MHz, 10us (~100x buffering and readout)
  - Powering: Serial Powering



- Developed and tested many test structures, building blocks and small pixel arrays
  - Extensive radiation testing to determine how best to obtain sufficient radiation hardness
- Developed design, simulation and verification framework
  - Architecture development and optimization, Extensive verification of complicated and expensive chip
- **RD53A**: Full scale demonstrator pixel chip. Submitted August 2017 and under extensive test. Major successful milestone.
- **RD53B framework: 2018 - 2019**: Development of final ATLAS and CMS pixel chips
- 22 collaborating institutes and many Guests (4 institutes joined recently)
  - Arragon, Bari, Bergamo-Pavia, Bergen, Bonn, CERN, CPPM, Fermilab, LAL-Orsay, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Santa-Cruz, Seville, Torino,
  - 180 on collaboration Email list, 110 on RD53 guests list (ATLAS/CMS people involved in phase 2 pixel but not on chip design), 95 on RD53 NDA list (65nm TSMC technology access), 80 on serial power list (ATLAS/CMS people interested/working on serial powering), 40 on RD53AB core design team, 100 on RD53A testing mailing list
  - ~16 PHDs, ~90 conference/workshop/ publications presentations

RD53A demonstrator



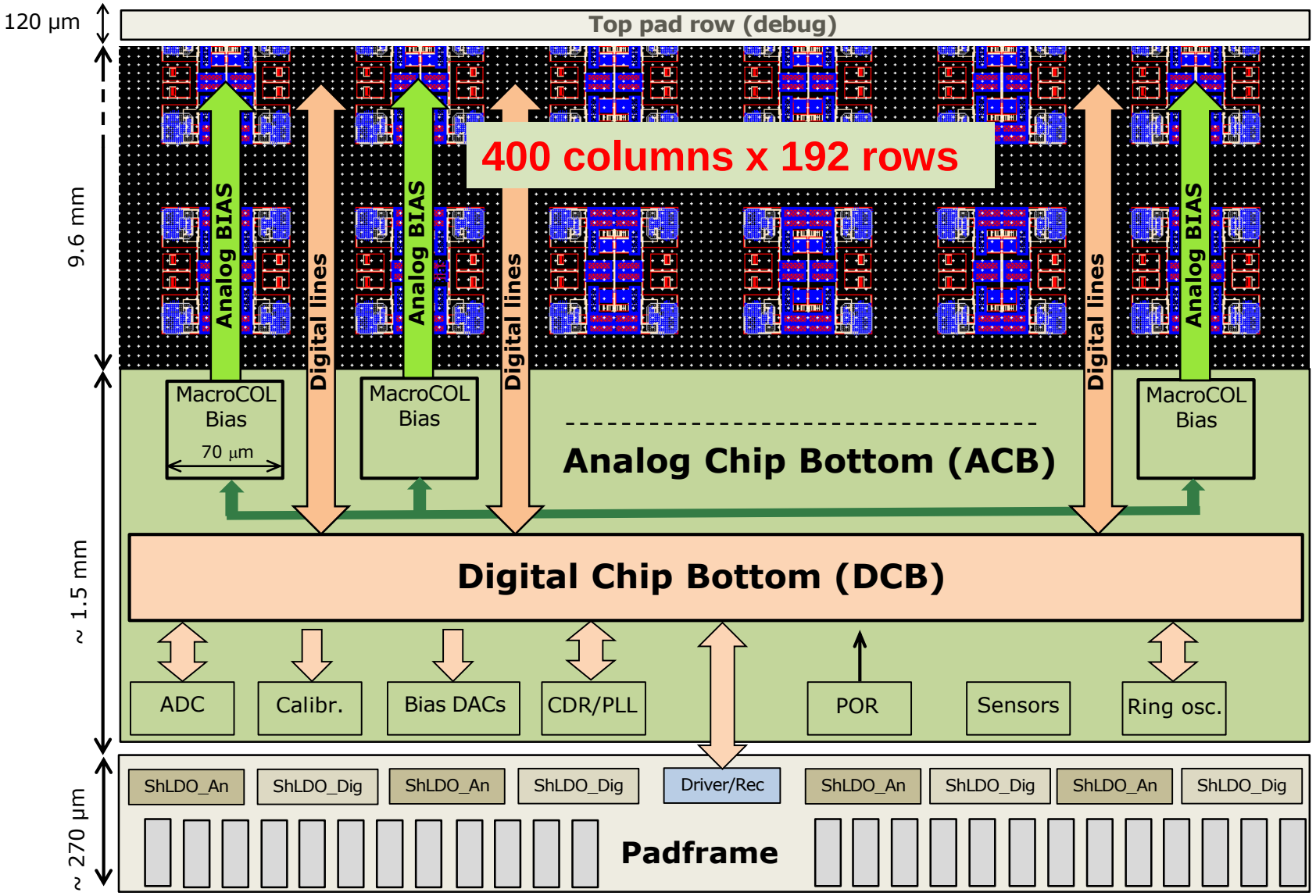


MPW together with CMS tracker chips

- **Aug. 31, 2017: Submission**
- **Dec. 6, 2017: First chip test**
- **Mar. 15, 2018: 25 wafers ordered**
- **Apr. 13, 2018: First bump-bonded chip test**

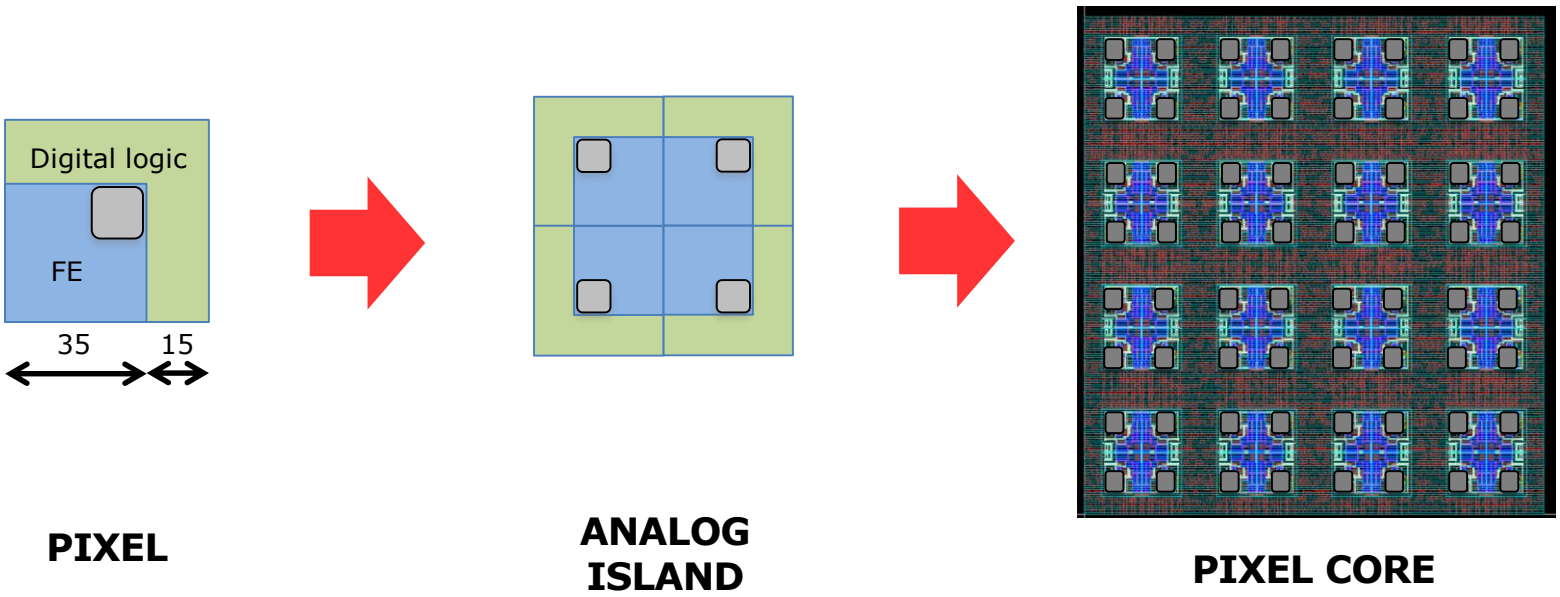
Chip doc on CDS: http://cds.cern.ch/record/2287593

RD53A demonstrator



Organization of pixel Matrix

- Pixel matrix built of 8 x 8 Pixel Cores: Used N x M times
  - 16 analog islands (2x2 quads) embedded in a flat digital synthesized sea
  - Readout of pixel array organized done via pixel core column busses.
  - Allows flexibility in organization of pixel region organization (hit buffering)
- Pixel Core simulated/verified at both digital gate level and analog transistor level
- All Cores (for each FE flavour) are identical
  - Hierarchical verification for very large transistor count

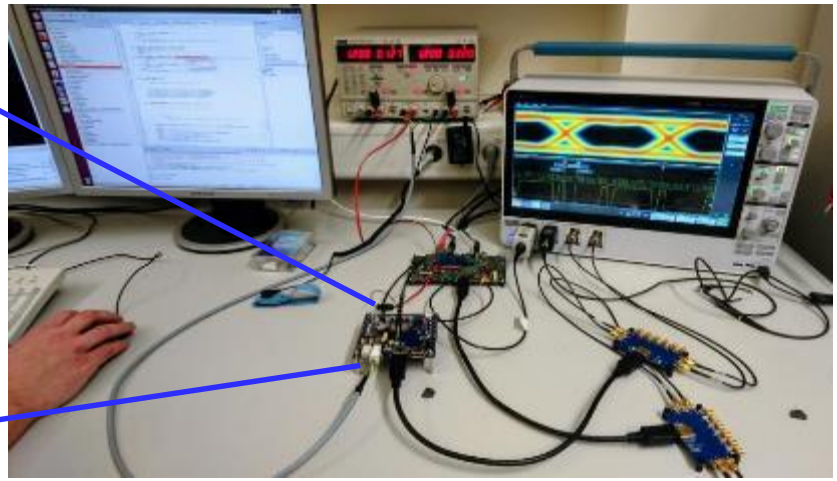


RD53A Specifications

Technology	65 nm CMOS
Pixel size	50x50 um^2 & 25x100 um^2
Pixels	400x192 = 76800 (50% of production chip)
Detector capacitance	< 100 fF (200 fF for edge pixels)
Detector leakage	< 10n A (20 nA for edge pixels)
Detection threshold	<600 e-
In-time threshold	<1200 e-
Noise hits	< 10^{-6}
Hit rate	< 3 GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1 MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤ 1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500 Mrad at -15°C
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1 W/cm^2 including ShLDO losses
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

http://cds.cern.ch/record/2113263

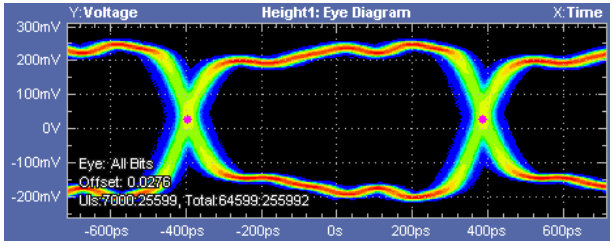
RD53A testing



- **Two test systems:**
  - **BDAQ53 – Bonn University https://gitlab.cern.ch/silab/bdaq53**
  - **YARR – LBNL https://gitlab.cern.ch/YARR/YARR**
- **Functional and radiation testing of RD53A on-going**
- **Distribution of setups across collaborations (RD53, ATLAS, CMS) has started**
- **First test of pixel assemblies in test beams and with radioactive sources**
- **Weekly RD53A testing meetings with latest test results, where anybody from ATLAS and CMS pixel communities can join in**
- **RD53A public plots: https://twiki.cern.ch/twiki/bin/view/RD53/RD53APublicPlots**
- **RD53A being integrated into tracker testbeam systems**

RD53A measurements: I/O

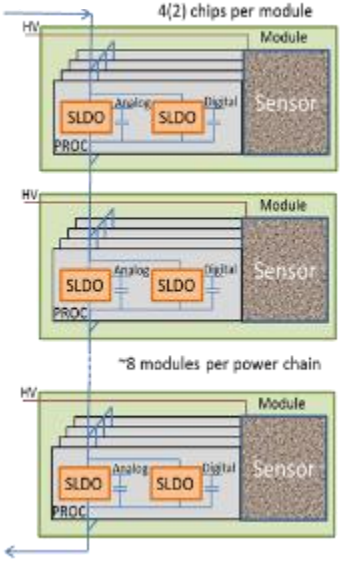
- Fully operational using serial I/O ports
- 160 Mbps CMD input (LVDS): Clock + Data
  - CDR/PLL recovers data and clock from input stream @ 160 MHz.
    - In certain conditions (VDD, Temperature, Radiation) a lock issue is encountered. Problem understood. Proposed solution under final verified.
    - New prototype submission in summer 2018 to test improved version
  - Command decoder responds
  - Chip can be configured
- Aurora readout links (4) with CML output:
  - Readout tested at 160Mbits/s - 1.28Gbits/s



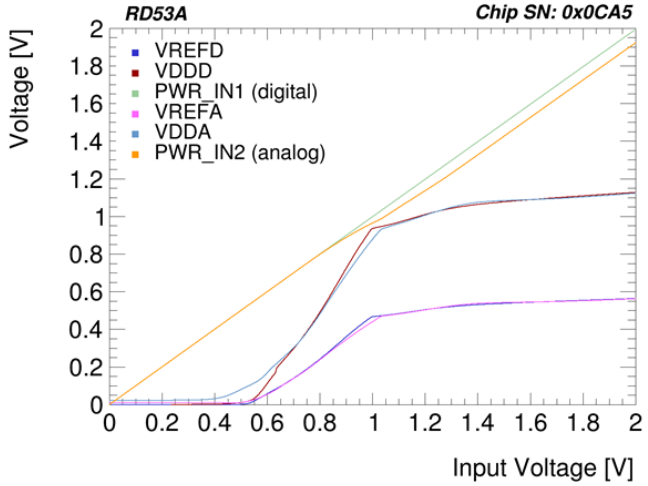
ShuntLDO

- Designed to operate with **Serial Powering**
  - Constant current to power: Modules in series; Chips on same module in parallel
  - ShuntLDO dimensioned for full size production chip.
- Three operation modes:
  - ShuntLDO: Constant input current, Local regulated VDD
  - LDO: External un-regulated voltage, Local regulated VDD
  - Direct power: Shunt-LDO bypassed
- **All three powering modes shown to work**.
  - Chip/System tests with serial powering on-going
- Improvements and additional features:
  - Absolute precision of on-chip bandgap: Done
  - Startup behavior, Low power mode, Output current limitation, Over voltage protection, Current monitoring

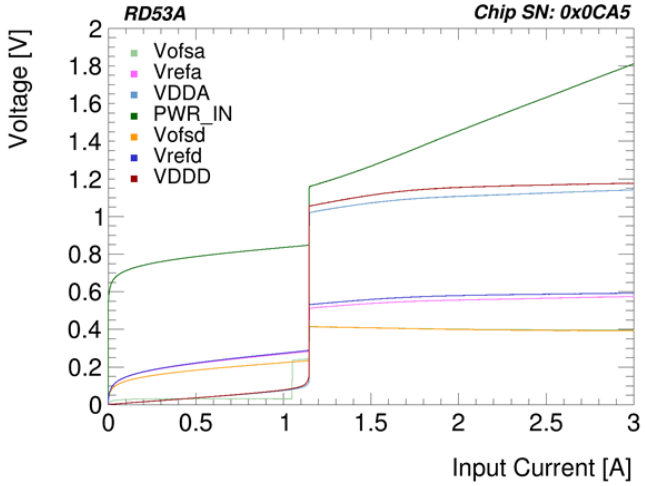
New SLDO prototype will be submitted this summer



LDO mode

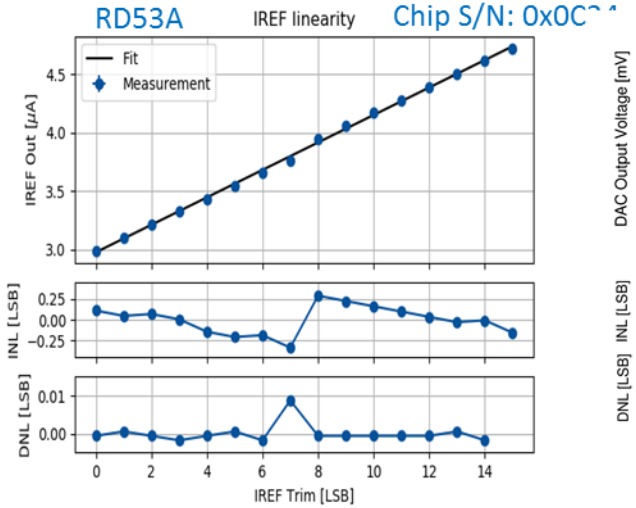


ShuntLDO mode

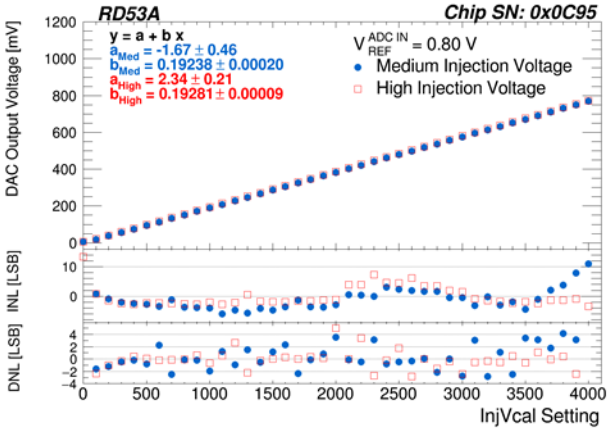


Calibration, bias and monitoring

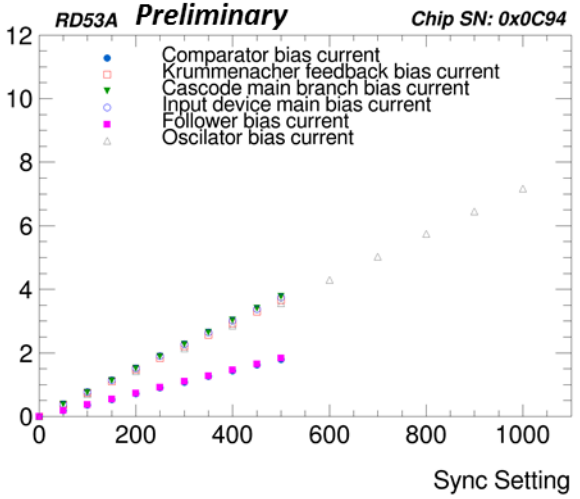
- All biases provided by internal current DACs
- All bias currents and voltages monitored using internal 12-bit ADC and can be accessed on two multiplexed outputs: IMUX and VMUX (used also for ADC calibration)
- 4 temperature (and radiation) sensors on different locations of the chip
- Ring oscillators with different gates to monitor effective radiation damage
- Works well and don't require major modifications



Ref. current vs Trim bits



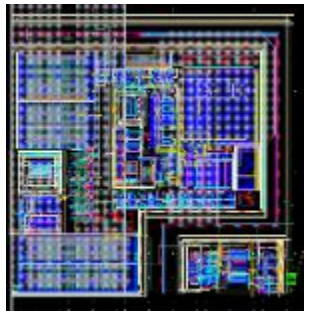
Characterization of injection 12-bit DACs

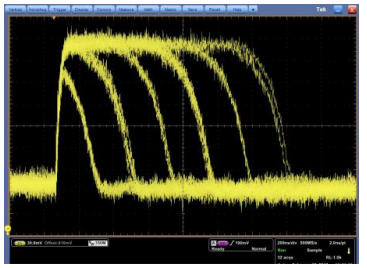


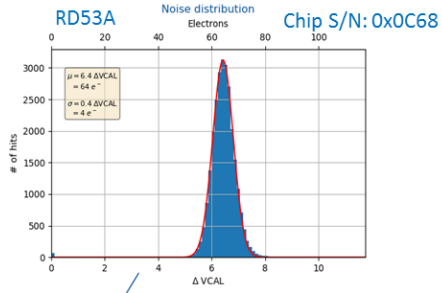
Example of bias DAC scan

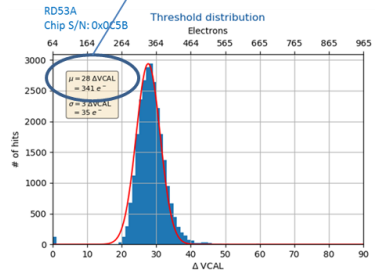
Analog FE testing

- **All 3 FEs working well**
  - Can be tuned for use at thresholds of 1000e- and below
    - Tuning procedures improving as getting more experience.
    - Use of a preliminary noise tuning optimization indicates possible operation with threshold as low as ~350e- (TBC)
  - Diff FE: A parasitic loading effect between analog and digital design domain gives more pixel – pixel variation than anticipated
    - Easy to resolve in final pixel chip
    - Good “warning” that we have to be more careful about this for final chips
  - Sync FE: Auto-zeroing cycle for self threshold adjust (and fast TOT counting)
    - To be taken into consideration for firmware and software when using this
  - Lin FE: Extended threshold adjust range could be advantageous.
- Operation experience with each FE rapidly improving
  - Baseline parameters
  - Recommendations for FE tuning (threshold)
  - Software and firmware support for characterization and tuning
  - Different operation conditions: With and without pixel sensor, Room and cold temperature, radiation, etc.
- More details on each FE in backup slides.



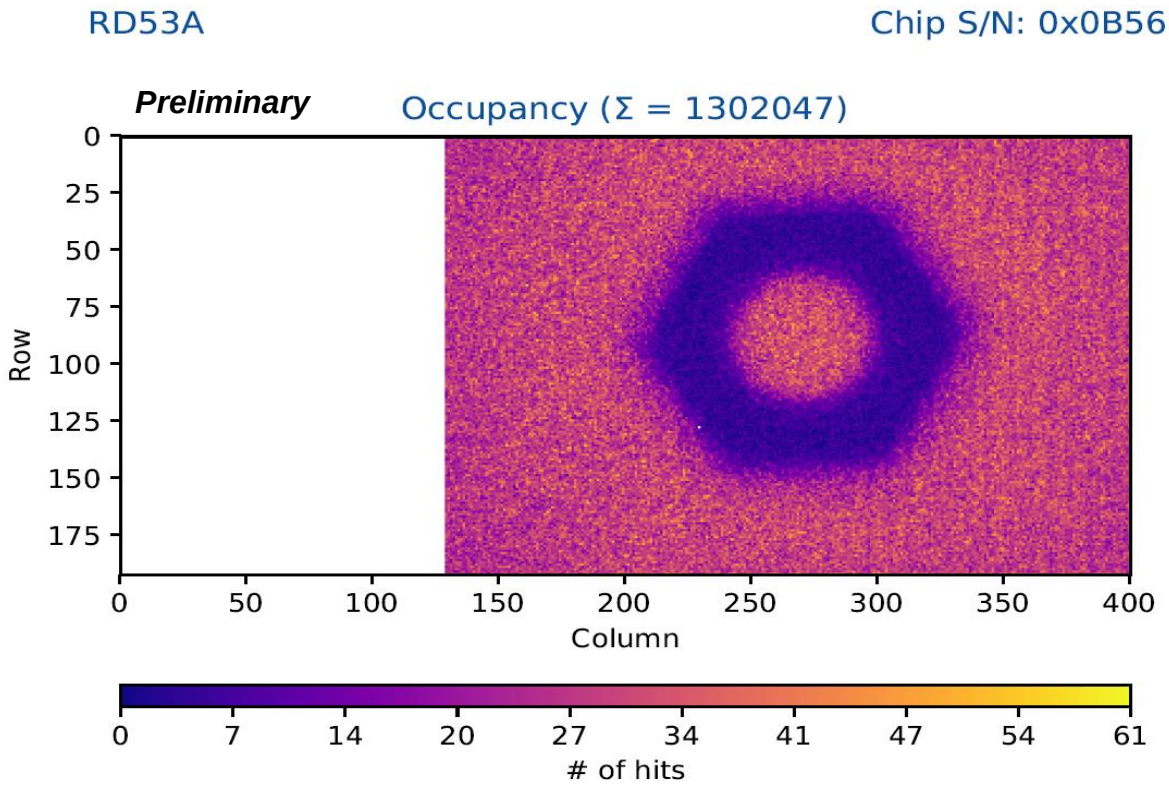






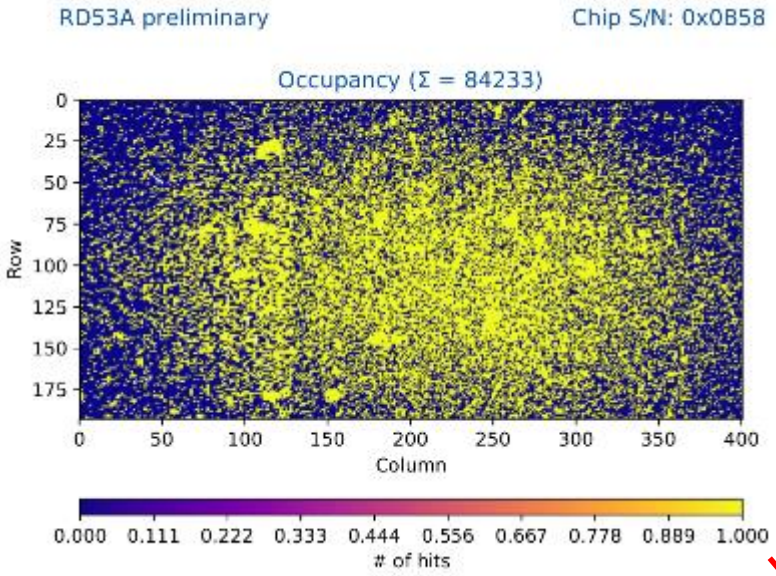
First signs of life of chip assembly

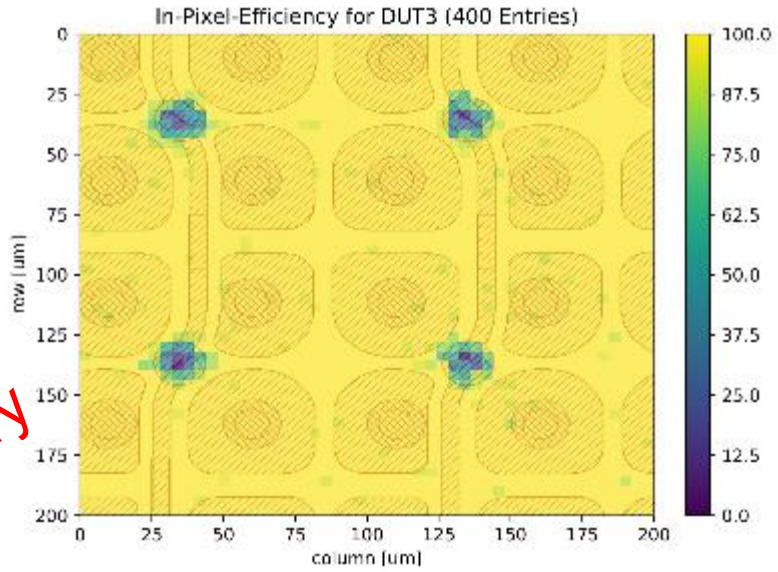
- 4 RD53A chips with sensor arrived in Bonn on 13 April 2018
- Image of a nut placed on the sensor backside, illuminated with Am241 source
- Hit-OR-trigger scan, LIN and DIFF FE, both set to 3 ke- threshold, un-tuned
  - FW/SW for SYNC FE auto-zero were not yet available



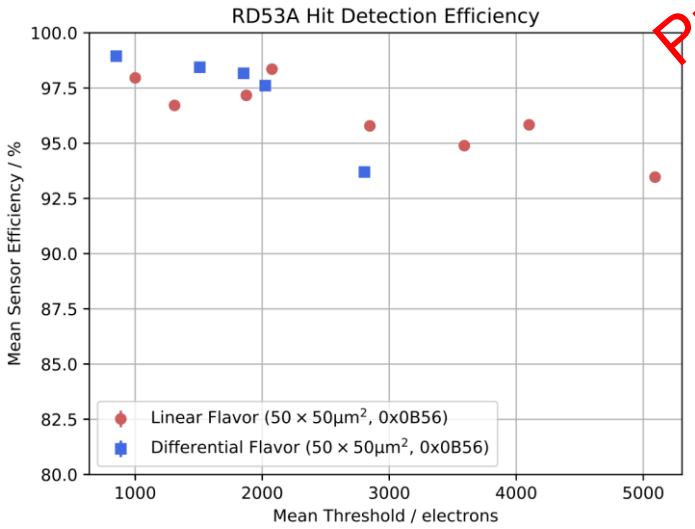
Sensor ID W8S7: 50x50 µm, 150 µm , n-in-p planar (MPP)

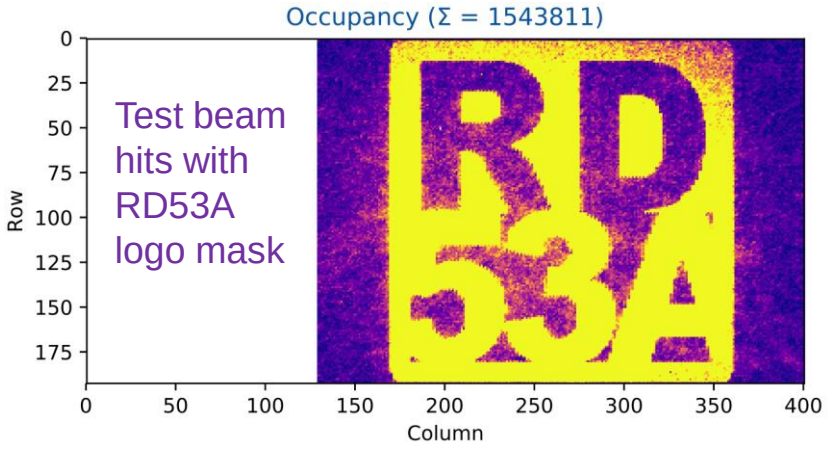
First test beam results with sensor





Preliminary





Preliminary test summary

- **RD53A is fully functional with very promising test results**
- No major problems so far, but some “features” require proper Single Chip Card configuration and firmware/software optimizations
- First X-ray tests at CERN done: Promising results but more test routines and setup verification required.
- These early results gave information for the improvement of some IPs, to be submitted as small prototypes in Q3/2018
- First production lot of 25 wafers ordered
  - More lots to be added soon to cover community needs
- ATLAS/CMS plans to test different pixel sensors types (~10) and variants (2 - 4 for each type) with RD53A in the coming months (https://indico.cern.ch/event/721883/)
- Pixel modules (2x1 and 2x2) being designed with RD53A chip in both ATLAS and CMS pixel communities
- Large scale serial powering tests planned with RD53A based pixel modules
- **Test results confirm that RD53A is a fundamental and solid baseline for final ATLAS/CMS chip development**

MAKING FINAL PIXEL CHIPS FOR ATLAS AND CMS

ATLAS – CMS final chip(s)

- Many common requirements
  - 160Mbits/s Control/configuration link, 4 x 1.28Gbits/s readout E-links, Pixel size, Readout formatting/compression, Monitoring, Serial powering, Radiation, TOT charge measurement, Analog pixel Front-end (threshold, noise, etc.), , ,
- But also some differences
  - Trigger:
    - CMS: 1 level: 750KHz, 12 us
    - ATLAS: 1 level: 1MHz, 10us 2 level: L0: 4MHz, 10us, L1: 600KHz, 25us

    Both trigger schemes can be accommodated with one design (under final verification)
  - Beam distance (and hit rate): CMS: r = 3cm ATLAS: r = 4cm

    Comply with the highest hit rates (CMS): Dead time, buffering, readout (under final verification)
  - Serial power protection
    - ATLAS: Possible use of active serial power protection chip/system
    - CMS: Passive, extra current taken by other chips in parallel.

    Passive protection scheme needed for both
  - On-module data aggregation (low rate regions): CMS

    Non challenging and requires only few (3) on-module signals
  - Chip size:
    - CMS: **20x19.2 mm^2 (400 x 384 pixels)**
    - ATLAS: **22x16.4 mm^2 (440 x 328 pixels)**

    Determined by detector layout (e.g. CMS inner barrel at r = 3cm)
- **Meetings between the two experiments to converge on the best approach to assure appropriate pixel chips for both experiments. Catalyzed by the LHCC and dedicated meeting (one week ago) to assure convergence:** https://indico.cern.ch/event/728067/
- **Differences can be accommodated by one common architecture, mapped into two physically differently sized chips.**

Proposed design strategy

- One common design framework: called RD53B
- One common design team : Keep good/efficient team together
- Two submissions of the RD53B design framework with different matrix sizes
- The matrix size is a parameter in the design framework, controlling how many identical Pixel Cores are arrayed in x and y
  - Scalable hierarchical netlist
- All common and specific requirements implemented in a unique architecture
  - no difference in the chip bottom or in the core design

Common design team (as RD53A)

Collaboration board chair:
Lino Demaria, Torino

Interface to experiments: Co-spokespersons
Jorgen Christiansen, CERN (CMS) , **Maurice Garcia-Sciveres, LBNL** (ATLAS)
- General organization, Funding, Specifications,

Experiment observers
Duccio Abbaneo, CERN (CMS) ,
Kevin Einsweiler, LBNL (ATLAS)

RD53 design framework for final pixel chips: Flavio Loddo, Bari; Tomas Hemperek, Bonn ~13 FTE

Floorplan/integration: 1 FTE
Flavio Loddo, Bari
- Pixel array, Bump pad, EOC, Power distribution, Bias distribution, Analog/digital isolation, Integration, Verification

Analog FEs with biasing: 2 FTE
Luigi Gaioni, Bari; Ennio Monteil, Torino; Amanda Krieger, LBNL
- Specification/performance, Interface, Analog isolation, simulation model, Abstract, Integration, Verification

Monitoring: 1 FTE
Mohsine Menouni, CPPM;
Francesco De Canio, Bergamo,
IP designers
- Specification/performance, Interface, Analog isolation, simulation model, Abstract, Integration, Verification

PAD frame: 1 FTE
Hans Krueger, Bonn
CDR/PLL: Piotr Rymaszewski, Bonn
High speed drv: Konstantinos Moustakas, Tianyang Wang, Bonn
Diff. IO: Gianluca Traversi, Bergamo

Digital: 6 FTE
Tomasz Hemperek, Bonn; Luca Pacher, Torino
- **Simulation Framework:**
  Sara Marconi, CERN; Herve Grabas, Santa Cruz
  – Framework, Hit generation/ import MC, Reference model / score board, Monitoring/verification tools, Readout rate estimations, Behavioural pixel chip, SEU injection.
- **Pixel array logic:**
  Sara Marconi, CERN; Andrea Paterno, Torino
  – FE interface, Latency buffer, Core/column bus
- **Digital chip bottom:**
  Roberto Beccherle, Pisa; Francesco Crescioli, LPNHE; Andrea di Salvo, Torino
  – Configuration, Control interface, Readout data format/protocol, Compression
- **Verification:**
  Sara Marconi, CERN; Herve Grabas, Santa Cruz; Attiq Rehman, Bergen
  SEU: Rafael Girona, Seville
  SET: Fernando Munoz Chavero, Seville
  Mixed signal: Luca Pacher, Torino;
  Aikaterini Papadopoulou, LBNL, Oliver Lemaire, LAL
  – Functional, SEU, Interfaces, specifications
- **Library cells:**
  DICE: Denis Fougeron, Mohsine Menouni, CPPM
  Compact latch: Dario Gnani, LBNL
  Timing characterization : Sandeep Miryala, FNL

Serial Power: 1.5 FTE
SLDO: Michael Karagounis, Andreas Stiller, Dortmund.
Bandgap: Gianluca Traversi, Francesco De Canio, Bergamo
Verification: Alvaro Luengo, Aragon; Stella Orfanelli, CERN
- Shunt-LDO integration, On-chip power distribution, Optimization for serial powering, System level power aspects, Power Verification

Design for testability: 0.5 FTE
Giusieppe De Robertis, Bari
- Scan path, BIST, production test patterns, Fault simulation, bump bonding testing

IPs:
Current DAC: Bari
Voltage DAC: Prague
ADC, mux, temp: CPMM
Power on reset: Seville
Ring osc: LAL
Analog buffer: RAL

Support and services:
Tools, design kit: Wojciech Bialas, CERN
Repositories: Flavio Loddo, Bari;
Tomasz Hemperek, Bonn
Radiation model: Mohsine Menouni, CPPM

Testing: Timon Heim, LBNL 3 FTE in RD53 + ATLAS/CMS group
YARR system: Timon Heim, LBNL
BDAQ53 system: Marco Vogt, Michael Daas, Hans Krueger, Tomasz Hemperek, Bonn
Radiation test: Luis Miguel Jara Casas, CERN
Plus many ATLAS/CMS groups not formally part of RD53

Pixel sensor and bump-bonding:
Fabian Huegging, Bonn (ATLAS),
Georg Steinbrueck, Hamburg (CMS)

Names in bold: Member of RD53 management board

Worked very well for RD53A

Additional people added: Verification, DFT, SEU

RD53B library development

RD53B library design activity started for final production chip/s

- Design team well defined:
  - ~ 30 designers (~13 FTE)
  - ATLAS/CMS: ~ 50/50
- RD53A elements with bug fixes and technical improvements
- Small prototype submissions this summer for blocks requiring major changes
  - Bandgap + SLDO, PLL + cable driver, Thin temp sensor for pixel top, SEU test structures, (Lin FE)
- Choice of Analog FE
- Known features left out of RD53A but needed for production chips:
  - Bias of edge and top “long” pixels
  - Large pixels for outer layers (CMS, to be confirmed)
  - 6 to 4 bit dual slope ToT mapping
  - 80 MHz ToT counting (less dead time at ~same power)
  - Design for test scan chains
  - SEU hardening
  - Serial power regulator updates (bandgap, low power mode)
  - ATLAS 2-level trigger scheme
  - Optimal data formatting and compression
  - Date aggregation between pixel chips (CMS)
  - Cable driver optimization/verification with final cables
  - …

Analog FE choice

- RD53 analog Front End Review Committee (**May/June 2018**) made of:
  - Analog FE experts independent from the two experiments
  - Detector experts from ATLAS-CMS

Charge:

- Help to define key performance parameters used for the choice of FE and determine appropriate tests and simulations to be made (during May - June)
  - Initial parameter list and required tests defined
  - Many non trivial tests to be made (non uniform radiation, calibration shift over run, etc.)
- Review the three RD53A front-end designs, test results and any proposed revisions, and recommend the best suited FE for a common ATLAS/CMS readout chip. Consider performance requirements, operational needs and reliability
- If no single front-end can match all requirements without significant compromises or large design changes, suggest the best front-end for each experiment

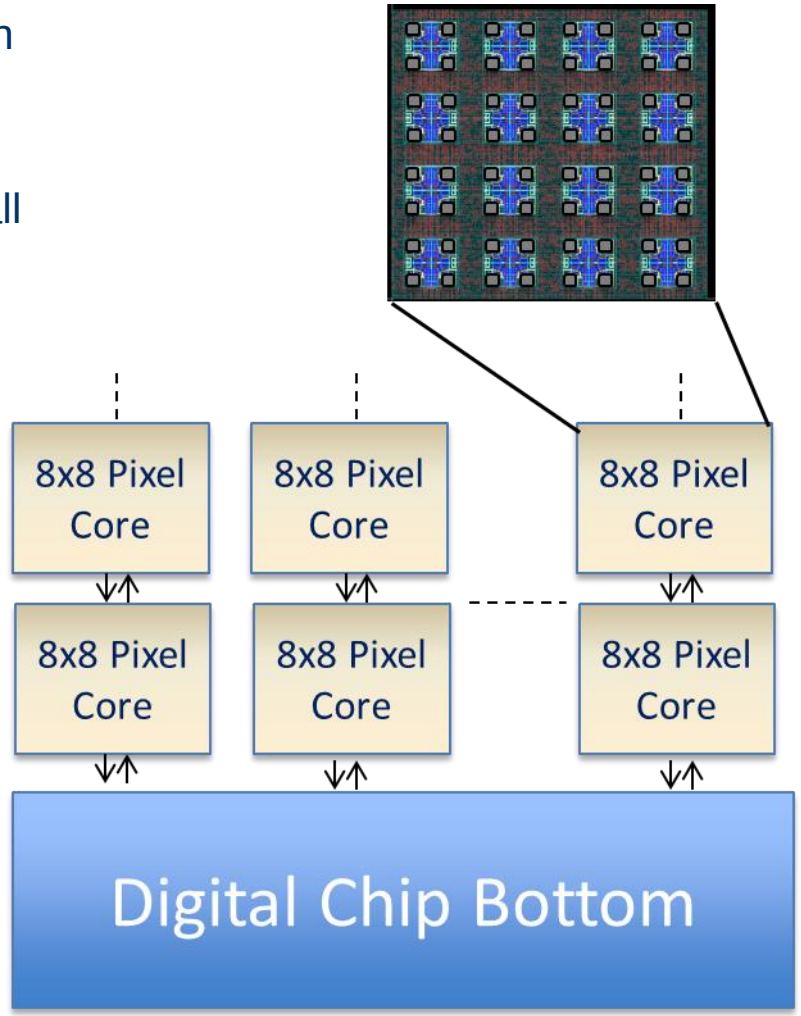
Recommendation to be delivered before November 15, 2018

1. Common FE -> Common 8x8 Pixel Core -> January 2019

2. Different FE with the same digital architecture (small difference in configuration pins)
   - ATLAS Pixel Core: January 2019 ---------- CMS Pixel Core: March 2019

Same chip, different size matrix

- RD53A chip conceived to be highly configurable in terms of size (#rows, #columns)
- Pixel Cores are stacked-up: each Core receives all input signal from the previous Core (closer to the Digital Chip Bottom) and regenerates the signals for the next Core
- Cores are abutted
  - No external routing for connections
  - Efficient hierarchical physical verifications
- Netlist parametrized with COLS, ROWS
  - 2 chips with “identical” netlist




```
for( coreColumnIndex = 0; coreColumnIndex < `COLS; coreColumnIndex = coreColumnIndex + 1) begin : CoreColumn
…
for(coreRowIndex = 0; coreRowIndex < `ROWS; coreRowIndex = coreRowIndex + 1) begin : CoreRow
```

Same architecture/Chip Bottom

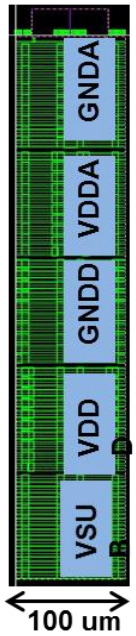
1. **Digital Chip Bottom**: Digital circuit will contain all common functions plus ATLAS/CMS specific features, to be enabled/disabled by hard-wired settings (wirebond pads)

2. Synthesis: from RTL to Gate-Level → can be initially the same, with possible specific tuning for different sizes optimization

3. P&R: identical flow/scripts, with different extracted parasitic → specific verifications (timing, power, SEU, …) will be needed

Analog Chip Bottom contains:

1. **Analog IPs assembly:** Can be exactly the same for the two chips (same blocks with same routing)
2. **Power grid**: Modular assembly, based on 100 µm wide grid cells and built using configurable scripts → two power grids with same height and different widths are easily implemented, but require **specific Power Distribution Analysis**

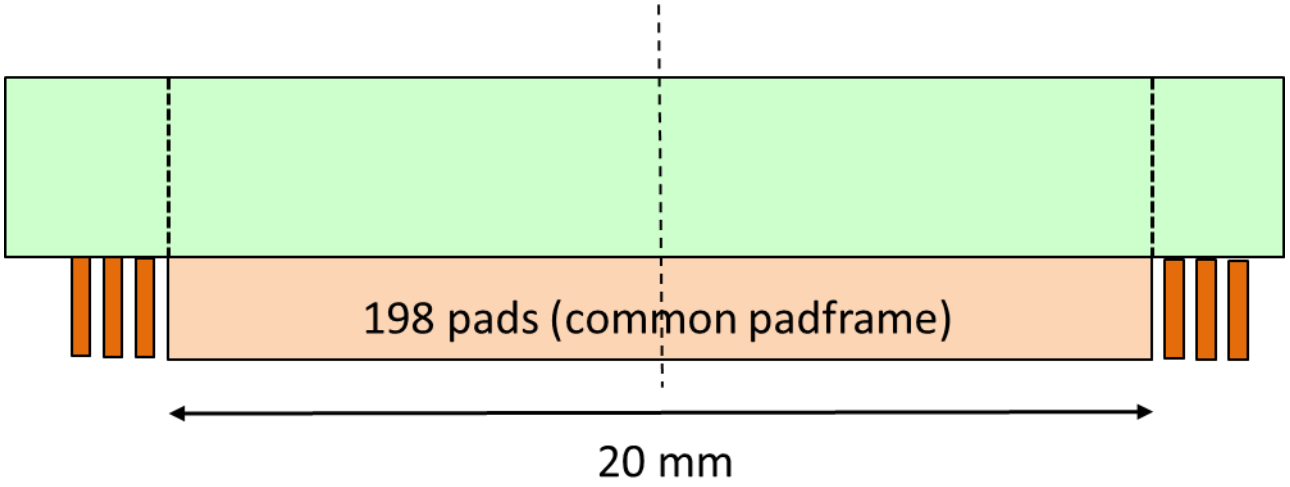


PAD frame

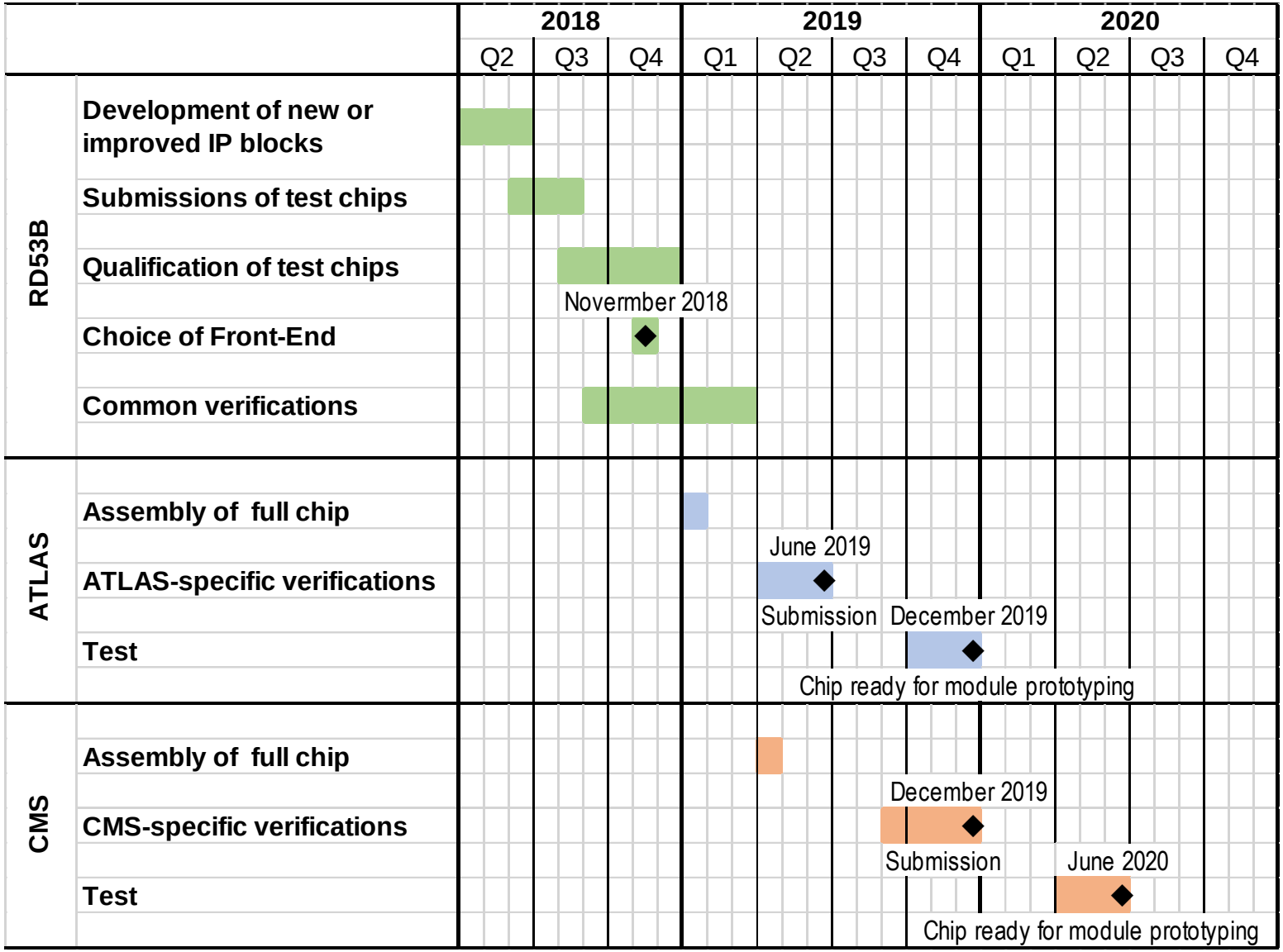
PADFRAME contains I/O pads, ShuntLDO and drivers/receivers
Two chips -> two options:

1. Same Padframe (preferred option), based on the ATLAS chip (20 mm)
   - 198 pads (120 pads for Power/Ground)
2. CMS chip (22 mm) requires 6 additional pads for data merging (space for 20 pads)
   - In case they cannot fit in the 198-version, we will add the additional pads to the left or right of common centred padframe

Padframe built by scripts -> two versions not an issue
(but requires Power Distribution Analysis/verification)



Time schedule



Summary

- RD53B library design is highly configurable and allows to implement **the same chip in two versions with different sizes with minimal overhead**
- The design team is well structured and capable to assemble and submit the two chip versions with a planning suitable for both experiments
  - Design 10 FTE
  - Verification 3 FTE
  - Test 3 FTE + ATLAS + CMS
- Tight ATLAS schedule implies ATLAS chip to be submitted first: Mid. 2019
- The CMS chip will be assembled before ATLAS chip submission, but will wait for first ATLAS tests before tape-out: End of 2019
  - ATLAS chip can also be verified/used by CMS groups
- Success is strongly driven by **Verification** for such a complex design
  - The Verification will start in 2018 during the common developments (RD53B)
  - Specific ATLAS chip verification, before its submission, will not interfere with CMS chip assembly
  - After ATLAS chip submission and during chip testing, the Verification team will focus on the CMS chip verification
  - ATLAS test team ≠ Verification team

RD53 Collaboration considers negligible the extra-risks for making two versions of the same chip instead of one single version.

Formal proposal will be submitted by RD53 before LHCC meeting in September

Formal confirmation with ATLAS and CMS experiments

Formal verification of proposal with RD53 institutes and confirmation of manpower commitments

Additional verification that common architecture can be used by both experiments

More Info

- RD53 A testing: https://indico.cern.ch/category/9316/
- RD53 conference talks: https://indico.cern.ch/category/5598/
- ACES:
  - ATLAS & CMS pixel detector upgrades: https://indico.cern.ch/event/681247/contributions/2929051/attachments/1639335/2617028/2018_04_25-aces2018_pixel_upgrade-theim.pdf
  - RD53: https://indico.cern.ch/event/681247/contributions/2929050/attachments/1639273/2616772/Loddo_ACES_25April2018.pdf
  - Serial powering: https://indico.cern.ch/event/681247/contributions/2929073/attachments/1640109/2618527/SerialPowerACES2018.pdf

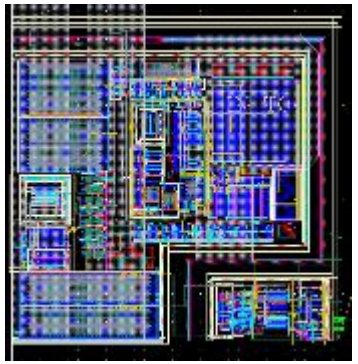
BACKUP SLIDES

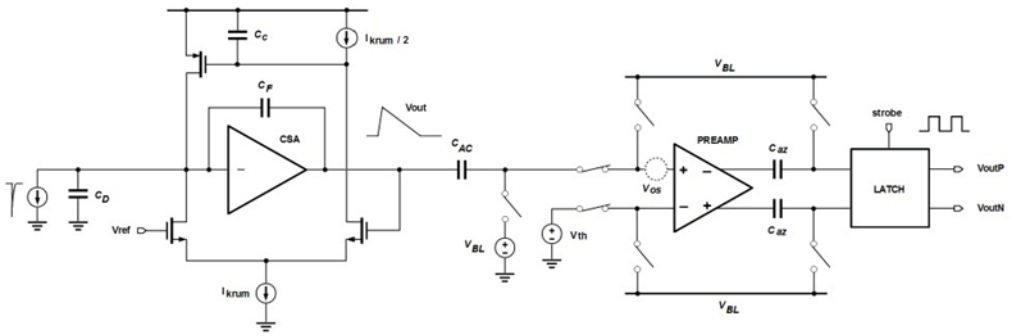
Test of Analog Front-Ends

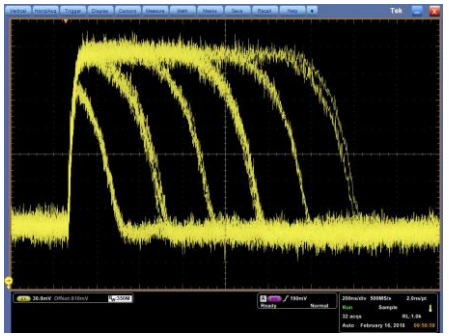
Synchronous FE

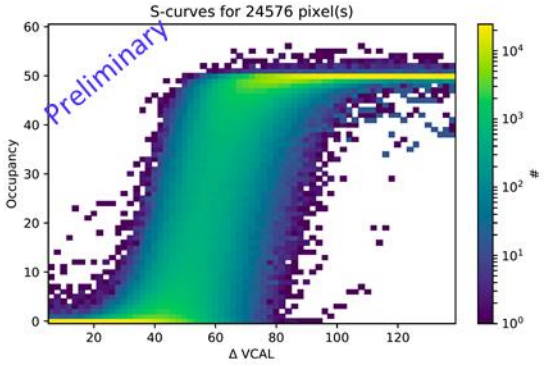
- Telescopic-cascoded CSA with Krummenacher feedback for linear ToT charge encoding
- Synchronous hit discriminator with track-and-latch comparator
- Threshold trimming using the auto-zeroing technique (no local trim DAC)
- ToT counting using 40 MHz clock or fast counting using latch as local oscillator (100-900 MHz)
- Efficient self-calibration can be performed according to online machine operations

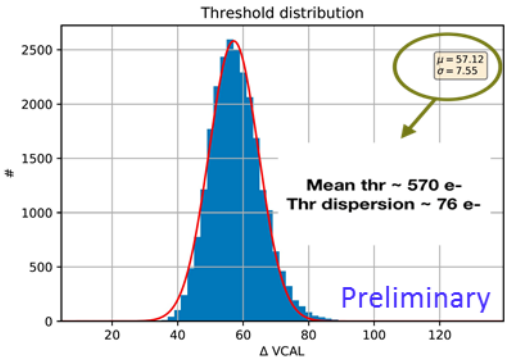
Compliant with simulations and specs: **No further prototype needed**

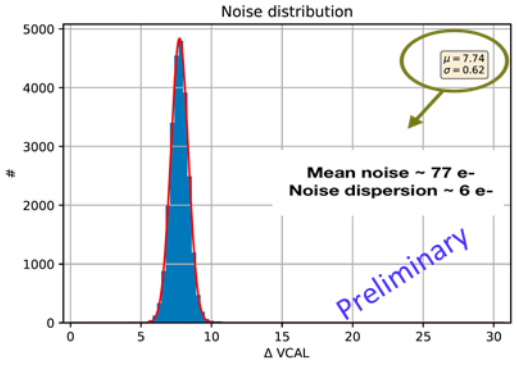








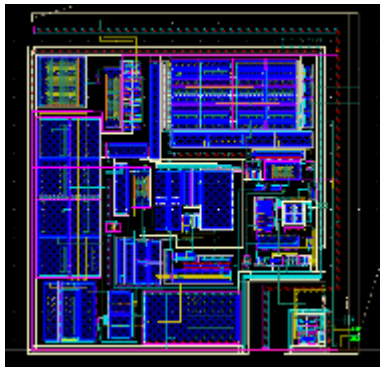


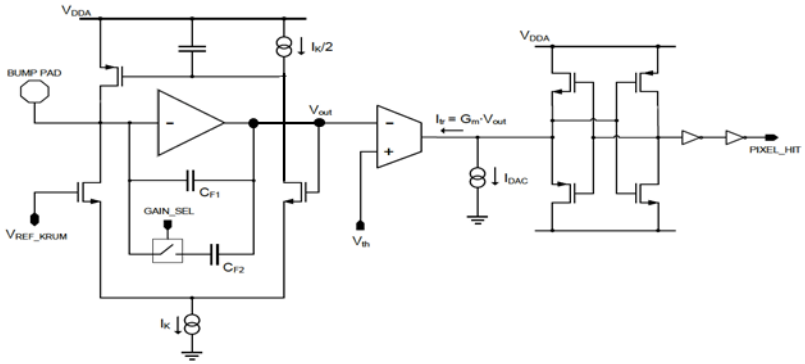


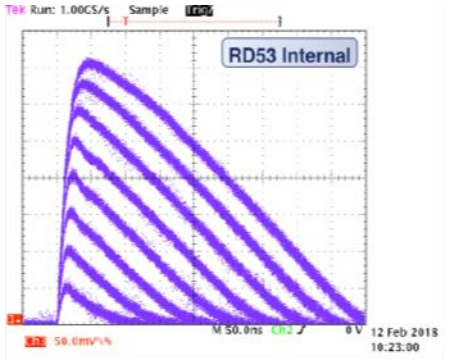
Linear FE

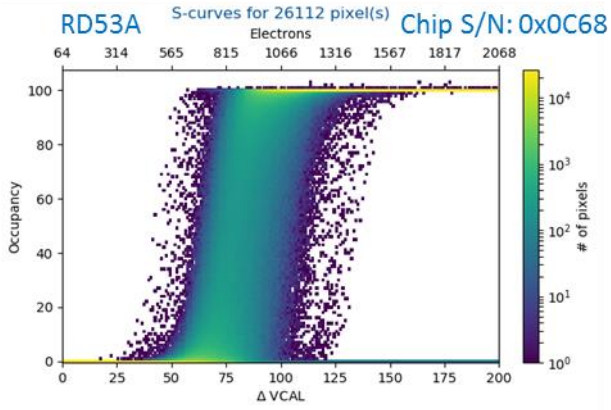
- Single amplification stage for minimum power dissipation
- Krummenacher feedback for detector leakage current
- Asynchronous, low power current comparator
- 4 bit local DAC for threshold tuning

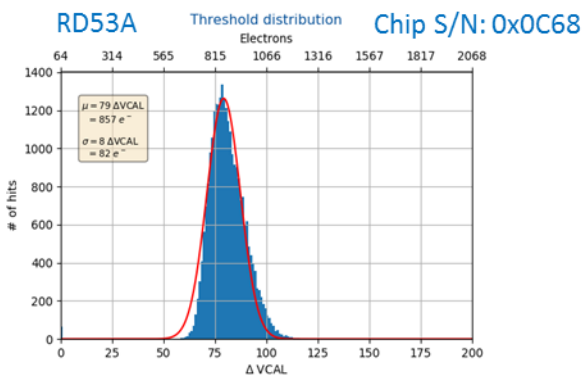
Fully functional. Tuning procedure being optimized.
Possible iteration (before summer) with extended tuning range

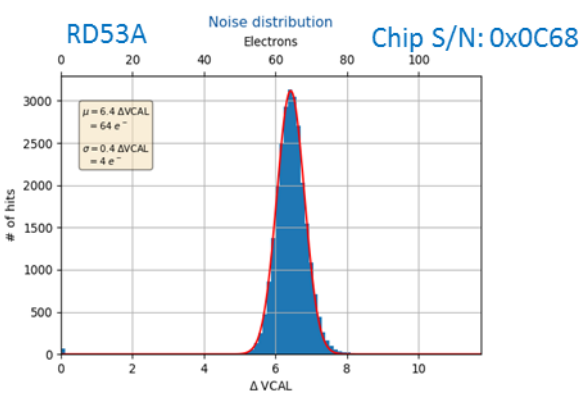






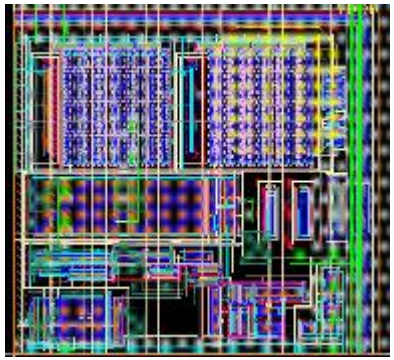


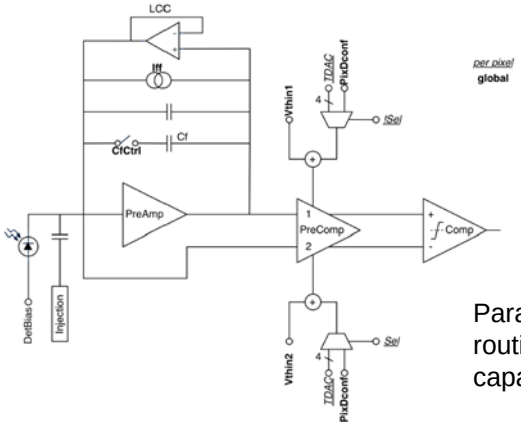




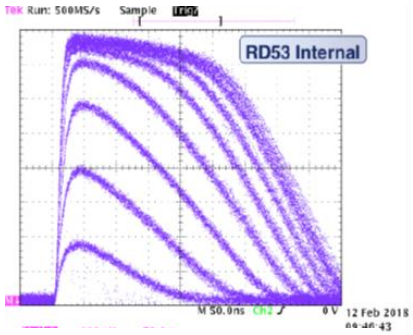
Differential FE

- Continuous reset integrator first stage with DC-coupled pre-comparator stage
- Two-stage open loop, fully differential input comparator
- Leakage current compensation
- Threshold adjusting with global 8bit DAC and local 4+1 bit DAC

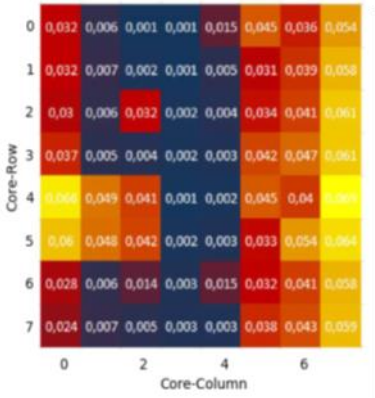




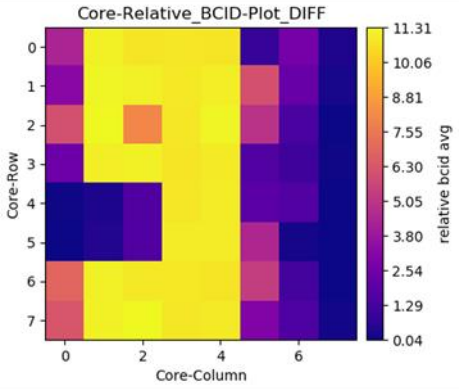
Parasitic routing capacitance



Extracted outdisc net load [pF]



- Bug in A/D interface: Missing P&R constraint on the Diff. FE hit output -> Varying load capacitance on comparator output -> systematic variation of delay and ToT
- Will improve A/D verification strategy for production chips
- Partially recovered increasing comparator bias current and decreasing preamp discharge current
- Full characterization can still be made
- Easy bug fix, so no new prototype planned

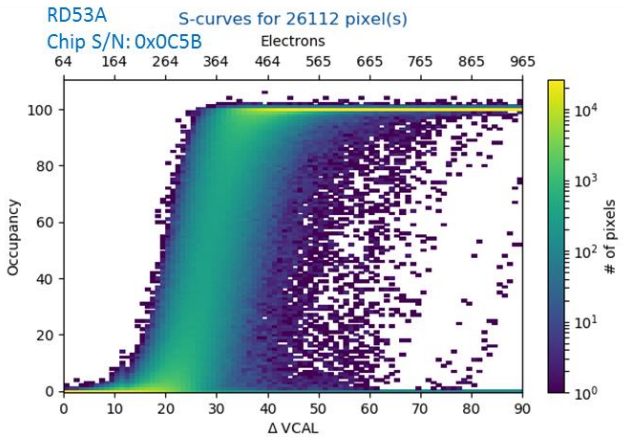


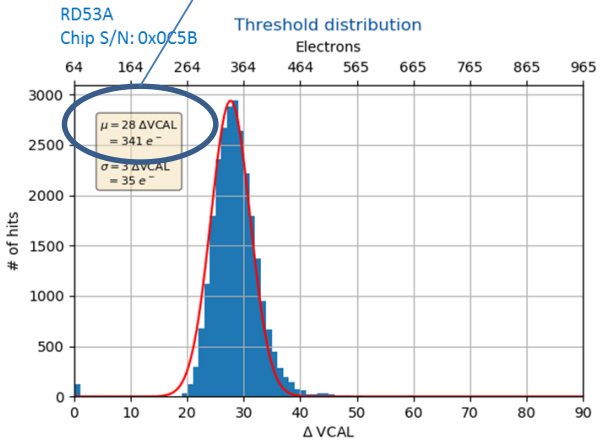
Differential FE (cont)

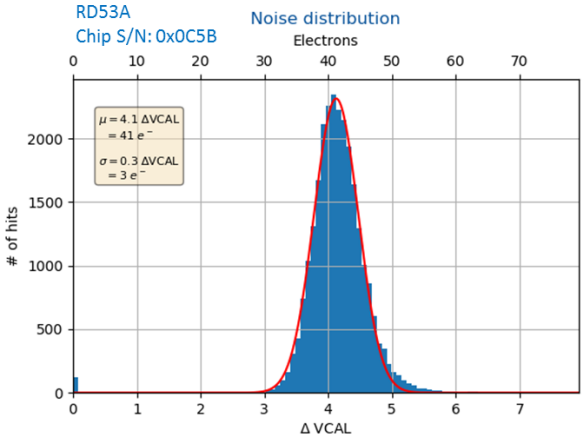
Noise based tuning

- Increased comparator current (compensate for extra load capacitance)
- Decreased discharge preamp. current

Can work with threshold as low as ~350e-







Detailed schedule

Detailed task list with 24 summary tasks and > 230 sub-tasks, with defined responsibility and time schedule

WBS	Task description	Start date	Finish date
WBS	Task description *	Start date	Finish date
1	Chip specifications	26/02/2018	30/09/2018
2	Sync Fe	01/03/2018	31/07/2018
3	Lin Fe	01/03/2018	31/07/2018
4	Diff Fe	01/03/2018	31/07/2018
6	Define comparison table of AFE	01/05/2018	15/05/2018
6	ShLDO	01/05/2018	20/12/2018
7	IPs Development	01/03/2018	20/12/2018
8	Pixel Core	01/03/2018	20/12/2018
9	SEU Strategy	1/4/2018	30/11/2018
10	Digital Chip Bottom	1/6/2018	31/12/2018
11	Analog Chip Bottom	1/3/2018	30/11/2018
12	First trial of assembly with GAFE	01/08/2018	15/08/2018
13	Modelling	1/4/2018	30/5/2018
14	IO Padframe	1/6/2018	20/12/2018
16	Choice of AFE	10/11/2018	15/11/2018
16	TOP Level assembly Atlas chip	01/01/2019	31/01/2019
17	Design readiness review	1/2/2019	20/3/2019
18	TOP Level assembly CMS chip	01/04/2019	30/04/2019
19	VERIFICATION (Common)	1/7/2018	30/03/2019
20	VERIFICATION (ATLAS specific)	1/4/2019	15/8/2019
21	Tape Out ATLAS Chip	1/6/2019	30/6/2019
22	VERIFICATION (CMS specific)	1/7/2019	30/11/2019
23	ATLAS chip basic testing	01/10/2019	30/11/2019
24	Tape Out CMS Chip	20/11/2019	15/12/2019

*RD53B requirement document for common chip under development

Cost scenarios

Cost of mask set: ~750k (25% cost decrease last year, one-off)

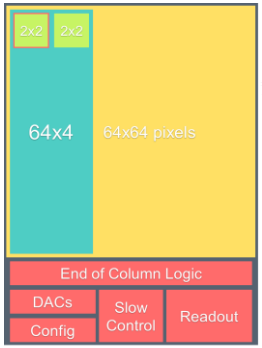
Cost of wafer: 3.5k.

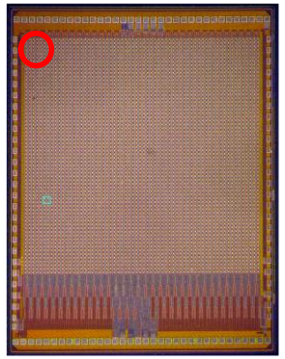
A. One single chip for both experiments:
   1. The proto chip is perfect → 1 mask set
   2. 2nd iteration to fix problems → **2 mask sets**

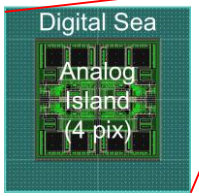
B. **Same chip with 2 sizes**:
   1. The proto ATLAS and CMS chips are perfect → 2 mask sets
   2. Find bug in proto ATLAS chip before CMS submission → 2+1 mask sets
   3. **2nd iteration for both → 4 mask sets**
      - Costed for in both experiments
        - Prototype mask set
        - Production mask set

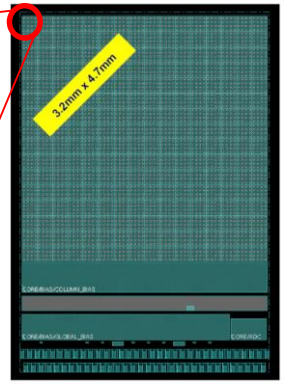
Submitted test chips

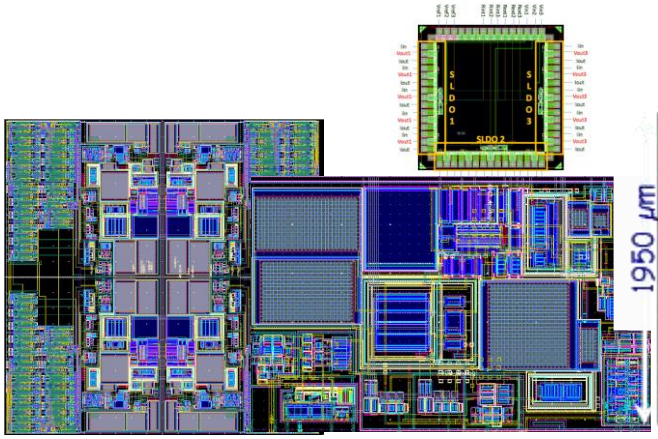
- Design, submission, functional/performance test, radiation test of many different circuits
  - Building blocks (optimized for radiation)
    - 4 different analog front-ends, DACs, ADCs, Analog buffer, PLL, Biasing, Shunt-LDO, Differential IO, Serializer, Cable driver, Power-on reset,
  - Radiation test structures:
    - Transistor arrays, Analog Circuits, Digital libraries (small transistors)
  - Two small scale (64x64) pixel arrays: FE65-P2, CHIPIX65
    - 3 different FEs
    - Analog islands (4 channel quad) in digital sea with shielding
    - Two different latency buffering architectures: Fully functional
    - Demonstrated good analog performance and radiation tolerance
- Given extensive experience to our community on 65nm technology, design tools, design repositories, testing, radiation tolerance, etc.
- Foundation for building large complex rad hard ICs

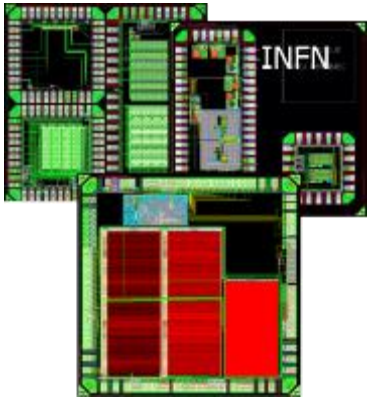


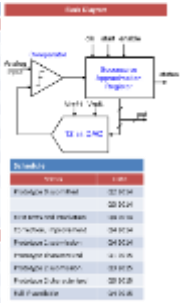








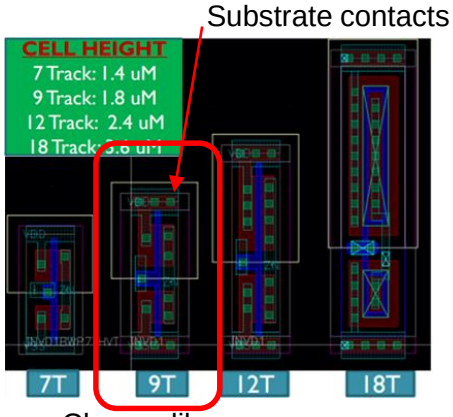




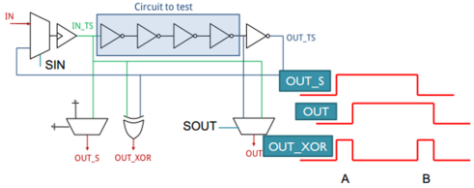
Radiation tolerance

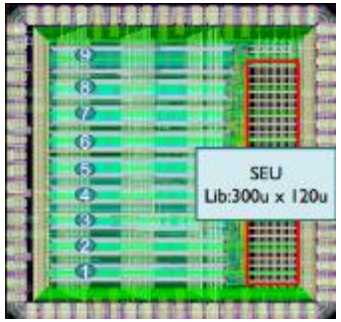
- Radiation test and qualification of 65nm technology: 1Grad and 2 10^{16} neu/cm^2
  - Radiation tests with X-rays, Cobalt source and 3Mev protons
- Significant radiation damage above ~100Mrad (only critical for pixels)
  - New radiation effects made it difficult to reach clear conclusions
- Two major “effects”
  - Radiation damage (transconductance) during radiation depends on: Device type, L, W, Bias, Temperature
  - Annealing effects depends on: Temperature, Time, Bias, Device type, L, W, Received dose
    Partial recovery (transconductance) or getting worse (V_t shift)
  - (Low dose rate effect seen. Requires long term low dose rate radiation tests)
- Realistic to stand 500Mrad with conservative design approach
  - Cold detector: -20 ^oC, Not getting hotter than room temperature while powered for limited periods
  - Analog: Appropriately designed (large transistors) will only have small radiation degradation
    - Confirmed with multiple RD53 prototypes
  - **Digital: Speed degradation when using small transistors**
    - High density logic in pixel array could have significant speed degradation.
      Only needs 40MHz operation frequency.
      High/moderate density digital library for pixel array (small modifications of TSMC lib)
    - High speed circuits designed with large transistors (high speed serializer)
    - Leakage NOT a problem in 65nm (is the case for 130nm).
    - Verified with dedicated digital radiation test chip (DRAD)
  - Inner barrel layer can be replaced after 5 years
- Conservative 200/500Mrad simulation models for circuit simulations and optimizations
- RD53A demonstrator will determine if 1Grad can be accomplished

Digital speed degradation

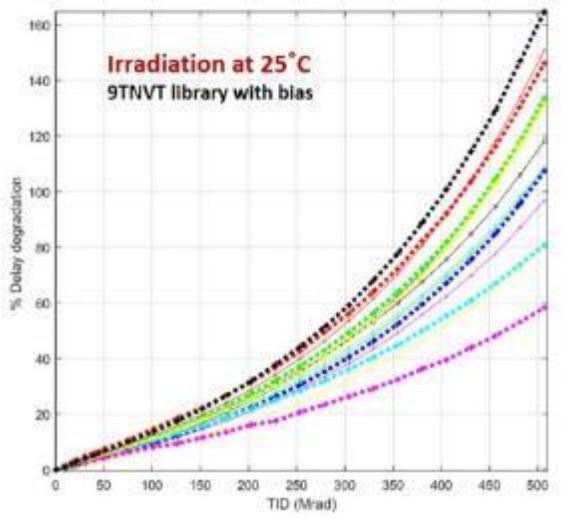


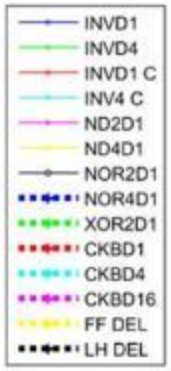
Chosen library

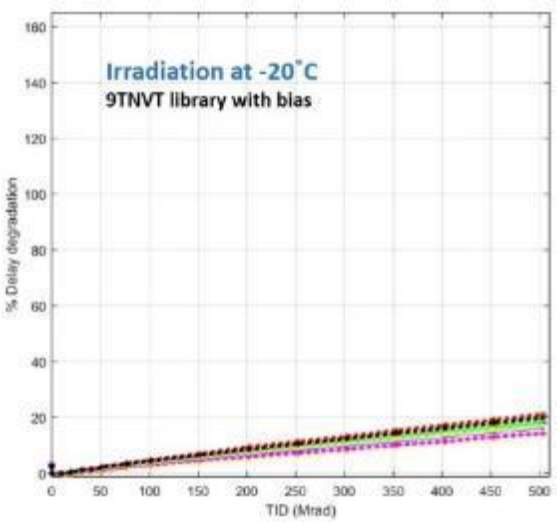


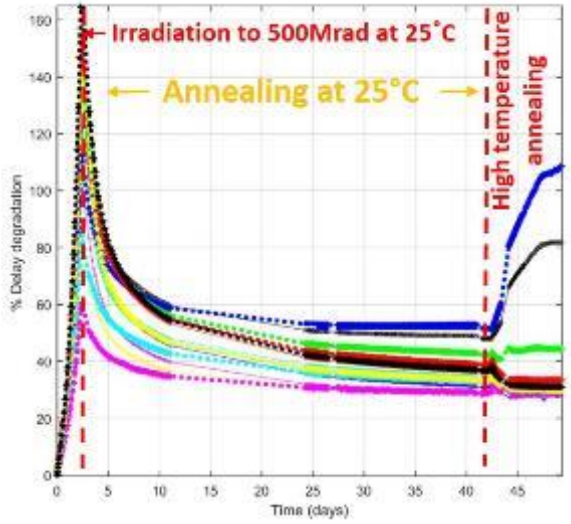


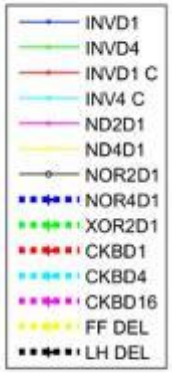
1. 7T-HVt
2. 9T
3. 9T-HVt
4. 9T-incr
5. 12T
6. 12T-LVt
7. 12T-HVt
8. 12T incr
9. 18T-ELT

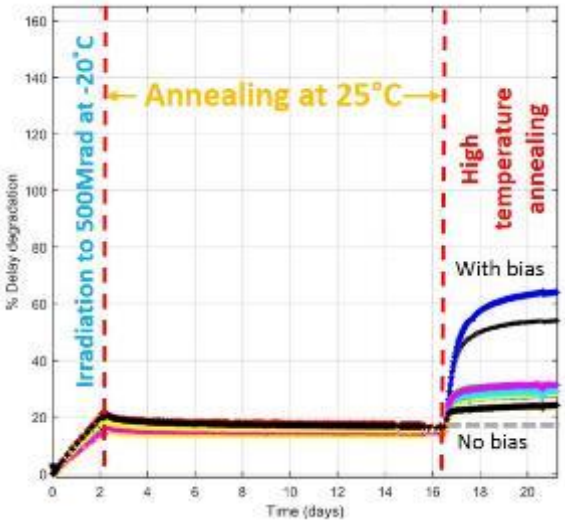




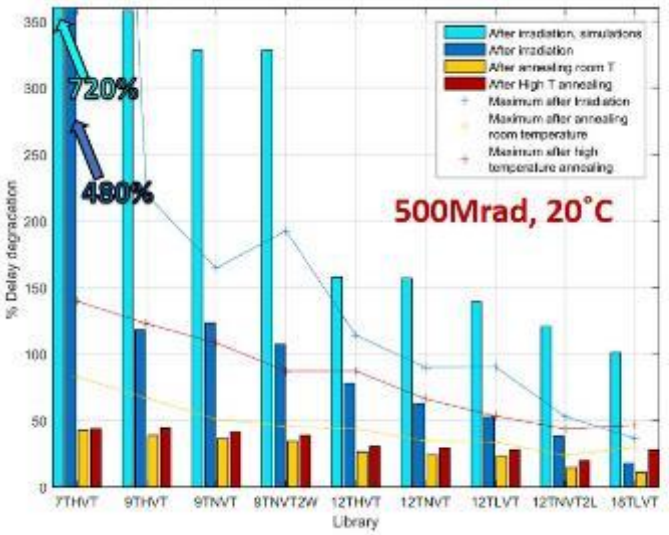


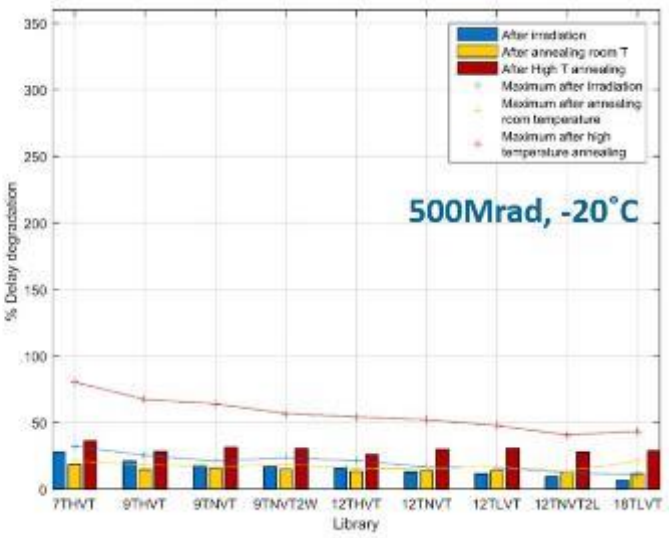


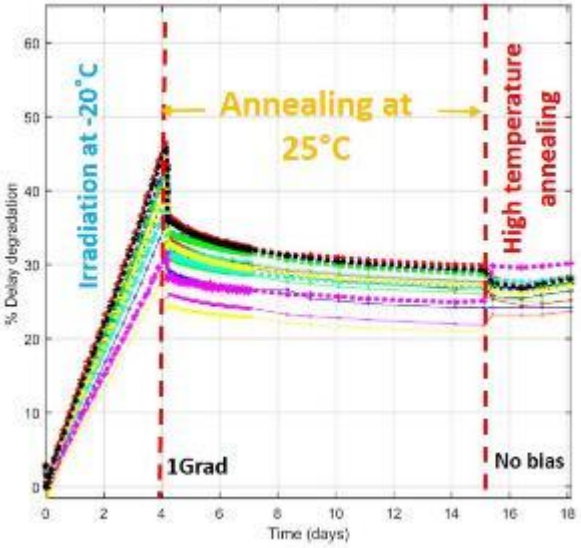


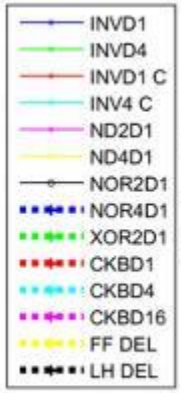


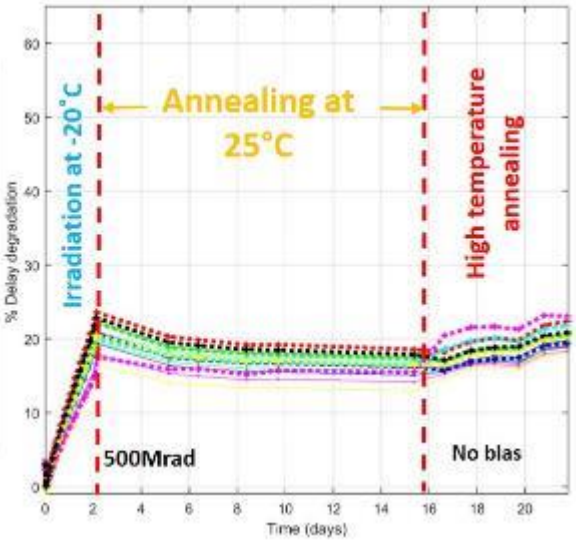
Digital lib and 1Grad ?











Extensive DRAD test results: https://cds.cern.ch/record/2242708

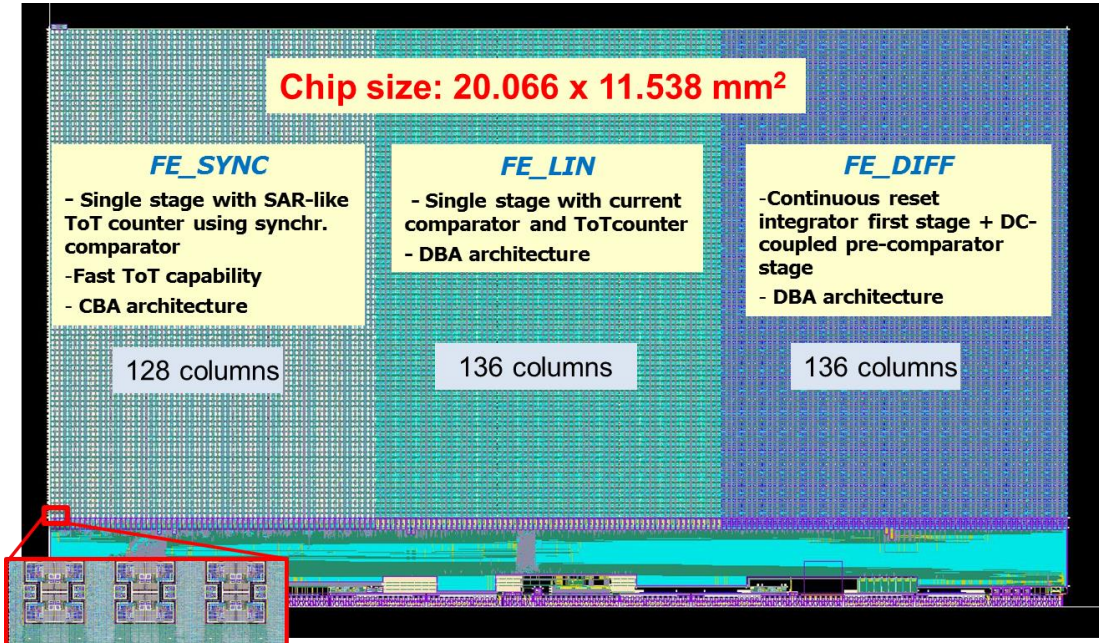
RD53A large scale demonstrator

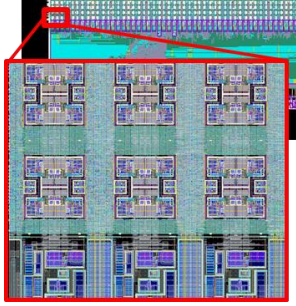
- Large complicated chip:
  - Chip size: 20mm x 12(20)mm, small pixels (50x50um^2), 3 alternative analog FEs.
    Two alternative buffering scheme. Very high hit and trigger rates, Radiation and SEU tolerance,
    600e- threshold, 1200e- in-time threshold, “Low” power, Serial powering,
    Extensive analog and digital monitoring, Calibration features, Fully functional in test beams, etc.
- Specification document agreed with CMS and ATLAS phase 2 pixel communities:
  https://cds.cern.ch/record/2113263
- Core design team of ~10 designers for ~1year
  - 9 months remote collaboration with weekly meetings, common repository, Gitlab, blog, Emails, etc.
  - 3 months together at CERN with daily coffees and weekly meetings
  - 3 months for extensive verification: multiple problems and bugs resolved
  - Not forgetting major work before on radiation, IPs, simulation framework, prototypes with testing, ,
- Engineering run ~1M$ (last minute 25% reduction):
  - Shared run with other projects: CMS MPA/SSA,
    Clicpix, Pixfel, RD53 small pixel arrays,
    Radiation test structures
- Implementation document of ~80pages
- **Submitted last week, chips back in November**

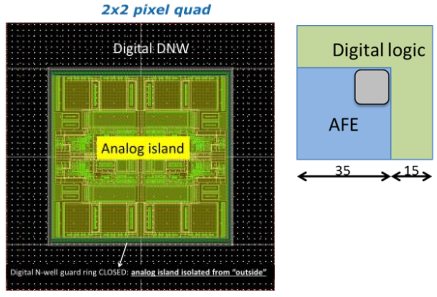
Basic specs

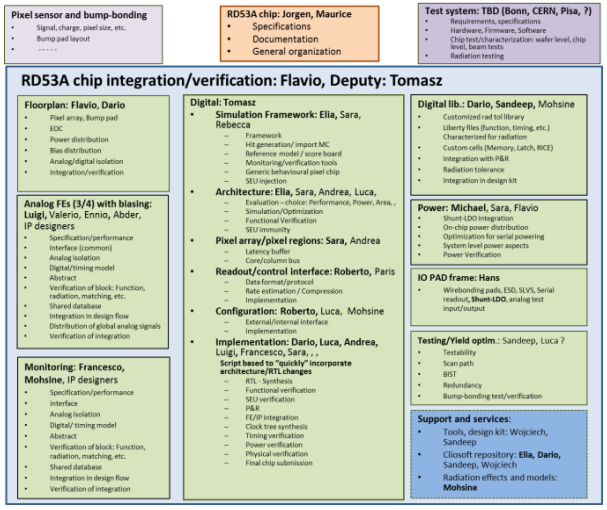
Technology	65nm CMOS
Pixel size	50x50 um^2
Pixels	192x400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	<1200e-
Noise hits	< 10^{-6}
Hit rate	< 3GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500Mrad, 1 10^{16} 1Mev eq. n/cm^2 at -15°C
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1W/cm^2 including SLDO losses
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

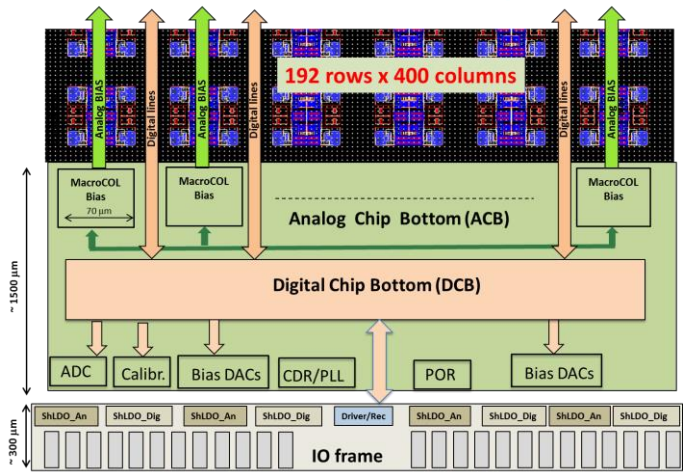
Implementation

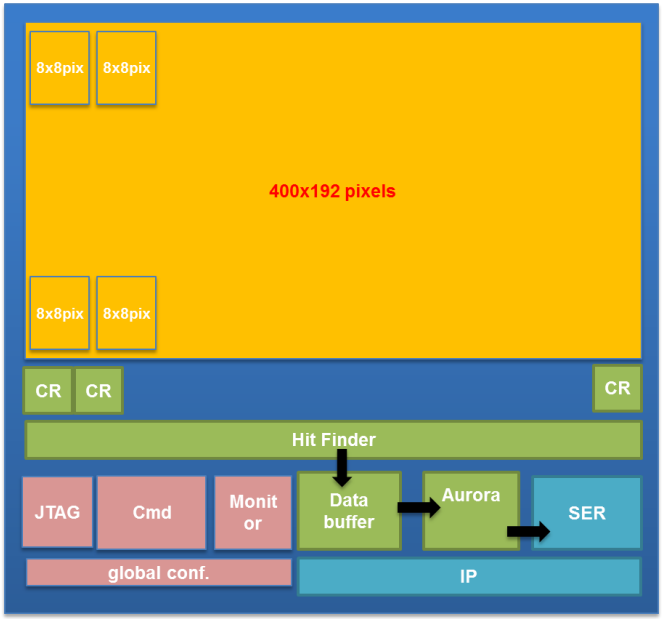






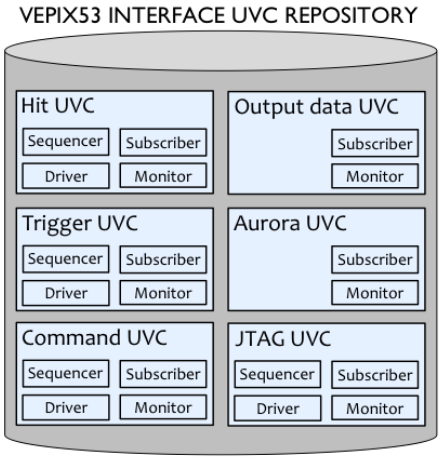


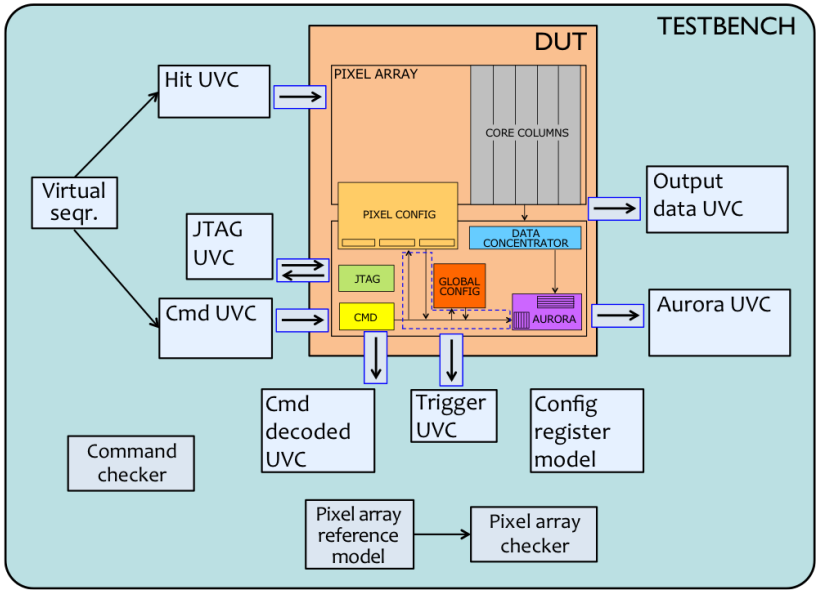




Verification

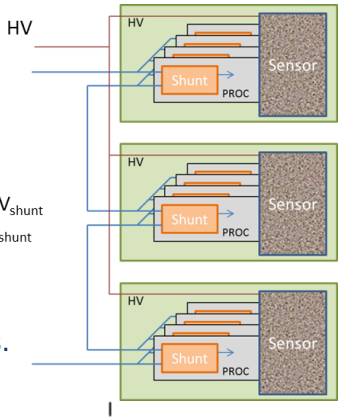
- Analog simulations
  - Analog blocks
  - Multiple analog blocks
  - Pixel core with both analog and digital
  - Availability of conservative radiation models
- Timing verification of digital
  - Challenging for large chip when taking into account radiation damage
- Formal equivalence checking (after synthesis)
- VEPIX53 simulation and verification framework: System Verilog & UVM
  - Developed/used in RD53 during last 3 years
  - Architecture optimization and verification
  - Debugging during design
  - Final design verification
    - Behavioral level, RTL level and Gate level
    - Driving mixed signal simulations for analog blocks (FE, biasing, monitoring, etc.)
    - Driving power simulations/verifications
    - Global tests with hits and triggers at different rates
      A. Internally generated hits
      B. Monte Carlo hits from detector simulations
    - Directed tests for specific functions
    - (SEU simulation: to come)
- Critical for design verification
  - Many major and small bugs found and corrected during whole design process and in particular during last 3 months for final verification
  - Even more effort must be put on this for verification of final chips



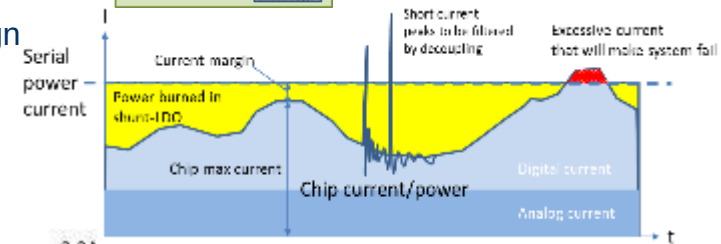


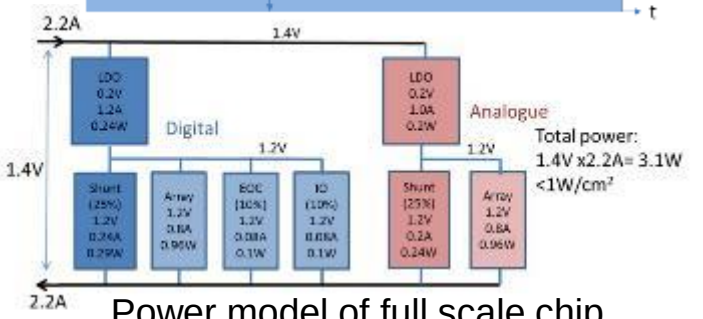
RD53A serial powering

- Serial powering critical for low mass power distribution:
  - ~10k chips of 3W = ~30kW in ~1m^3 ,
    ~10K chips of ~3A = ~30kA over 50-100m cables
- Integration of Shunt-LDO in pixel chip critical
  - SLDO prototypes (0.5A and 2A): Works as simulated
    - Radiation, Noise coupling, Failure modes
  - Improvements made of SLDO for RD53A:
    - Improved control loop to assure stability with capacitive loads.
    - Configurable voltage offset of SLDO impedance
  - Extensive system simulations made with detailed SLDO design and detailed power profiles from detailed chip design: Analog and Digital power
  - Verification of local thermal hot spots (to be extended)
- Power "model" of full sized pixel chip available

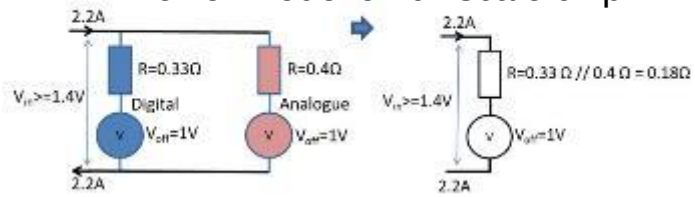


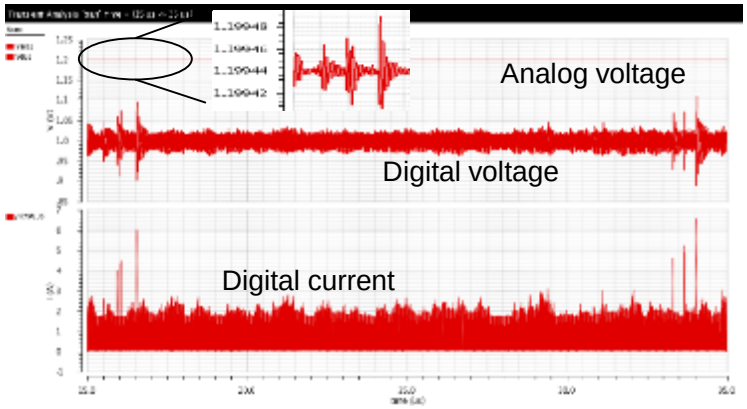
SLDO testing





Power model of full scale chip

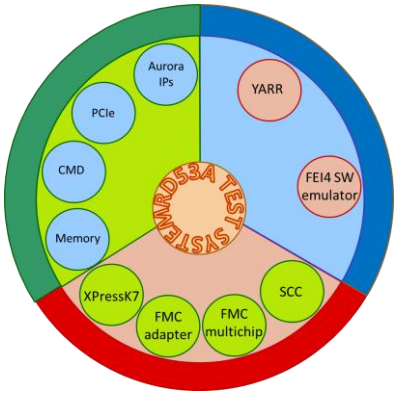


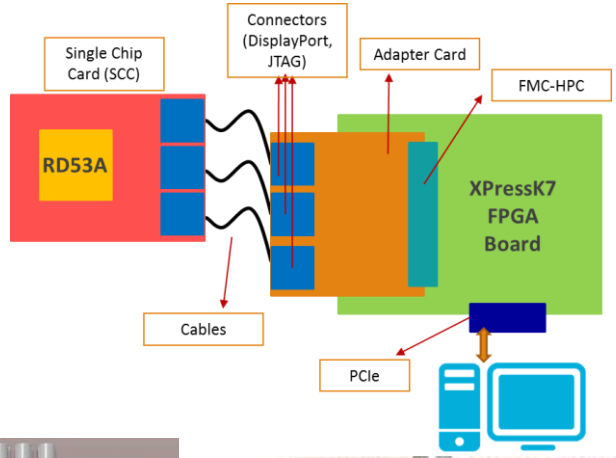


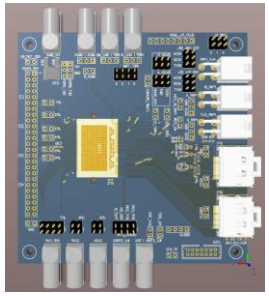
Serial power simulation: System, shunt-LDO, chip

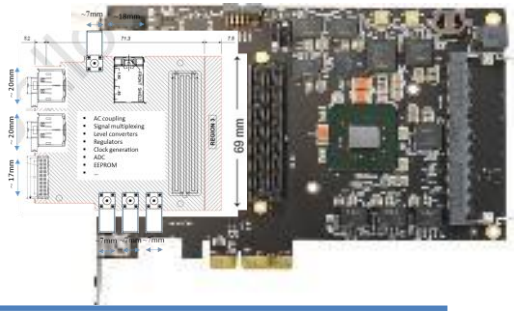
RD53A test preparation

- RD53A test working group preparing testing
  - Chips will come in November
  - Also ATLAS/CMS groups in formally in RD53
- Test systems being prepared:
  - A. PC plug-in Hardware:
    - Commercial PCI-E FPGA card
    - Custom FMC adapter card
  - B. Standalone custom card: Ethernet
  - Single chip card with standardized interface:
    - Command/clock line and Readout link(s) on standard display port cable
    - Power prepared for serial powering
  - Multi-chip hybrids: In the pipeline for later tests
  - Firmware,
  - Software
  - Based on previous experience with FEI4 test systems
- Pixel sensors being produced in both ATLAS and CMS.
- Bump-bonding being prepared
  - RD53A dummy wafers and sensors for initial trials
  - 300mm wafer handling in HEP community and BB companies
    - Community getting equipped with 300mm wafer probers
- Radiation testing
- Many systems will be used in ATLAS/CMS pixel community









Final CMS and ATLAS chips

- Final CMS and ATLAS chips
  - Differences:
    - Chip size (can unfortunately not fit both on common reticle)
      - CMS: ~22 x 16.4 + 2 mm^2
      - ATLAS: ~20 x 20 mm^2
    - Hit rates: 3GHz/cm^2
      - CMS (r=3cm), ATLAS (r=4cm)
    - Readout interface:
      - CMS: 4 x 1.28Gbits/s to LPGBT module with opto conversion(~0.5m).
        Number of links according to location 1, 2, 3, 4
        Data merging on pixel chip between up to 4 pixel chips to shared link (outer layers)
      - ATLAS: Single 5Gbits/s to patch panel (6-8m)
        Opto conversion on patch panel
    - Latency buffering
      - CMS: 1 level trigger: 12.8us , 750KHz
      - ATLAS: 2 level trigger for possible future upgrades
    - Analog Front-end: Each experiment will choose most appropriate analog FE

  Common chip seems impossible/difficult
- Many common issues
  - Building blocks: Support, integration and verification must be assured for both designs
  - Radiation effects: TID and SEU
  - Serial powering and power optimization.
  - General architecture, configuration, Monitoring, Data merging, Data compression
  - Design approach, Global floorplan, Synthesis & P&R scripts, Verification framework, , ,

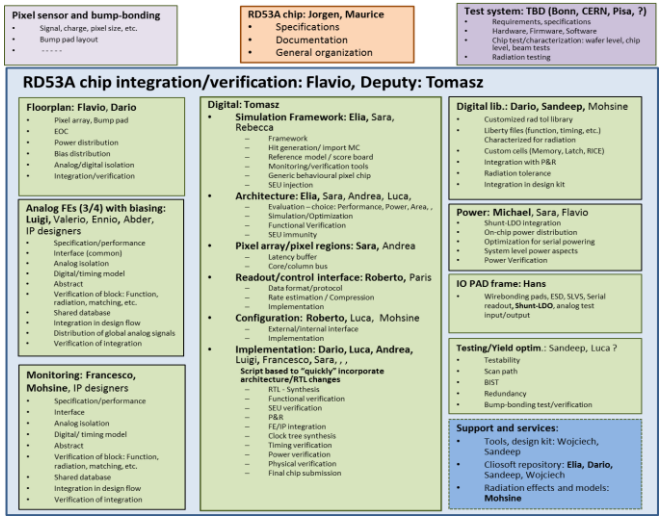
Proposal

- Design ATLAS & CMS chips within RD53
  - Common design framework
  - RD53A was a common design framework mapped into one physical chip
  - Updated common design framework can be mapped into two different physical chips
  - Common design framework with dual responsibles for major parts.
  - Dedicated teams for final implementation and verification
  - Schedule sketch
    - 2017: Finalize specifications of both chips
Extended architectural simulations
Incorporate experience and test results from RD53A
    - 2018: Design and finalization of common design framework
Extended optimization and Verification framework
Extended SEU protection and verification
Mapping into generic implementation (like RD53A)
    - 2019: Mapping into CMS and ATLAS specific implementations
Exhaustive verification and submission
- We will profit a lot from common IP blocks, architecture, design expertise, verification, testing and qualification, etc.
- RD53A team worked very well across CMS – ATLAS boundaries.
  - Helped a lot bringing team physically together for extended period (4 months at CERN)

Experiments represented by RD53 co-spokes persons	CMS	ATLAS
Integration		
Digital design		
Analog integration and verification		
Control, readout and IO interface		
Analog front-end		
Chip verification		
Serial powering		
Radiation hardness		
Common IP blocks	One per IP block	

In the process of assigning names
(most names known from RD53A)

We had similar structure for RD53A



Summary and outlook

- RD53A has been successfully submitted
  - Huge design, verification and testing efforts
  - Team worked very well across ATLAS – CMS boundaries
  - This was the principal milestone of the RD53 collaboration
- RD53A testing is being prepared
  - Many ATLAS and CMS pixel groups will do chip, sensor, pixel module, serial power and system tests with this chip in the coming months - years
- Better understanding of radiation issues
  - Radiation when cold and no bias when at high temperature assures 0.5Grad (possibly 1Grad) radiation tolerance
- Propose to develop final ATLAS and CMS pixel chips within RD53
  - Common design framework (as for RD53A)
  - Final mapping into two dedicated chips
  - Project structure and responsible will be finalized in coming RD53 collaboration meeting (November)
- We formally request the RD53 collaboration to be continued for the final CMS and ATLAS chips
  - Supported by both ATLAS and CMS experiments
  - Supported by RD53 collaboration members (18)

    Additional institutes (2-4) want to join for development of the final ATLAS and CMS pixel chips