Status of the FPGA based module

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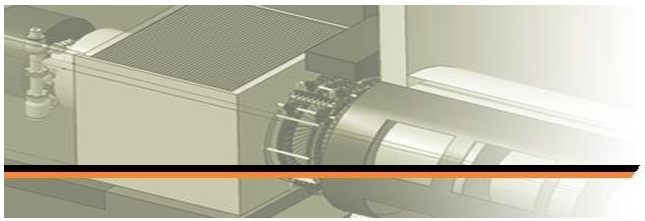

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SETUP

AC701 evaluation board is based on XC7a200YT Xilinx Artix 7 architecture FPGA

8 GTP ports - high speed serial transceivers – max. transfer 6.6 Gb per port – which allows to operate in test conditions with 20 MHz sampling frequency

Each port contains two pairs of signals: for transmitter and receiver.

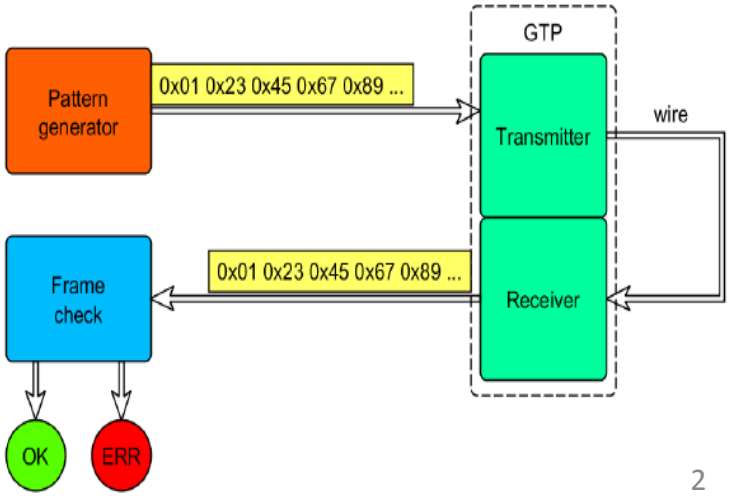
External loopback on SMA connector

Firmware based on Xilinx Vivado

The current prototype uses only 1 port: enough for testing communication, develop data preselection and uploading data to an external storage (PC) over an Ethernet connection

Test of the transmission using generated data

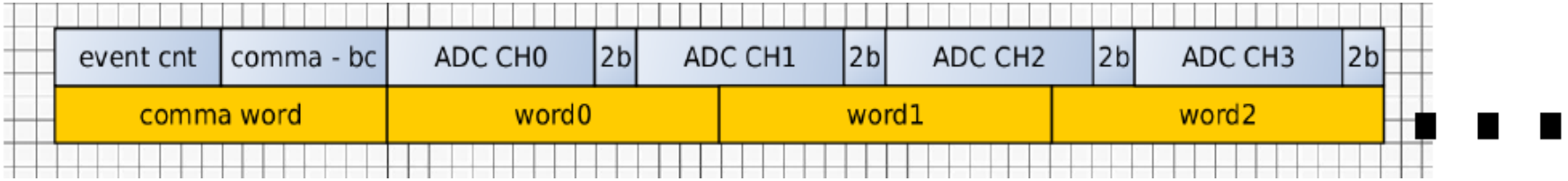
Checking the identity of sent and received data



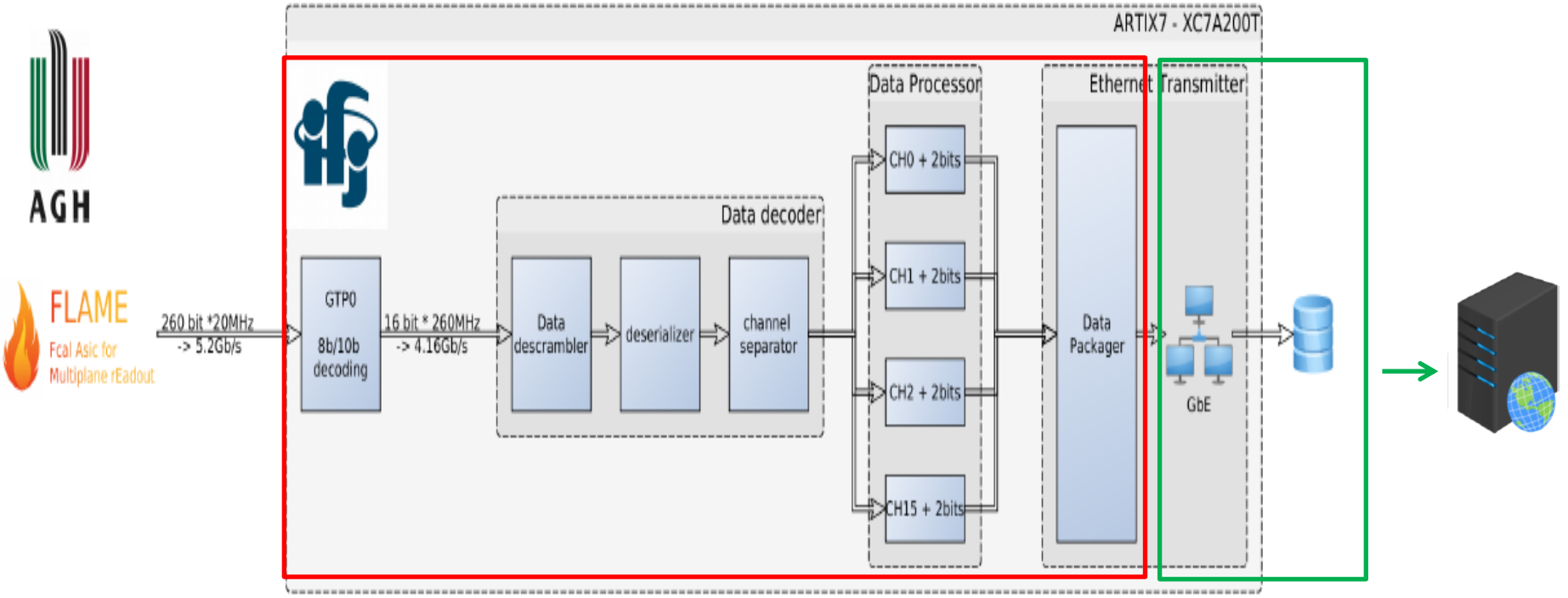
Data Format

Initial data format used in simulation

Modified data format



Data Flow: from FLAME to PC



RP module
(Reading and processing FLAME data)

GbE module
Allows for data transfer via Ethernet

Initial steps:

- deserializes incoming data from GTP
- separates each ADC channel for data processing
- takes clock from GTP
- put data to some buffer inside FPGA

The final step:

- Gigabit Ethernet module
- data analysis using PC

RP module

GTP0 module

- reads data directly from the FLAME system (ASIC)
- decodes the signal (8b/10b)
- gives 16-bit words on the output.

The received signal have proper or mixed bit structure and needs to be corrected (aligned data)

Data decoder

- receives data from GTP0
- arranges them if necessary (data descrambler)
- makes deserialisation: creates vector of bits corresponding to one event (192 bits, deserializer)
- and makes synchronisation data (comma_resync module which is connected to data procesor)

Data procesor

- separates the data vector into individual channels (channel separator)
- compares the input data with values set by proc_driver and generates a vector with information about accepted words (comparator)
- makes synchroniation data received from data separator and comparator
- creates again one wide vector of data which can be send outside (data combiner)

element proc_driver makes control over data procesor

Data packager

- divides data into 32-bit words which are compatible with Ethernet protocol

The creation of the GbE module will enable data transfer via Ethernet

GbE module : for communication in the Ethernet standard

Key features:

- Gigabit Ethernet with UDP/IP (User Datagram Protocol) stack
  (connectionless protocol for sending data packets, here: ASIC data)

- Good functionality:
  - Implemented as pure logic FPGA
  - No integrated microcontroller required
  - Portable between various FPGA platforms (as logic is independent of equipment)
  - Economic resource usage
  - Full-duplex at 118 MBps (high speed and two-way communication)
  - Multiple parallel instances (programming)

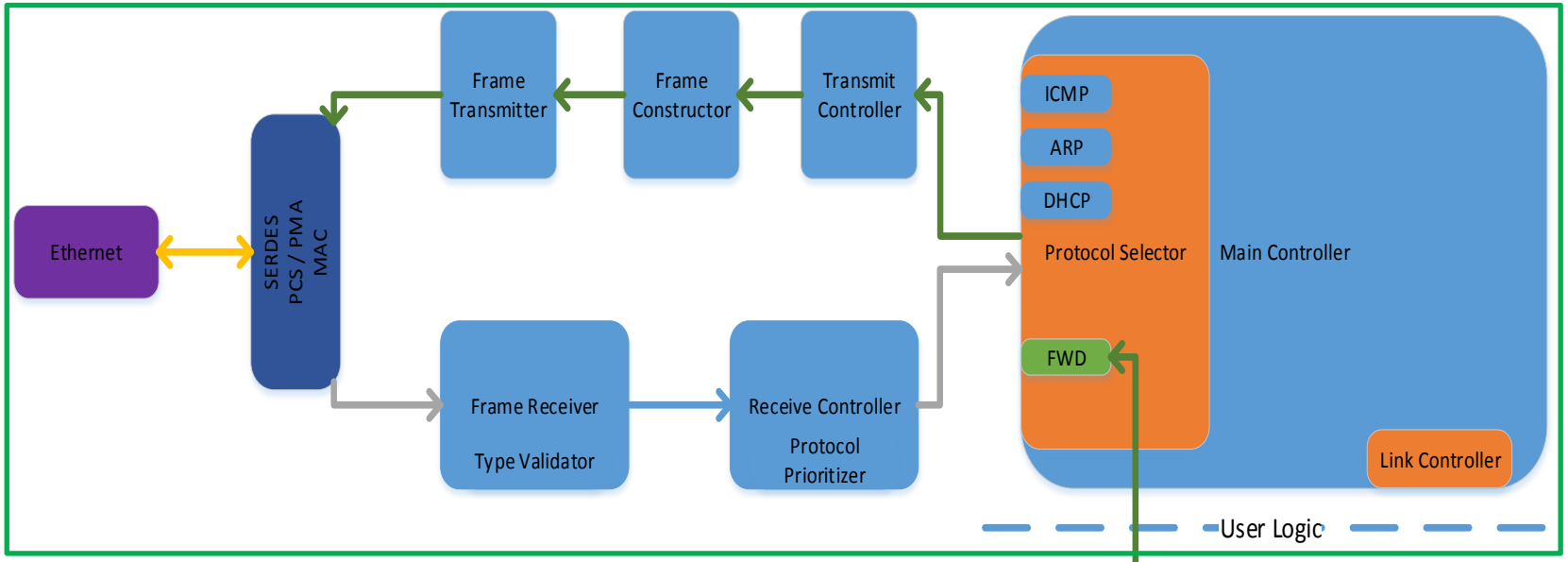
- Basic network protocol

  - Network discovery (It allows collects the information about devices on our network. Protocols needed for active participation in the Ethernet network so that other devices know who sends packets and to whom they should be sent). They are:
    - ARP (Address Resolution Protocol: connects hardware MAC address with logical IP)
    - DHCP (Dynamic Host Configuration Protocol: allows assign IP addresses to new devices)
    - ICMP (Internet Control Message Protocol: controls the connection, command PING as example to check if the device corresponds and is visible in the network)

  - User protocol (receiving and transmitting data in the form of UDP packets)
    - UDP receiver with fragments reassembly
    - UDP tramsmitter with payload fragmentation
      The maximum packet for UDP – 65 kB , for Ethernet usually 1.4 kB
      For tramsmission: dividing the UDP packet into smaller ones
      For receiving: merging into one large UDP packet

GbE module

FLAME data saved to the buffer by **RP FPGA module** are read by the **GbE module** and sent to the network.
The buffer is on the User Logic line and the Main Controller is the block that builds the UDP packets.
FWD (forward) protocol: sending ASIC data straight to the network.



- Medium access:
  - Hardware embedded transceivers (GTP on Artix7)
  - SERDES (pairs of modules to compensate for limited I/O in communication)
  - PCS/PMA core (implemented as hardware (inside FPGA) or as logic)
  - MAC (hardware or logic)
- RX path
  - Packet type and addresses filtration
- TX path
  - Packet construction and payload fragmentation
  - Encapsulation with headers and addressing

- Main Controller (contains implementations of all protocols)
  - Controls the link status
  - Redirects data to designated protocol module
  - Activates User protocols

Summary

- The work on the FPGA module is on going

- Previously obtained results were related to the RP module and concerned:
  deserialization data coming from GTP
  data separation for each ADC channel for data processing
  saving data to the buffer that will be used by the GbE module

- The recent work concentrated on GbE module for smooth transmission through Ethernet

- The final step:
  work on general optimization and integration tests with FLAME test board