NSW Trigger Processor Carrier Card v2
High-Level Specification

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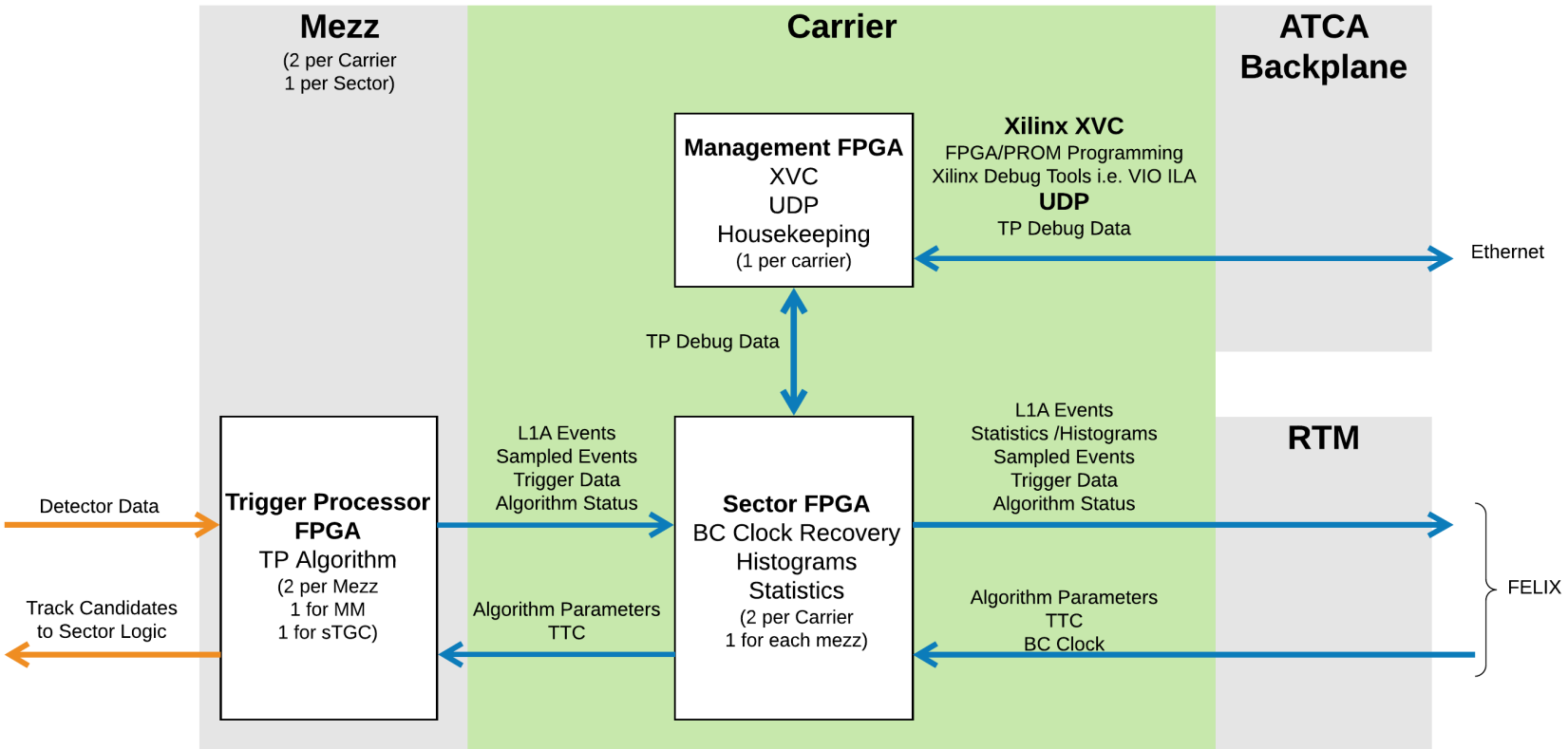
Overview of NSW TP Carrier Card

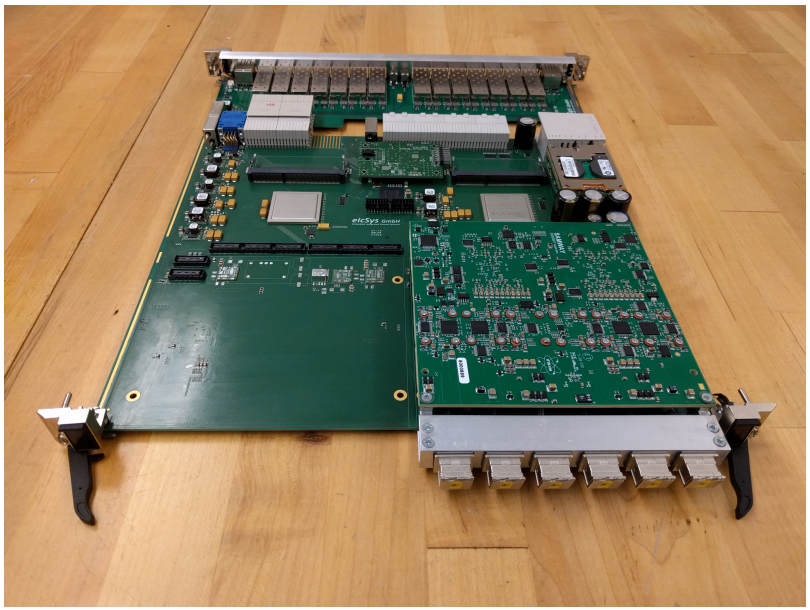


- Each carrier board processes two sectors
  - Recall two mezzanines per carrier board → each mezzanine has 2 FPGAs (one for MM and one for sTGC)
- Carrier board consists of 2 main FPGAs (1 per sector) and 1 management FPGA

NSW TP Carrier Card Functionality

- Functionality of Sector FPGAs
  - distribute clocks – BC (40.079 MHz, recovered from FELIX or from a local oscillator), Ethernet and ATCA Backplane clocks.
  - supports trigger algorithms running on the Mezzanine FPGAs
  - monitor and configure the trigger algorithm
- Functionality of central management FPGA
  - sensors monitoring
  - hardware configuration
  - communication through regular network protocols (TCP stack)
  - algorithm debugging
  - remote FPGA configuration and low-level debugging using remote JTAG based on Xilinx Virtual Cable (XVC)

Motivation for Carrier Card v2



- COTS (carrier board + RTM)
- 1 big FPGA per sector
- 1 small FPGA for management
- Plenty of links on RTM

The upgrade is necessary since the current carrier board has the following limitations:

- Its Virtex 6 and Spartan 6 FPGAs are not supported by current Xilinx tools.
- Limitation in clock resources and flexibility.
- XVC support is desirable in hard-to-access environment as the ATCA standart but implementation not straightforward
  - Separated XVC services running on soft processors implemented in the Sector FPGAs. Spartan 6 not included.
- Dificult debug paths with low-level and limited dataflow control.

- **Specifications for carrier card v2 based on the experience with the current card.**

Constraints for deriving the specifications

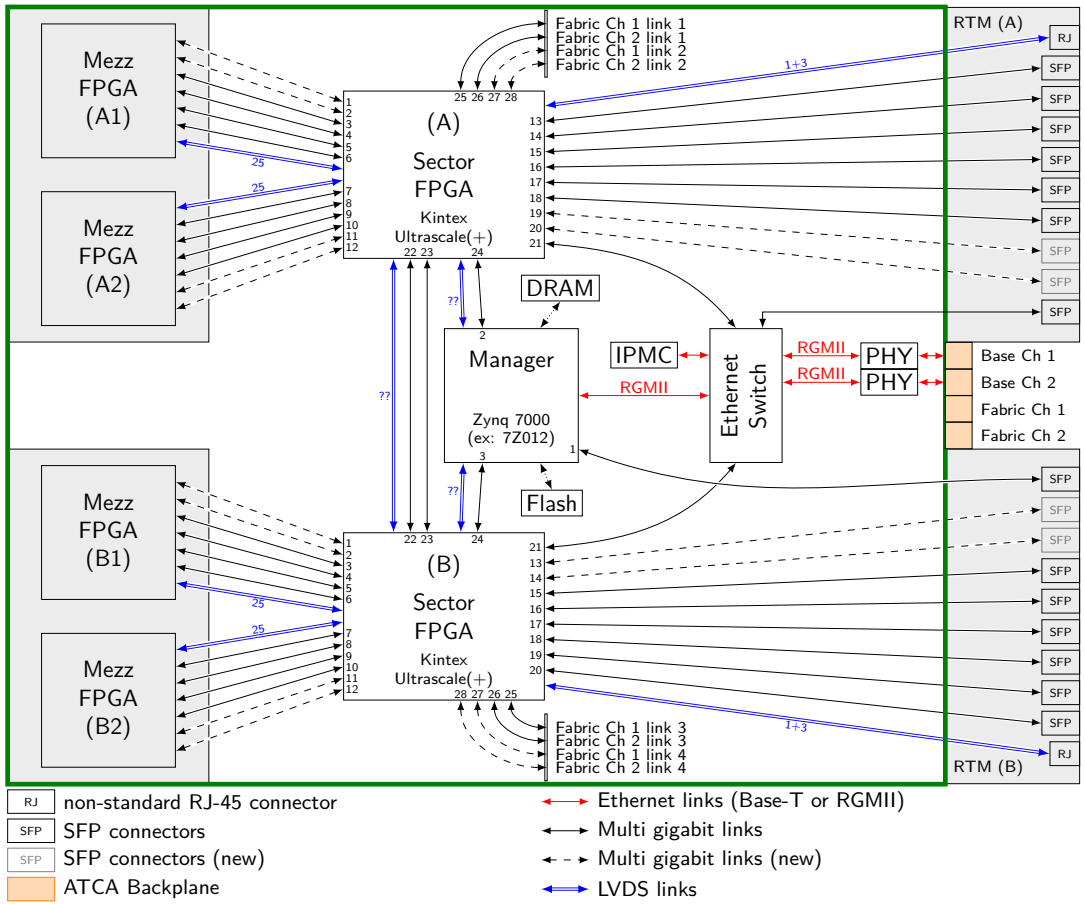
General constraints

- Do NOT reduce bandwidth between sector FPGA and mezzanines.
- Use previous design as base (components and capacities known).
  - Carrier board shall comply with requirements of ATCA standard
- New devices should be available in development kits
  - Development possible during board design.
  - Working designs as reference.
- More flexible central management unit (CPU+FPGA)
- Optional Ethernet access through ATCA backplane
- As flexible and redundant as possible due to short deadlines

Additional mechanical constraints

- Satisfy the mechanical requirements of the ATCA standard
- Design shall be compatible with existing designs, including pin connector definitions
  - NSW TP mezzanine, Rear Transition Module (RTM)

Interconnections



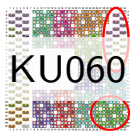
- Several requirements for interconnections: Ethernet, serializer, backplane links.
- LVDS signals: shall cover existing signals for the Mezzanines, RTM and foreseen management functions. The remaining LVDS signals shall be evenly distributed between Sector FPGAs and Zynq devices.

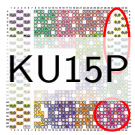
FPGA choices

Sector FPGA

Package	-1 A1156					
Part	KU035	KU040	KU060	KU095	KU11P	KU15P
Logic Cells (k)	444	530	726	1176	653	1143
Distributed RAM (Mb)	5.9	7.0	9.2	4.8	9.1	9.8
BRAM (Mb)	19.0	21.1	38.0	59.1	21.1	34.6
UltramRAM (Mb)	–	–	–	–	22.5	36.0
[Total RAM (MB)]	[19.0]	[21.1]	[38.0]	[59.1]	[43.6]	[70.6]
I/O (HR/HP)	104/416	104/416	104/416	52/468	48/416	48/468
MGT (GTH[a]/GTY[a])	16/0	20/0	28/0	20/8	20/8	20/8
Retailer price ($)	1250	1655	2536	4375	2734	3751

[a] 16.3 Gbps (package restriction)





- Choice of packaging that allows wide range of choices while keeping good ratio between cost and resources. Preference for KU060. Development kit: KCU105.

Management Unit

	Zynq 7000		
Package	-2CLG485		-2SBG485
Part	7Z012S	7Z015	7Z030
PS I/O	128	128	128
PL I/O (HR/HP)	150/0	150/0	50/100
Logic Cells (k)	55	74	125
BRAM (Mb)	2.5	3.3	9.3
MGT (GTP[a]/GTX[b])	4/0	4/0	0/4
Retailer price ($)	125	155	320

[a] 6.25Gbps [b] 6.6Gbps

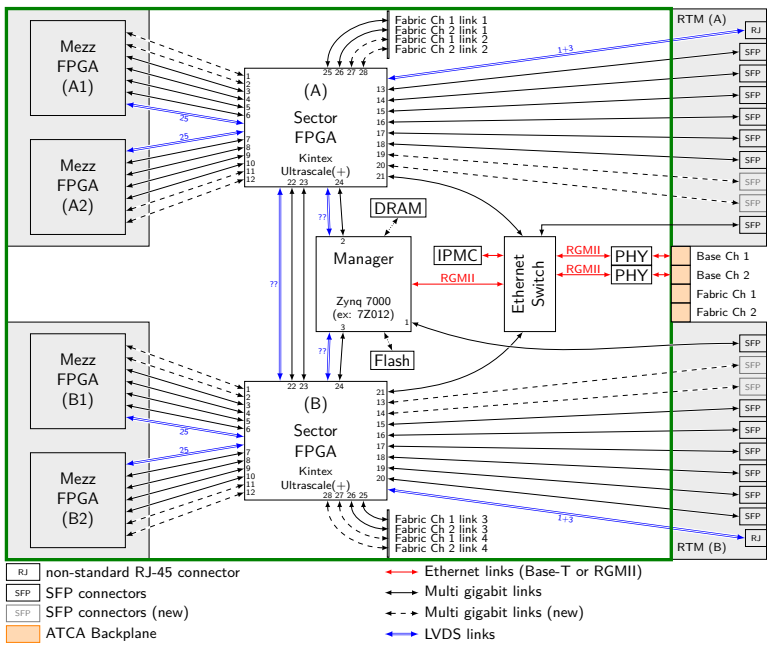
- Inexpensive Zynq 7000 with serializers. Development kit: PicoZed (7Z015/30).

Serializers

- All the eight serializers available form each mezzanine shall be routed directly to the related Sector FPGA (maximum bandwidth).
- All SFP connectors in RTM shall be routed to serializers in the Sector FPGAs (2×6) and Zynq Fabric (1), except a link to on-board Ethernet Switch.
- Extra links for each sector are reserved if a bigger Sector FPGA is affordable and might be routed to mezzanine (2), RTM (2), and Fabric Interface on the backplane. Conditioned by the detailed design.

Serializers foreseen:

- $4 + 2$ between Sector FPGA and mezzanine FPGA ($8 + 4$ in total for each Sector FPGA)
- $6 + 2$ between Sector FPGA and RTM
- $2 + 2$ between Sector FPGA and Backplane Fabric Interface
- 1 between Sector FPGA and Zynq (two in total for a Sector FPGA)
- 1 between Zynq Fabric and RTM

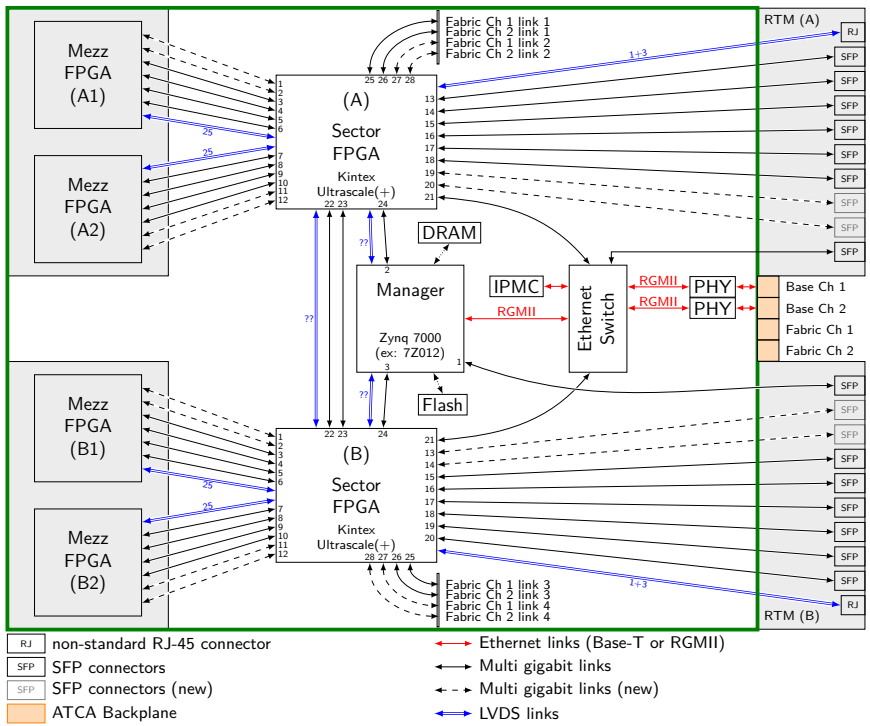


Ethernet connections

- A on-board gigabit Ethernet switch shall distribute the link received from the ATCA Base Interface on the backplane.
- For the case where no ATCA hub is available, an SFP connector on the RTM shall be connected to the switch.

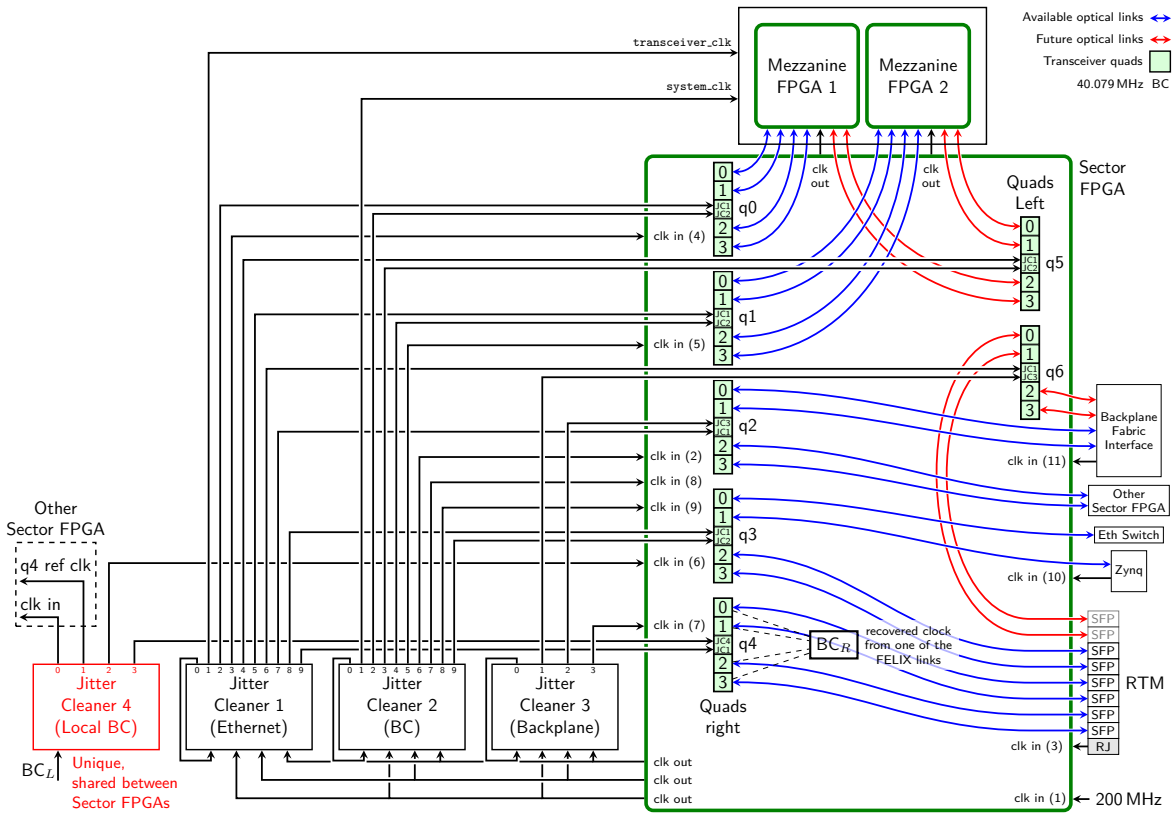
At least, 6 links are required:

- Base channel 1 – 10/100/1000Base-T
- Base channel 2 – 10/100/1000Base-T
- IPMC – 10/100Base-T
- Zynq – RGMII
- Sector FPGA 1 – SGMII or Base-X
- Sector FPGA 2 – SGMII or Base-X
- RTM link – SGMII or Base-X

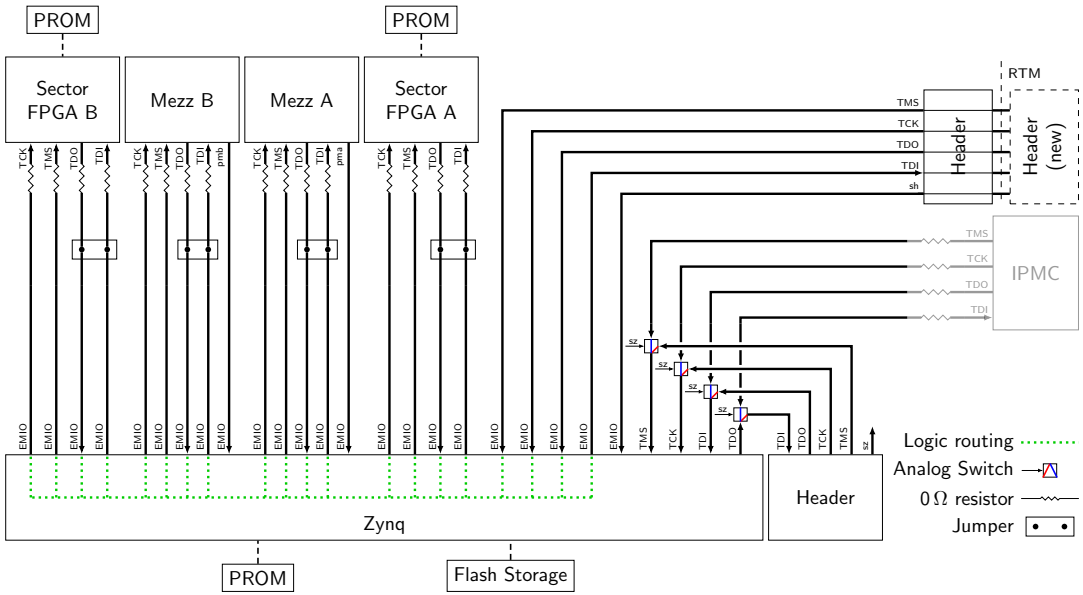


Clocking

- Distribute clocks derived from 3 clock sources at same time (3 clock regions: BC, Ethernet and Fabric Interface).
- Several clock sources: 200 MHz, local BC, recovered BC, Zynq provided, or external RTM clocks. Distributed by Sector FPGA.
- Quad reference clocks related to functionality.
- Local BC clock shared by both Sector FPGAs (needed for recovering BC clock).



FPGA Programming and in-system debugging



Overview

- Flexible JTAG scheme based on Zynq Fabric rerouting during regular operation. JTAG masters: local connector, remote (XVC service) or Zynq itself.
- Recovery targeted to Zynq only through IPMC (if available) or local header.
- A PROM for each reconfigurable unit.

Specifics

- On-board JTAG header has priority over IPMC XVC.
- Bypass jumpers to skip a reconfigurable unit.
- Zero-ohm resistors to eliminate components from the JTAG chain.

Other information

ATCA platform monitoring: shared between IPMC and Zynq SoC.

- 2 separated I^2C buses, independent masters.
- IPMC shall monitor passive and critical components.
- Zynq shall monitor configurable components, providing important sensing information via bridge (I^2C slave) to the IPMC.
- CERN (LAPP) IPMC form-factor is required.

Recovery path: based on IPMC, it should be provided at least by golden-version firmware through direct address management (user-defined functions). XVC service is strongly suggested.

Board and component ID: non-volatile memory independent from boot process. Extra pin connected to low level in one Sector FPGA and to high level in the other.

Conclusion

- Specifications for carrier card v2 are complete although high-level.
- SAMWAY is an experienced company with ATCA designs in charge of the detailed design.
- Specification document including details has been delivered to SAMWAY.
- Design has already started.

Backup