NSW Trigger Processor Thermal Test Results

Thiago Costa de Paiva

For the New Small Wheel Trigger Processor Group:
Harvard, Bucharest, Technion, Weizmann, U. Mass. Amherst

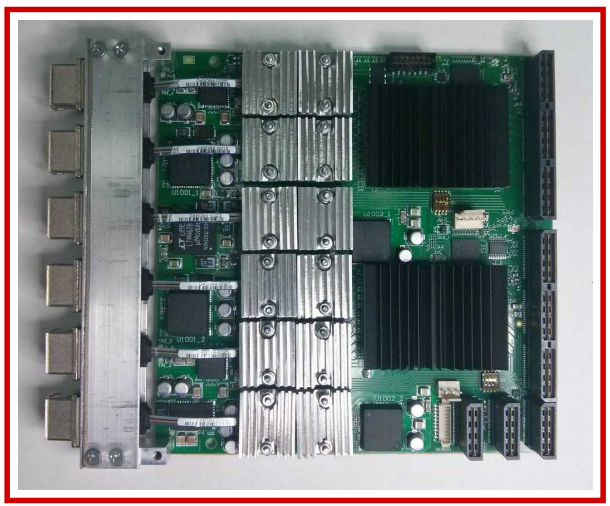
University of Massachusetts Amherst

June 26, 2018

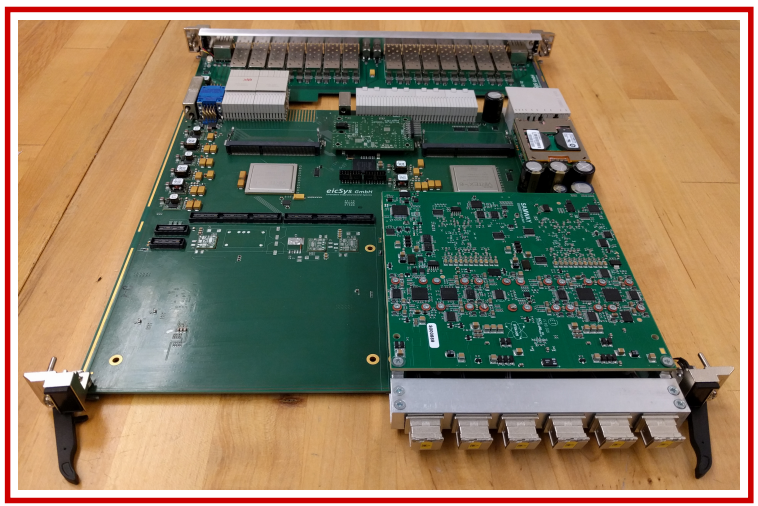
Goals

Main goal is to test the thermal properties of the NSW trigger processor hardware with full power load in a full crate under realistic conditions. Specifically:

- Build a temperature profile of the NSW Trigger Processor hardware $\rightarrow$ main sources of heat are trigger processor FPGAs and optical transcievers in the mezzanine card
- Measure the response of the hardware to an increase in temperature and verify performance up until expected power consumption (e.g. check if data is being corrupted, etc)



Horx Mezzanine



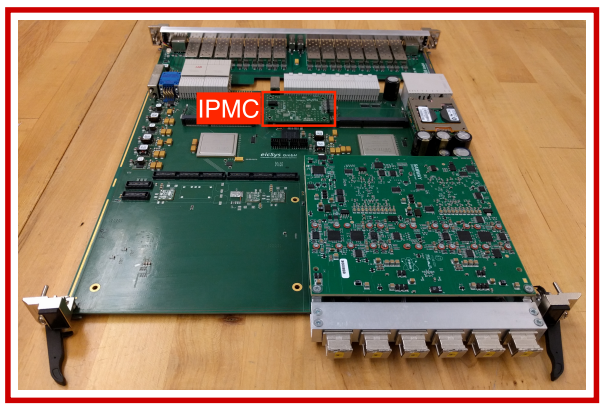
EATCA-100 carrier board

Terminology aside

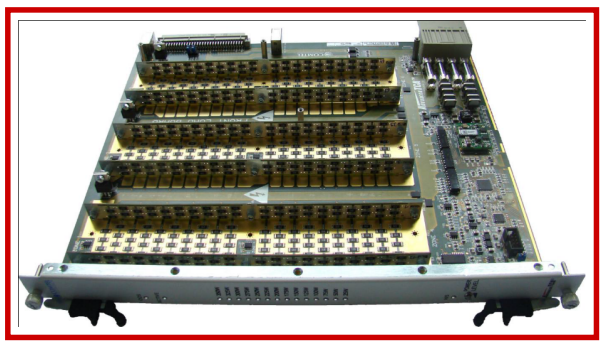
As a reminder, the ATCA standard offers a wide range of hardware management features to monitor (temperatures, voltages, current, etc.) and control (fan speed, power management, etc.) for the electronics. This is achieved through controller modules interconnected via an Intelligent Platform Management Interface (IPMI) bus:

- Module Management Controller (MMC) for Mezzanine Cards
- Intelligent Platform Management Controller (IPMC) for ATCA blades
- Shelf Manager for ATCA shelves
- Thermal Load Boards (manual setup, Shelf Manager monitored)

6-slot COMTEL ATCA Shelf



EATCA-100 carrier board



Thermal Load Board

Test Setup

Assembled a setup to perform thermal tests of the prototype boards.

Profiles studied

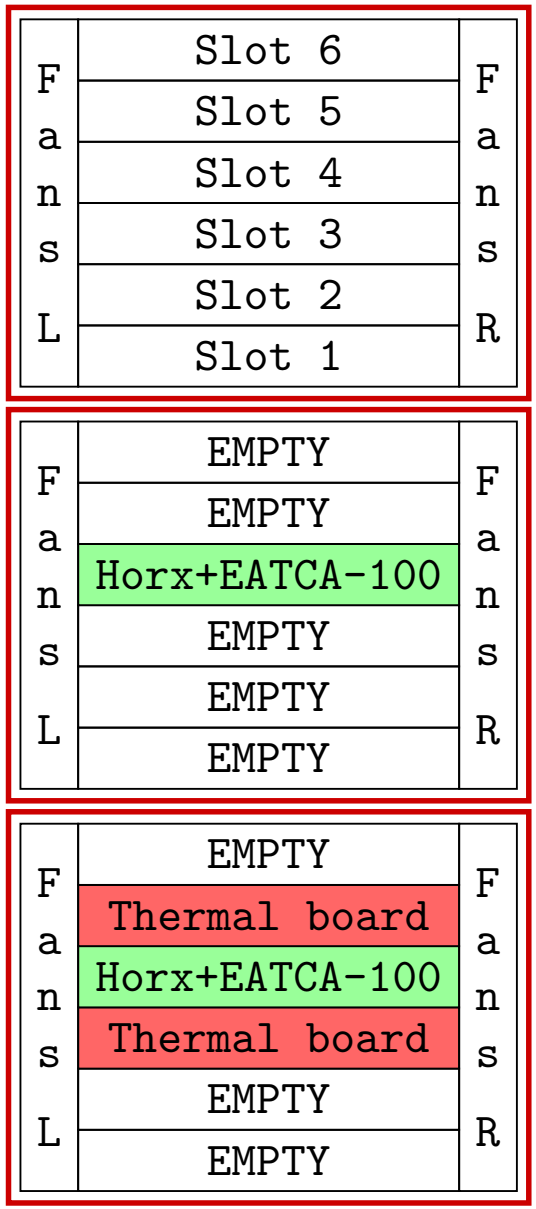
- Single board performance → verify performance of sensors
- Use thermal boards to emulate more realistic crate environment

FPGA firmware developed to

- exercise high speed communication
- use enough FPGA resources

Framework developed to access

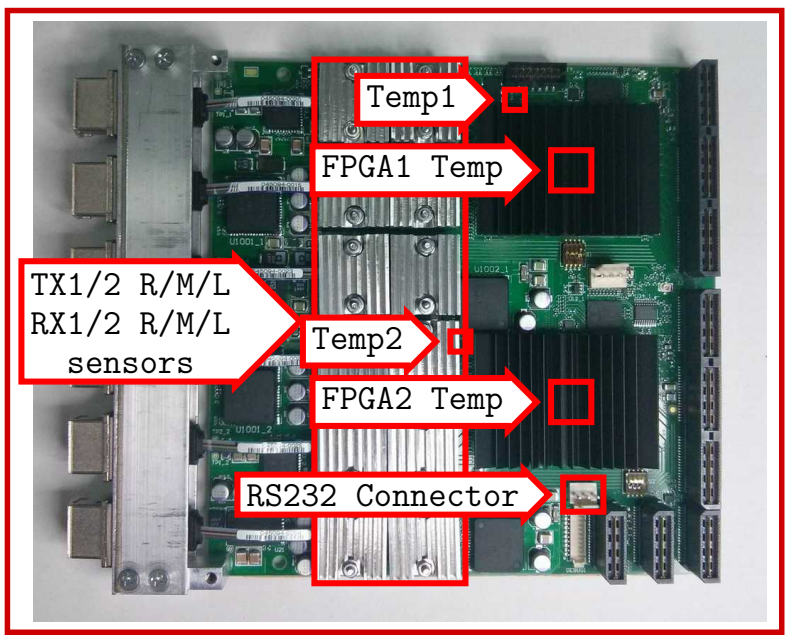
- ATCA shelf information through IPMI.
- Mezzanine sensors through MMC
- Discrete sensors via DMM (if needed)



Sensors measured in the Mezzanine card

No access to the temperature sensors on the Mezzanine card through IPMC

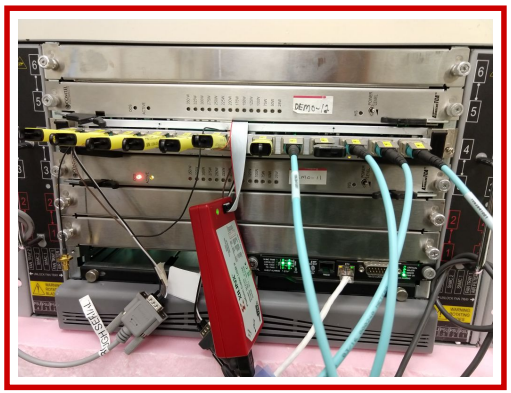
- Management firmware exposes the FPGA and optical transceivers temperatures over I2C to the MMC
- Direct access to Horx MMC over serial (RS232)

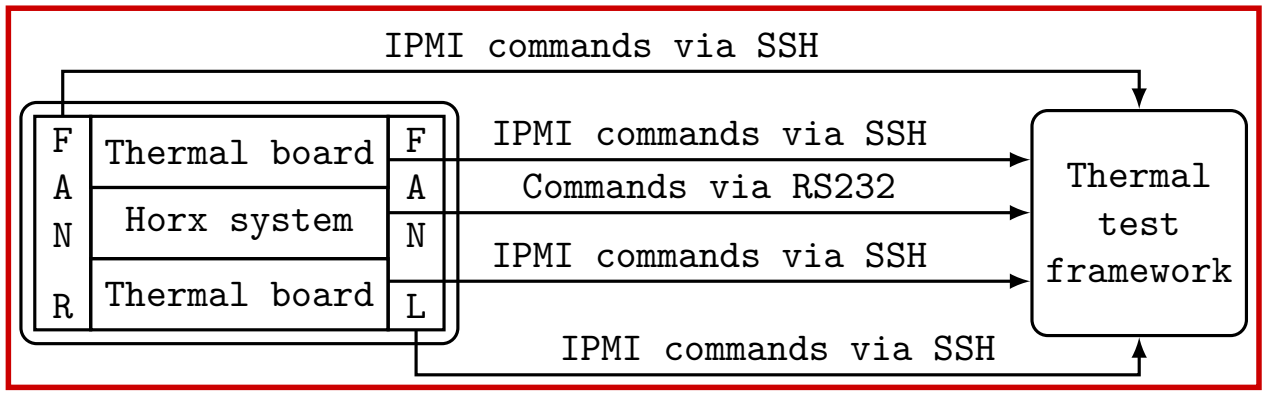



```
%>sensor
---------------------Sensor List-------------------------------
--no--Name--------------Value---Unit---State-------------------
*   1  Hot Swap Handle   Closed
*   2  1.8V_MGT1         1.81     V       Ok
*   3  1.8V_MGT2         1.81     V       Ok
*   4  1.0V_MGT1         1.01     V       Ok
*   5  1.0V_MGT2         1.00     V       Ok
*   6  1.8V_1            1.81     V       Ok
*   7  1.8V_2            1.80     V       Ok
*   8  3.3V_VCC          3.35     V       Ok
*   9  12V_IN            13.91    V       Ok
*  10  Temp1             42.00    deg C   Ok
*  11  Temp2             49.00    deg C   Ok
*  32  Pwr_Good_2.5V     1 Asserted
*  33  Pwr_Good_1.2V_1   1 Asserted
*  34  Pwr_Good_1.2V_2   1 Asserted
*  35  Pwr_Good_1.0V_1   1 Asserted
*  36  Pwr_Good_1.2V_2   1 Asserted
* 101  Fpga1 Temp        58.23    deg C   Ok
* 109  TX1 R             44.50    deg C   Ok
* 118  TX1 M             47.50    deg C   Ok
* 119  TX1 L             29.50    deg C   Ok
* 120  RX1 R             33.00    deg C   Ok
* 121  RX1 M             0.00     deg C   Ok
* 144  RX1 L             52.50    deg C   Ok
* 150  Fpga2 Temp        66.10    deg C   Ok
* 151  TX2 R             58.00    deg C   Ok
* 152  TX2 M             59.50    deg C   Ok
* 153  TX2 L             41.00    deg C   Ok
* 154  RX2 R             41.50    deg C   Ok
* 155  RX2 M             39.00    deg C   Ok
```

Output from MMC when `sensor` command is issued

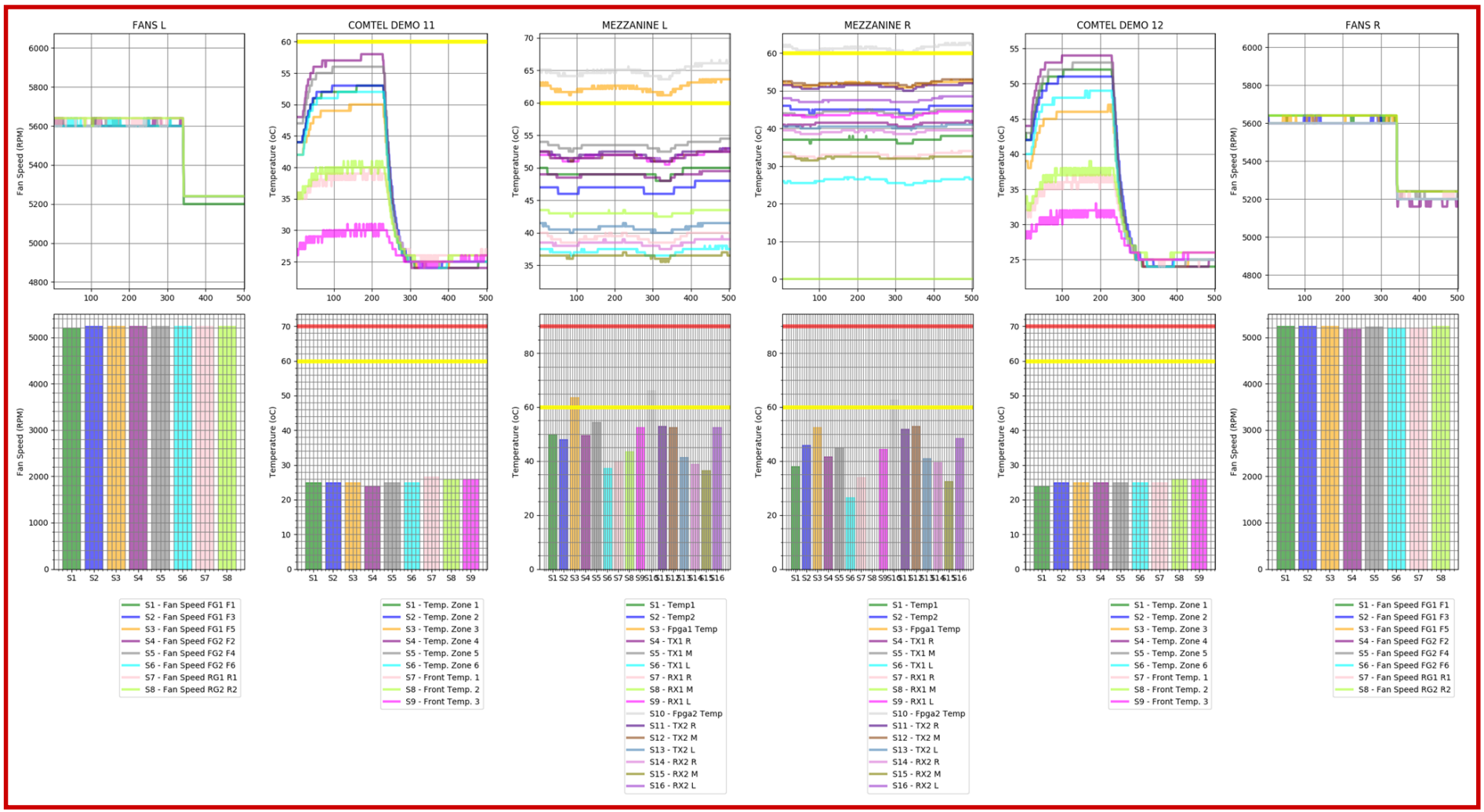
Test Assembly





- Optical Loop-back cables
- Thermal test framework GUI
- Readout temperature and crate information in setup with surrounding thermal boards
  - Data acquisition of ATCA sensors (temperature, fans, etc) through Shelf Manager
  - Data acquisition of Mezzanine sensors over serial link (RS232)
  - Display and log of sensors data using Python-based framework
  - Power level manually set at Thermal boards

Thermal Test Data in 6-slot Crate



- Right-to-left airflow (80% and 60%)
- Approx 4 s per cycle (sampling of all targets, approx 33-min window)

Thermal Test Data in 2-slot Crate

- Right-to-left airflow (100 %)
- Approx 5 s per cycle (sampling of all targets, approx 80-min window)
- Environment temperature decreasing

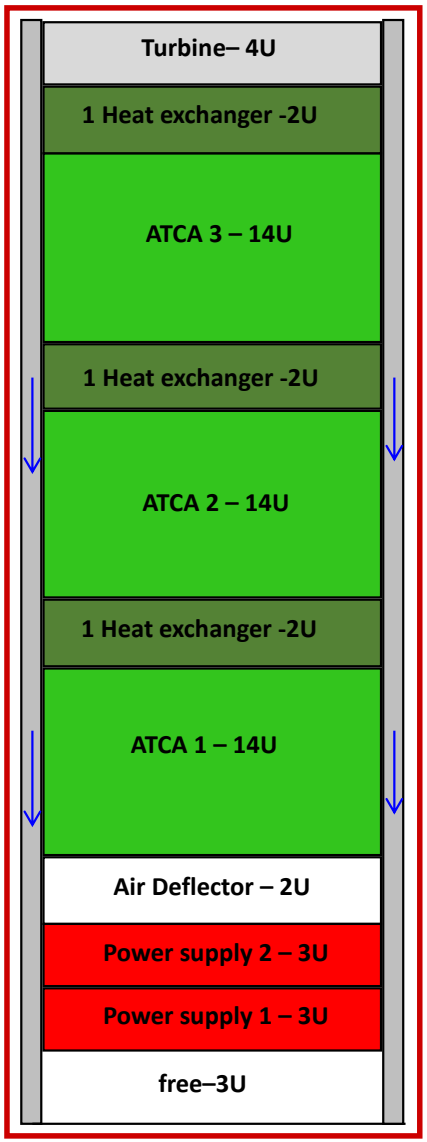
Thermal Test Preliminary Results

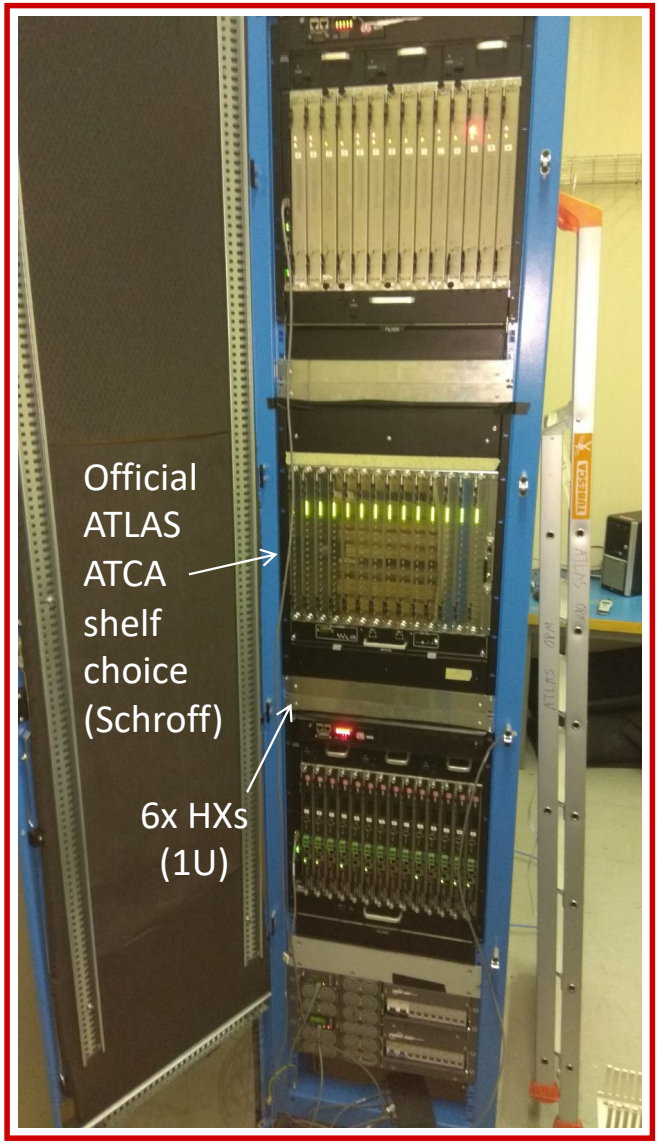
- 144 optical links (IBERT) running at 4.8 GBps
- Successfully readout mezzanine and crate information
  - Fan speeds
  - Thermal Load board temperature sensors
  - Mezzanine temperature sensors
- Data logging for post processing
- Firmware power consumption: approx 15W (18W estimated for MM algorithm)
- Temperature always below 70 °C
  - Horizontal airflow
  - Room Temperature environment
- Flexible setup (easily adjustable for different crates)
  - Tested with 3 unrelated crates

Plans

Tests at CERN with ATLAS standard resources and full setup in next few weeks (currently scheduled for July 4-6)

- ATLAS standard ATCA crate with 14 slots
- Vertical cooling and with prototype rack
- Adjustable airflow in thermal boards





Conclusion

- Non-ideal environments with horizontal airflow, Room Temperature environment, improper separation between slots
- Trigger processor hardware shows reasonable thermal performance in first tests
  - Power consumption of about 15 W per Mezzanine FPGA
  - Maximum temperature observed, about 67 °C (in FPGAs, optical transceiver are cooler)
- Plan to perform tests in ATLAS standard setup in next weeks to confirm the preliminary results obtained so far, in advance of production.

Backup

Overview of Thermal Test SW Framework

Target Class is a superclass

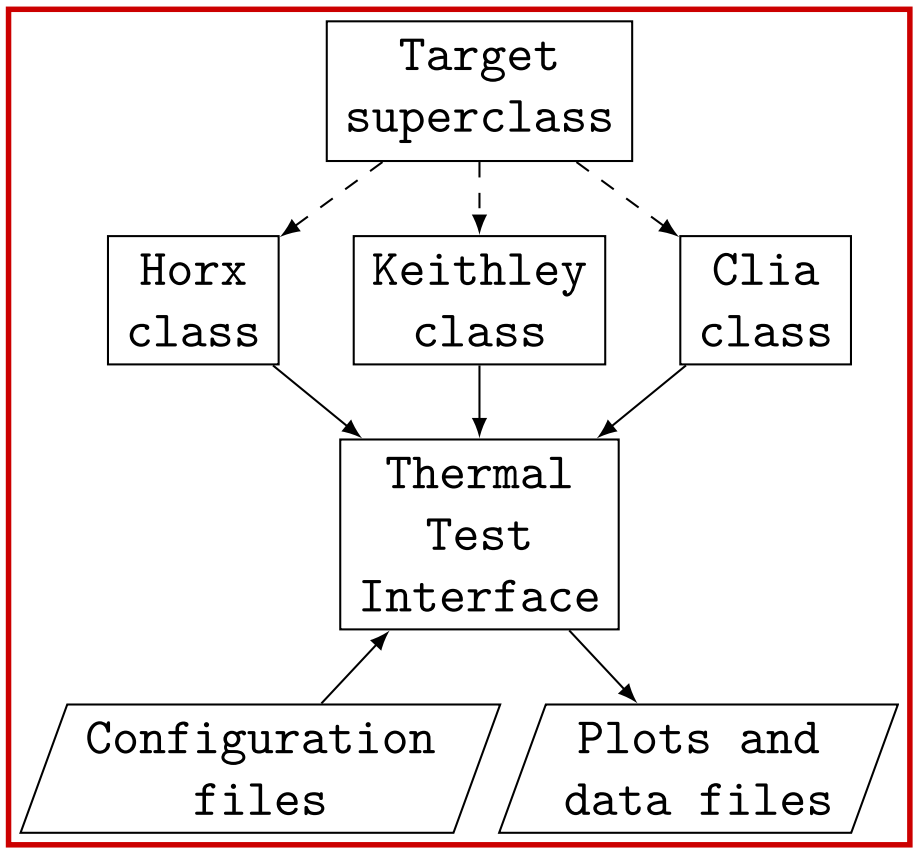
- Horx Class: NSW TP controller
- Clia Class: through shelf manager
- Keithley: using Keithley DMM

Configuration files

- flexibility to adjust to different ATCA shelves and carrier boards.
- general setup file for targets selection
- description file for each target
  - can be shared between targets

Output

- Plots for real time visualization
- data files for later processing



Code written in Python 2.7

More information about available Hardware

- Hardware resources
  - UMass has 2 COMTEL load boards
    - 50W to 350W
    - Power dissipation controlled in front panel
    - Temperature sensors reading through Shelf Manager.
  - UMass has a 6-slot ATCA shelf
    - horizontal airflow
- Mezzanine sensors
  - Firmware for internal temperature reading available for Virtex 7
  - Firmware to read the temperature of the optical transceivers is available.
  - MMC is also able to read temperature of discrete sensors on the board.
  - Virtex 7 workload firmware module
    - To exercise the resources of the FPGA available
    - Based on IBERT (from Xilinx) loopback communication
- GUI (Python)
  - Display and log of sensors data
  - Data acquisition of ATCA sensors (temperature, fans, etc) through Shelf Manager
  - Mezzanine sensors data acquisition over serial (RS232)

GUI explanation