A telescope based on MALTA CMOS sensors

Abhishek Sharma (University of Oxford (GB))
Carlos Solans Sanchez (CERN)
Enrico Junior Schioppa (CERN)
Ignacio Asensi Tortajada (Univ. of Valencia and CSIC (ES))
Patrick Moriishi Freeman (University of Birmingham (GB))
Valerio Dao (CERN)
ITK for ATLAS Phase II

HL-LHC Pixel detector upgrade (2024-2026): 5 pixel layers, inclined layout

Targeting the outermost Layer 4
- 2016 modules
  - ~3 m² of silicon
  - 45% of ITk outer barrel
  - 30% of thick planar modules
- For 3000 fb-1 integrated luminosity:
  - 1.5 $10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ (with safety factor)
  - 80 Mrad TID

Requirements for Pixel Layer 4:
- Radiation tolerance
  (without safety factors):
  - NIEL $1e15 \text{n}_{\text{eq}}/\text{cm}^2$
  - TID 60 Mrad
- Hit rate 100–200MHz/cm²
- Timing resolution 25 ns

<table>
<thead>
<tr>
<th>Pixel Hit Rate</th>
<th>Layer</th>
<th>Mhit/mm²/s</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>27.2</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>8.4</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>1.72</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>1.16</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>0.84</td>
</tr>
</tbody>
</table>
The TowerJazz 180 nm CMOS technology

- Small collection electrode (few $\mu$m$^2$)
- Small input capacitance
- High S/N for a depletion depth of $\sim 20$ $\mu$m
- To ensure full lateral depletion, **uniform n-implant** in the epi layer (modified process)
TowerJazz MALTA chip

- Monolithic Active Pixel made in CMOS technology by Towerjazz

- 512x512 pixels
- **8 sectors** with different pixel flavors
- Fully clock-less matrix architecture
  - low power
- Charge information from timewalk

- **Pixel size** 36.4 x 36.4 $\mu$m²
- 2-3 um collection electrode
  - small input capacitance
- 3.4 – 4 um separation between electrode and electronics
  - low cross talk
- 1 $\mu$W/pixel analog power (75 mW/cm²)
- 10 mW/cm² digital power @ layer4
MALTA architecture

- Groups of 2x8 pixels with pattern assignment to reduce data size from clusters
- Front-end discriminator output is processed by a **double-column** digital logic
- Pulse width adjustable between 0.5 ns and 2 ns
- Data are transmitted **asynchronously** over **high speed bus** to the end of column
- At the periphery, an **arbitration and merging** logic resolves timing conflicts of simultaneous signals
- Timing information is kept by dedicated bits
- Each hit is represented by a 40 bit word
- Output signals transmitted by 5Gbps **LVDS drivers**
First production of MALTA

January 2018

Very first image of a Fe$^{55}$ source
Second version to improve power distribution

- MLVLC = Metal Last Vias Last Change
- Improve connections to digital power in the slow control block
- Improve PWELL connections in the matrix
- Modified top metal and top via
Known issues

- Some DACs must be operated by external trimmers
- Some pixels/columns cannot be masked
  - Cannot go to too low threshold (~250 e unirr., ~350 e irrad.)

In case of high activity **merger logic** must be forced off due to the high noise activity

- All hit signals are pushing on the same output line
- Simultaneous hits are OR-ed
- Hit information (e.g. address) is lost

Half of the pixel matrix is masked manually using the external trimmers
Measurements from analog pixels

- MALTA has 8 special pixels:
  - No digital circuitry
  - Direct access to the analog output
  - Meeting 25ns BC ATLAS requirements

Out of time hits
5.3%

In-time threshold
130 mV = 300 e⁻
Threshold gain

- Measurements of threshold gain from Fe-55 spectra from the analog pixels
- Calibrate the energy in function of the substrate voltage
- Threshold gain estimated from the distance between the K- alpha and K-beta peaks

<table>
<thead>
<tr>
<th>SUB (V)</th>
<th>gain±0.002 (mV/e)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6</td>
<td>0.1464</td>
</tr>
<tr>
<td>-12</td>
<td>0.1480</td>
</tr>
<tr>
<td>-15</td>
<td>0.1371</td>
</tr>
<tr>
<td>-18</td>
<td>0.1364</td>
</tr>
</tbody>
</table>
Threshold dispersion

- Threshold dispersion $\sim x2$ larger than design
- Conclusion $\rightarrow$ adjustment bits in next submissions
Test beam campaigns

- March and April → ELSA, 3.2 GeV/c electrons
- From April to October → CERN SPS, 180 GeV/c pions
- CERN FEI4 telescope, resolution ~8 um
- MIMOSA telescope resolution <2 um
- MALTA based telescope
- Up to 2 DUTs can be tested simultaneously
- Irradiated samples are kept cold by a Si-oil system
- Results shown here are on SPS MIMOSA data
- We tested first and second versions of the chip
Cluster size

Unirradiated
(W6R6, S4)

Decreasing threshold, from ~600 e - to ~250(unirr)/350(irr) e -

Irradiated
5x10^{14} \, n_{eq} / \text{cm}^2
(W6R21, S4)

 Couldn’t reach lower threshold
In-pixel efficiency

Unirradiated (W6R6, S4)

Irradiated 5x10^14 neq/cm^2 (W6R21, S4)

Decreasing threshold, from ~600 e⁻ to ~250(unirr)/350(irr) e⁻

Reconstruction done with **Proteus**: https://gitlab.cern.ch/unige-fei4tel/proteus/

Mini MALTA

- Smaller matrix version that changes the p-well extension to address the efficiency loss on corners
- First production arrived on January 2019
  - First samples just bonded
- Will soon be tested for:
  - Power requirements
  - Minimum stable threshold
  - In-time threshold & overdrive
  - Threshold dispersion
  - Equivalent noise charge
  - Fraction of noisy pixels
The MALTA Telescope
MALTA Telescope

- Telescope built for carry-on test beam applications during LS2
- Built with 6 MALTA planes
- 6 FPGAs with ethernet IPBus readout
- EUDAQ compatible

- Tested in SPS end of October 2018

Beam Location

22.8 cm 45.2 cm 22.8 cm
0 cm 6.5 cm 15 cm 39 cm DUT 65 cm 79 cm 85 cm
### MALTA telescope setup

- Power distribution remotely managed from control room
- Trigger provided by scintillator using NIM logic
- Evolved into directly triggering on signals from the telescope plane (up to three planes coincidence)

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**Remote power supply control**

<table>
<thead>
<tr>
<th></th>
<th>IN1</th>
<th>IN2</th>
<th>Coincidence</th>
<th>Veto</th>
<th>Output</th>
</tr>
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<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**Diagram:**

- Scintillator
- MALTA planes
- Beam
- DUT
- Remote power supply control panel
MALTA telescope hardware

- CERN Network
- Switch
- PS07
  - IP: pcatlidps07
- USB hub (Octopus)
- Power supplies
- Router
  - IP WAN: ep-ade-gw-02
  - IP LAN: 192.168.0.2
- Scope
  - IP: 192.168.0.106
- Switch
- MALTA FPGA
  - IP: 192.168.0.1
- MALTA FPGA
  - IP: 192.168.0.10
- MALTA FPGA
  - IP: 192.168.0.11
- MALTA FPGA
  - IP: 192.168.0.12
- MALTA FPGA
  - IP: 192.168.0.13
- MALTA FPGA
  - IP: 192.168.0.14
- MALTA carrier
- MALTA carrier
- MALTA carrier
- MALTA carrier
- MALTA carrier
Future plans

- TLU combines hit information from MALTA and scintillator
- TLU provides common clock to MALTA
- TLU issues L1A to MALTA planes
- MALTA planes issue busy signal to TLU if deadtime
- MALTA planes write data to disk
Telescope read-out

Hitmaps
Timing

Data taking using custom Malta SW with C++, Python, IPBus and TDAQ
Telescope tracking

- 6 hits on track
- Pions resolution 4μm
- We have an issue with the multiple scattering of electrons and we may need to improve tracking.

Data of resolution

![Resolution Pions](image1)

![Residuals Pions](image2)

Simulations

![Residuals Electrons](image3)
Residual in various configurations

Residual = Difference between track intercept and cluster location
E(e^-)=3GeV

Moving planes closer together improves residuals

<table>
<thead>
<tr>
<th># of plane</th>
<th>Distance to plane 1 [cm]</th>
<th>Distance to plane 1 [cm]</th>
<th>Distance to plane 1 [cm]</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>6.5</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>15</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>DUT</td>
<td>39</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>65</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>79</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>6</td>
<td>85</td>
<td>12</td>
<td></td>
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</tbody>
</table>

Residual = 87um
Moving planes closer together improves residuals

https://cern.ch/allpix-squared
Allpix²: A Modular Simulation Framework for Silicon Detectors
2019 Plans

Test beam campaigns scheduled for 2019

- DESY and ELSA
- MALTA telescope will be used in ELSA (Bonn)
- Electron beams will have lower resolution

ELSA beam line

Bonn
Next steps

- Telescope **development continues** after test beam campaigns
- Using different sources
- Simulation in AllPix\(^2\) shows it **can be improved**

Telescope setup in CERN lab
Conclusions

- MALTA is a full demonstrator monolithic CMOS sensor produced in 180nm TowerJazz technology
- Uses a novel asynchronous readout with no clock distribution over the matrix to minimize power consumption
- Small electrode for low capacitance and low analog power consumption.
- First production came back in Jan 2018, second production in Jun 2018
- Merging logic is forced off leading to some hits being lost
- Analog tests show the expected in-time efficiency and low noise

- Most issues we see in the test beam results are explained by the degraded detection efficiency, especially in the pixel corners.
- All these issues will be addressed in the next submission(s)
- Successful operation of the MALTA telescope that will be used on 2019 campaigns
Thank you for your attention
Back up
Telescope alignment

Inter-plane correlations in x

Alignment using Proteus
Residuals DESY vs. SPS in AllPix$^2$

- Residual = Difference between track intercept & cluster location
- Much worse for e$^-$
- 87μm for e$^-$, 11μm for pions
- Mean 0 indicates good alignment
- Poor track fits -> large residuals
- Again, multiple scattering
- For pions, close to 36μm/sqrt(12)
Effect of p-well extension

Difference between medium p-well and maximum p-well becomes visible on irradiated chips at high threshold

Sector 3
Med deep p-well

Sector 4
Max deep p-well
Charge sensitive front-end

- Operating principle derived from the ALPIDE front-end
- < 5 fF sensor capacitance -> excursion at input of tens of mV
  Voltage amplifier can take the place of a standard CSA
  Optimization for minimal power consumption and fast timing response
- Power 0.9 uW, threshold ~200e-, ENC ~12 e-, gain 0.4mV/e-
- M1 acts as a source follower.
- M2 is a cascade transistor to increase the gain on the output node and eliminate the Miller effect for the input node.
- The analog output node is stabilised at low frequencies by active feedback on the transistor M3
- Efficient current usage for the input (the same branch current powers the source follower and the amplification stage)
- MALTA: optional clipping of the analog pulse
Readout: asynchronous oversampling

- Implemented on a Xilinx Virtex707 evaluation board
- Signal speed is 1 GHz
- Typical strategy is to sample with transceivers: recover clock from data and sample data
- But evaluation board does not have enough (40) transceivers to the FMC
- Alternative is to oversample the signal with 2 ISERDES shifted 45° and 2 clock phases shifted 90°
Simulation for DESY beam, 2019

- $\chi^2$ much worse (\(~23\) vs. \(~1.0\) 
  - Likely due to multiple scattering
- Clusters about the same as for pions: (1.08 vs 1.09)
Interpix efficiency loss

Substrate bias sweep on first production unirradiated (W4R7)

Sub -12

Sub -15

Sub -18

Sub -20
Pixel center artifact

Threshold sweep on irradiated 1x10^15 n eq/cm²

“High” threshold (~450 e)

“Low” threshold (~350 e)

- ARTIFACT: efficiency in the pixel center decreases due to the masking and merging issues
- Consistently observed in all samples
Telescope resolution

- Test beam results from 6 planes + 1 DUT plane simulated in Proteus
  - Proteus track reconstruction configuration is identical for real and simulation data
  - Rotational orientation in Z taken directly from Proteus reconstruction on real data
- Simulation of 120GeV Pi+ for SPS test beams from 2018
  - Mean Chi2 observed: 0.9, simulated 1.1
- Simulation of 3GeV e- at DESY for test beams in 2019

<table>
<thead>
<tr>
<th>Data Set</th>
<th>Resolution</th>
<th>Residuals $\sigma$</th>
<th>Mean cluster Size</th>
<th>Mean reduced $\chi^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>120 GeV Pi+, SPS TB</td>
<td>4.2 µm</td>
<td>-</td>
<td>1.12</td>
<td>0.90</td>
</tr>
<tr>
<td>120 GeV Pi+, simulation</td>
<td>4.3 µm</td>
<td>11 µm</td>
<td>1.09</td>
<td>1.10</td>
</tr>
<tr>
<td>3 GeV e-, simulation</td>
<td>4.3 µm</td>
<td>151 µm</td>
<td>1.08</td>
<td>160</td>
</tr>
</tbody>
</table>
First tests performed on unirradiated and neutron irradiated chips ($5 \times 10^{14}$ n$_{eq}$/cm$^2$ and $1 \times 10^{15}$ n$_{eq}$/cm$^2$)

Analog tests show the expected in-time efficiency and low noise

Digital tests show a higher threshold dispersion than expected → might add adjustment bits in the next submissions

Next submissions will address the radiation hardness and will fix the slow control issues

Successful operation of the MALTA telescope

Report at ITK week September 2018
- https://indico.cern.ch/event/726191/contributions/3149674

Report at AUW November 2018
- https://indico.cern.ch/event/771784/contributions/3211969