Overview of the modular DAQ hardware designed for beam tests of the HGCAL prototype

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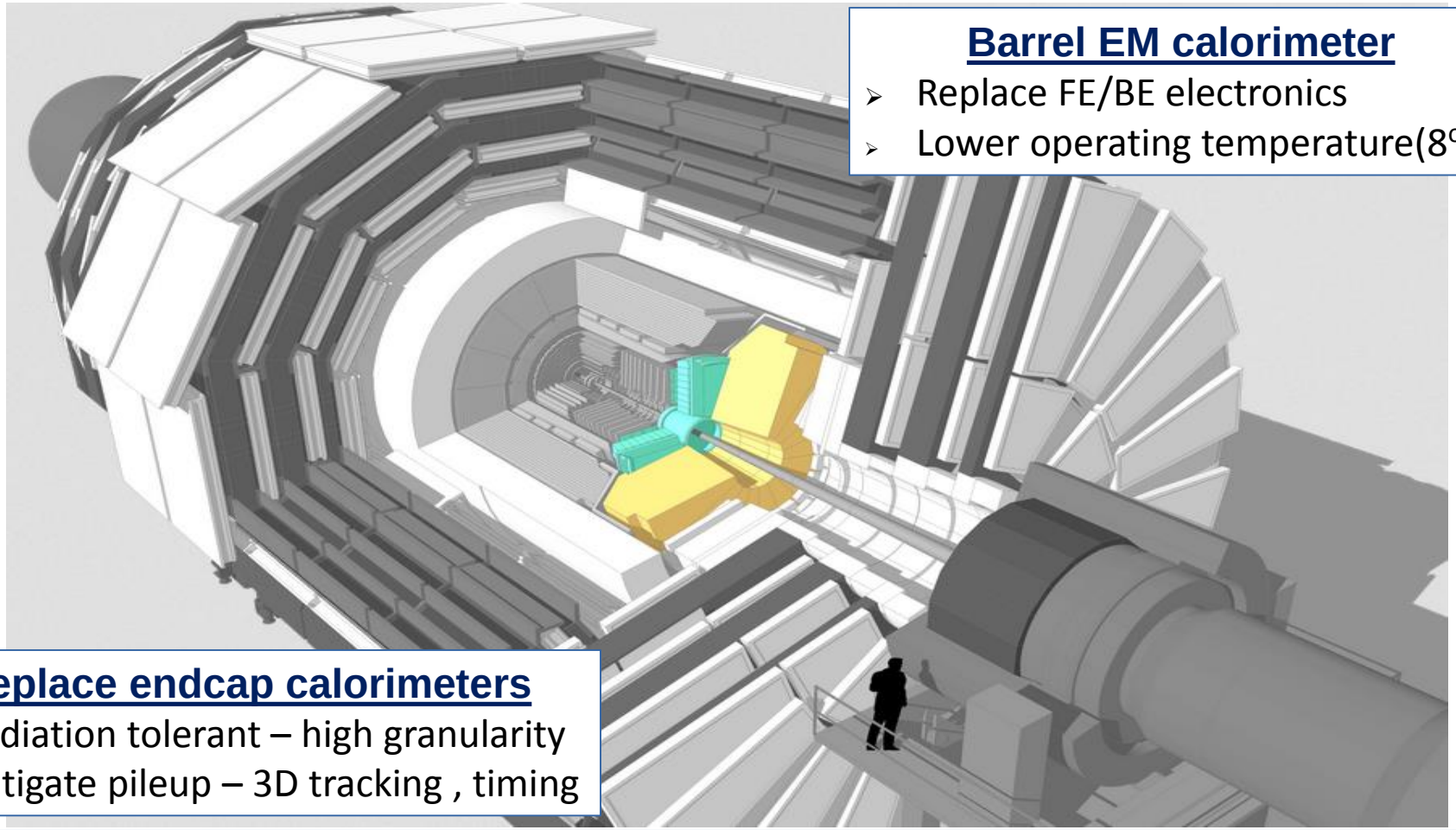
Upgrades to CMS calorimeters for HL-LHC



Barrel EM calorimeter

- Replace FE/BE electronics
- Lower operating temperature(8°C)

Replace endcap calorimeters

- Radiation tolerant – high granularity
- Mitigate pileup – 3D tracking , timing

The endcap calorimeters need replacement as they will not support the doses and fluences at the HL-LHC.

The CMS upgrade endcap calorimeter: Design

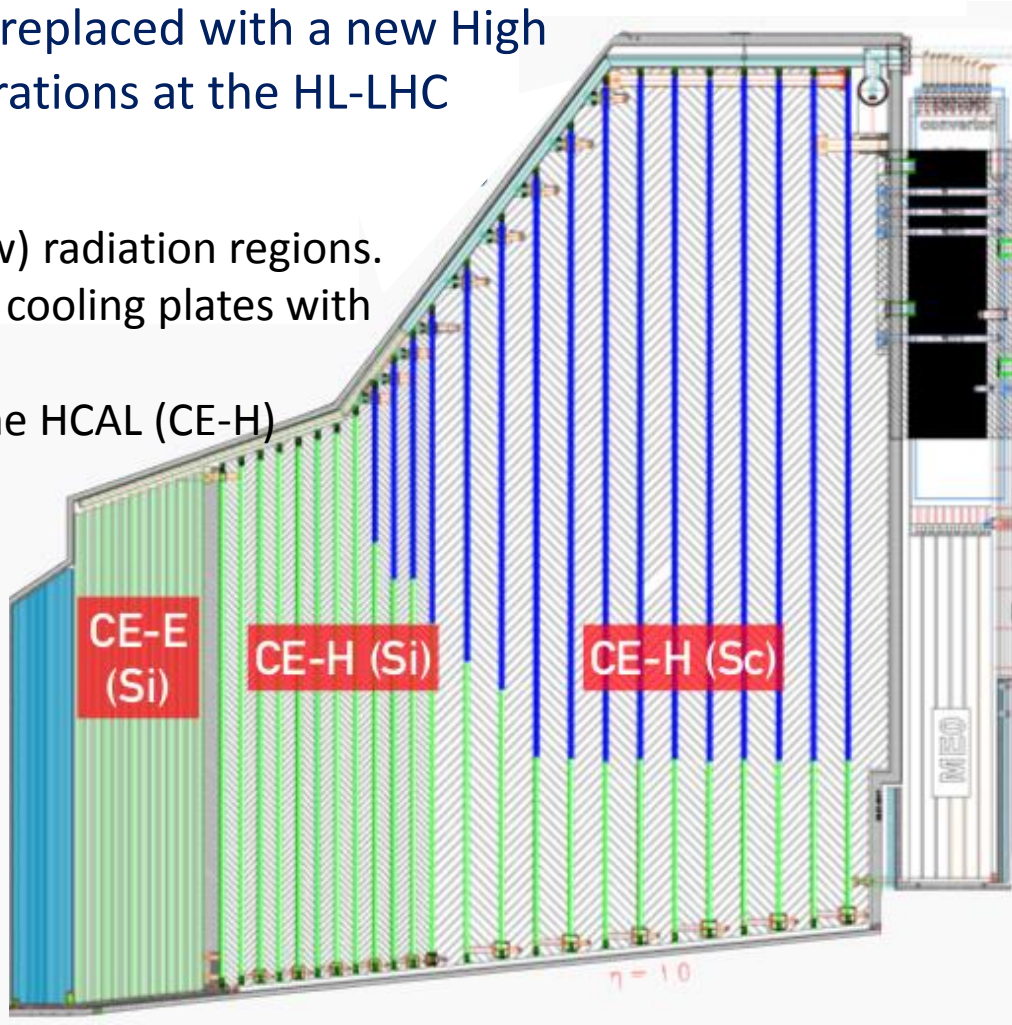
The current endcap calorimeters will be replaced with a new High Granularity Calorimeter(HGCAL) for operations at the HL-LHC

Active Elements:

- Silicon(Scintillator) detectors in the high(low) radiation regions.
- "Cassettes": multiple modules mounted on cooling plates with electronics and absorbers.
- 28 layers in the ECAL (CE-E) + 24 layers in the HCAL (CE-H) compartments.

Key Parameters:

Endcap coverage: $1.5 < \|\eta\| < 3.0$		
Total	Silicon sensors	Scintillator
Area	600 m^2	500 m^2
Number of modules	27 000	4 000
Cell size	0.5 — 1 cm^2	4 — 30 cm^2
N of channels	6 000 000	400 000
Power	Total at end of HL-LHC: ~180 kW @ -30°C	



- See F. Simon's slides for details.

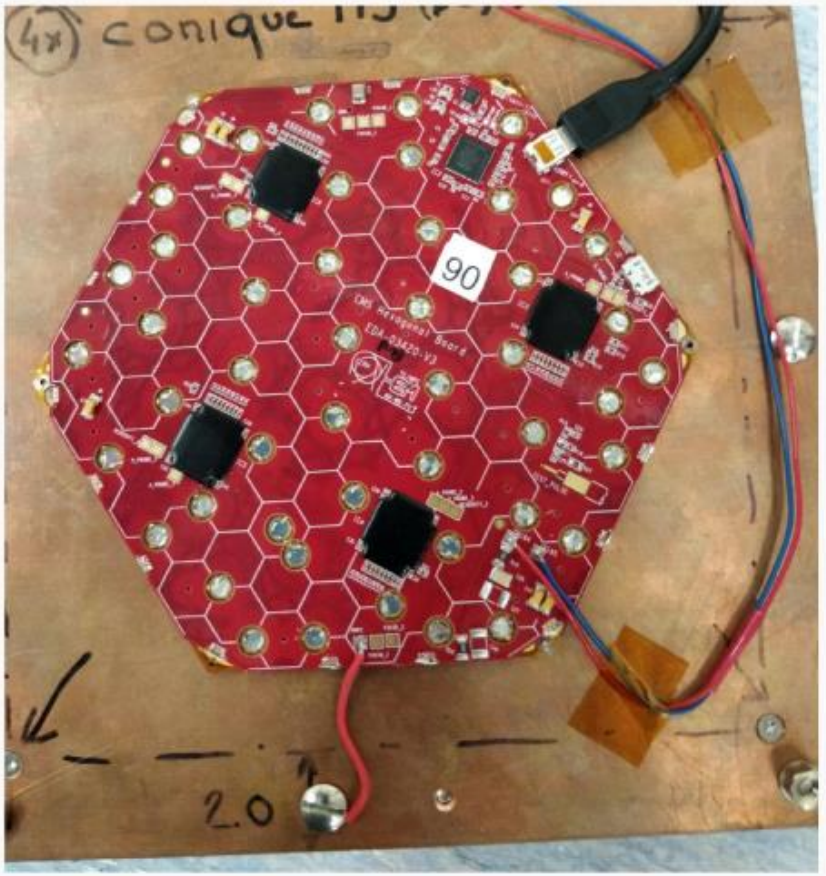
BEAM TESTS

Why beam tests

Several beam tests performed since 2016 with the following goals:-

- Test the proof of concept of the baseline design with a closely spaced stack-up of modules.
- Validate the design of compact detector modules.
- First experience with a FE ASIC including the 3 basic components of the future HGROC.
  - An ADC(with two gains) for small pulses.
  - A ToT for large pulses.
  - A precise measurement of the pulse timing (target ~ 50 ps for large S/N).
- Calorimetric performance of electromagnetic and hadronic sections.
- Validation of MC simulation.

6'' Si prototype Module



History of HGCAL beam tests

2016(CERN/Fermilab)

- Silicon: Up to 16 modules in CE-E layers.
  - Results summarized in the publication JINST 13(2018) P10023 .

2017(CERN)

- Silicon: 20 modules in CE-E & CE-H layers with Skiroc2-CMS* ASIC | Scintillator: CALICE AHCAL.
  - New beam test DAQ.

March 2018(DESY)

- Silicon: Studies of single module response

June 2018(CERN)

- Silicon: Full CE-E depth prototype with 28 modules.

October 2018(CERN)

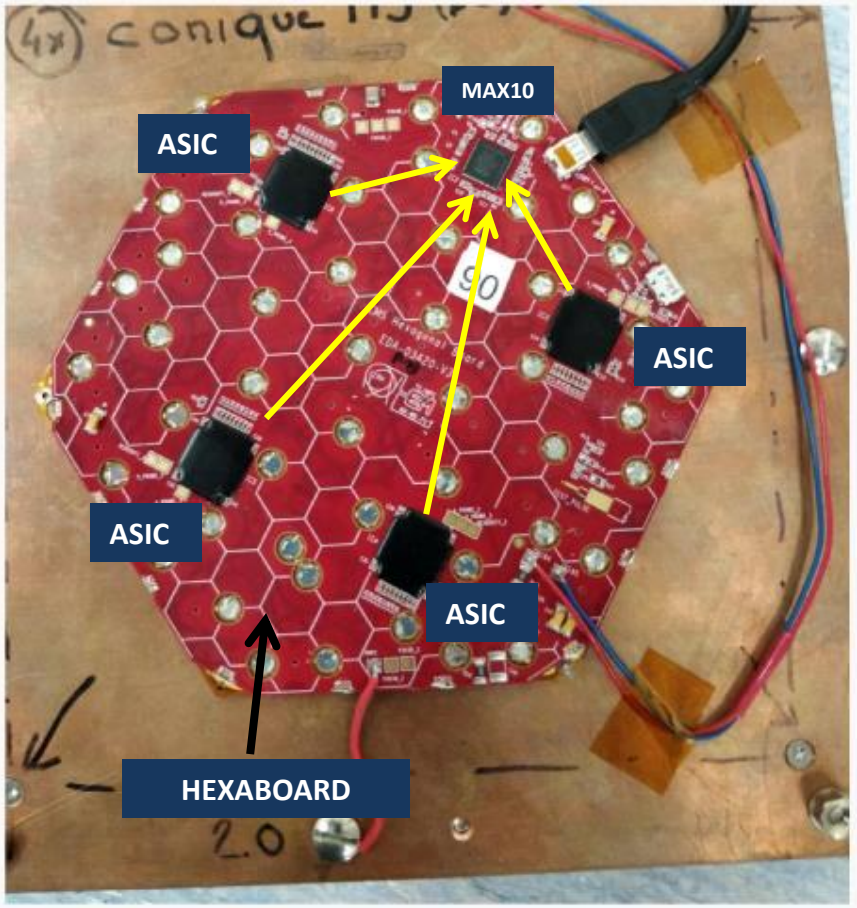
- Silicon: Up to 94 modules| Scintillator: CALICE AHCAL
  - Final major beam test before LS2.

* a special adaptation of a CALICE-developed chip to CMS read-out, in non-rad-hard technology

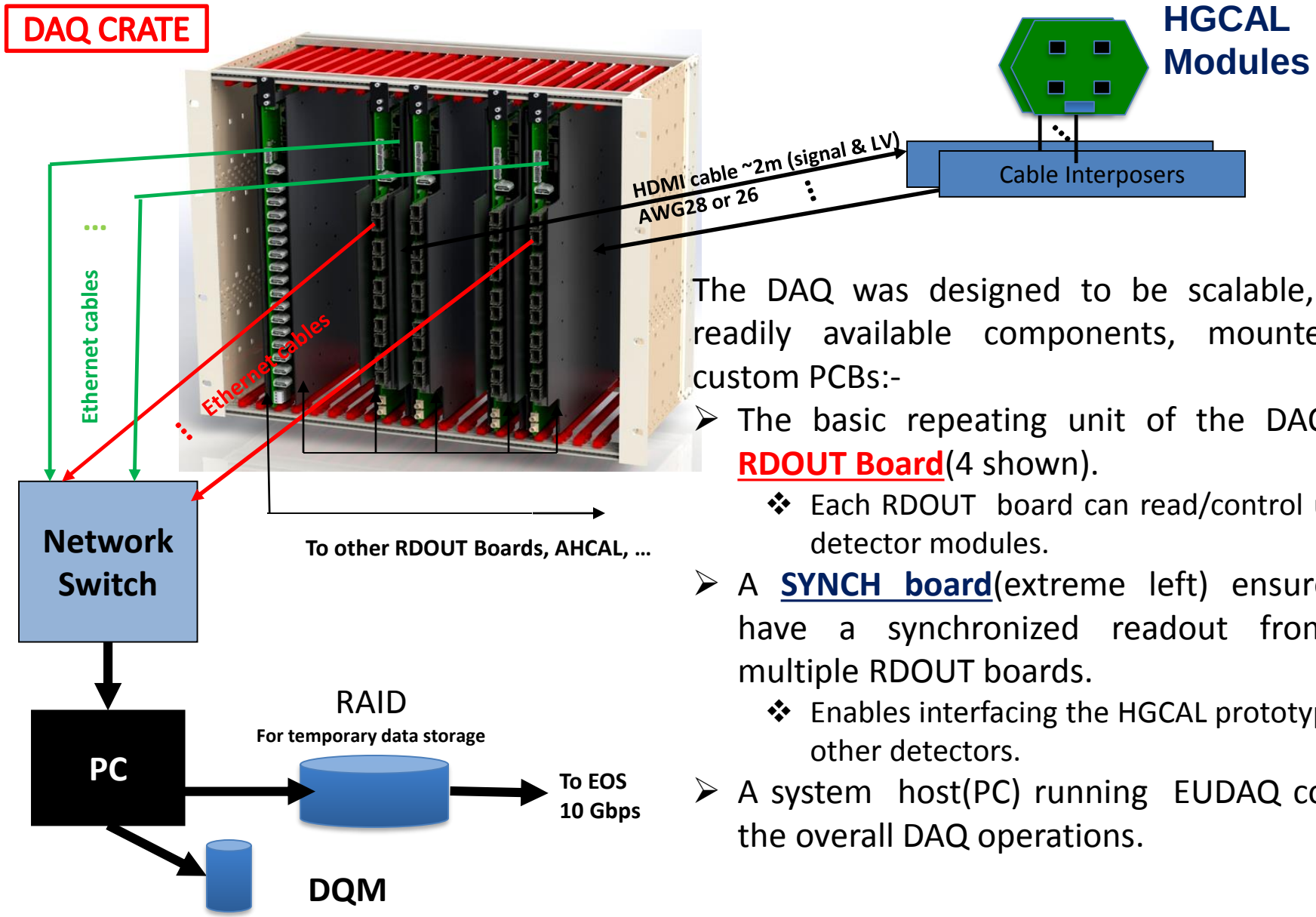
The data to be readout

- Each prototype module has 256 channels readout by 4 ASICs(Skiroc2-CMS).
- Per trigger the ASIC generates 1924 16-bit words.
  - For each channel 11 time samples in High and Low gain ADC. Additionally ToT and ToA.
- The local readout of these ASICs was controlled by a MAX10(Altera) FPGA.
- Signals from the MAX10 FPGAs were transmitted to a modular off-detector DAQ.

6'' Si prototype Module



DAQ system for HGCAL protoype: Overview

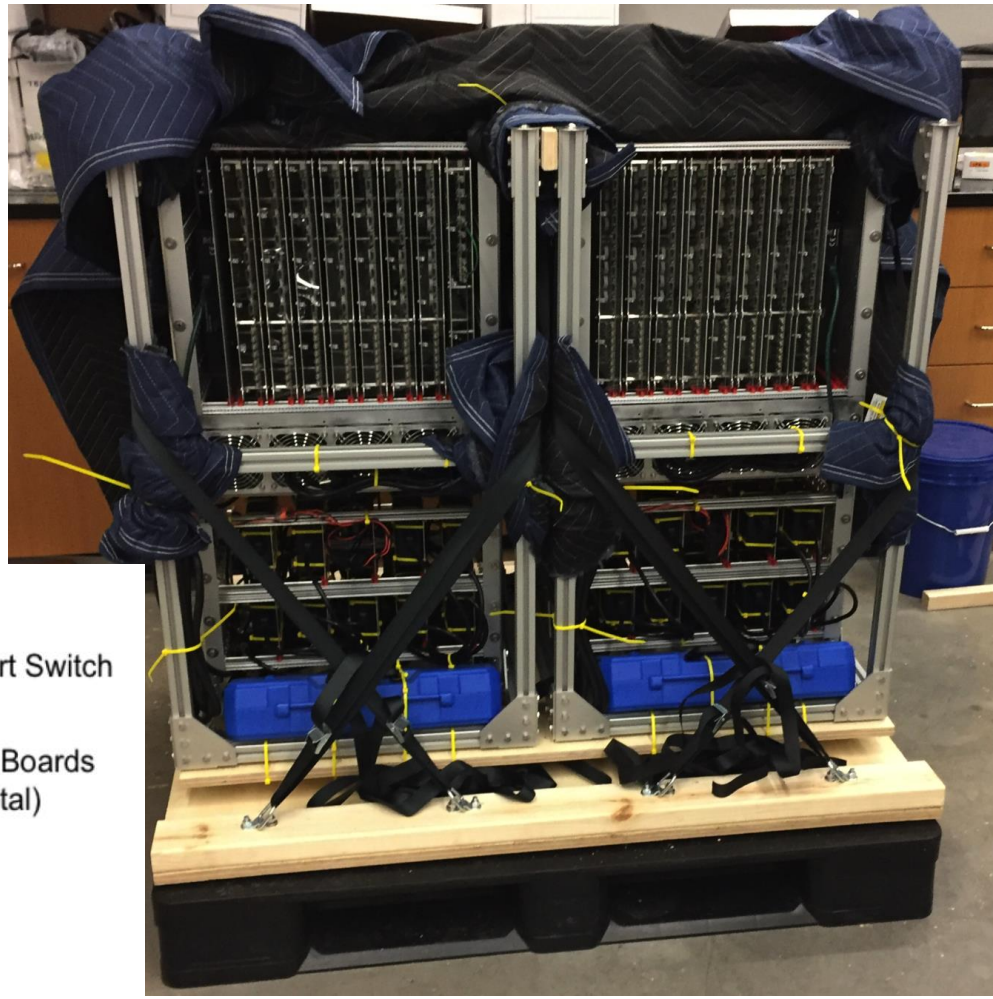


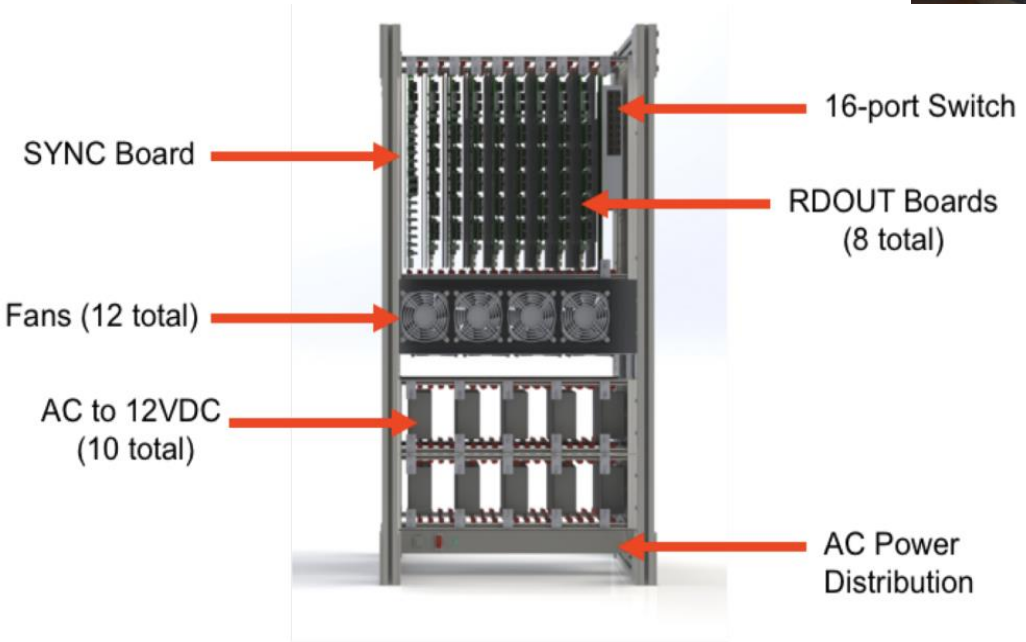
The DAQ was designed to be scalable, using readily available components, mounted on custom PCBs:-

- The basic repeating unit of the DAQ is a **RDOUT Board**(4 shown).
  - Each RDOUT board can read/control up to 8 detector modules.
- A **SYNCH board**(extreme left) ensures we have a synchronized readout from the multiple RDOUT boards.
  - Enables interfacing the HGCAL prototype with other detectors.
- A system host(PC) running EUDAQ controls the overall DAQ operations.

DAQ system for HGCAL protoype: Mechanics

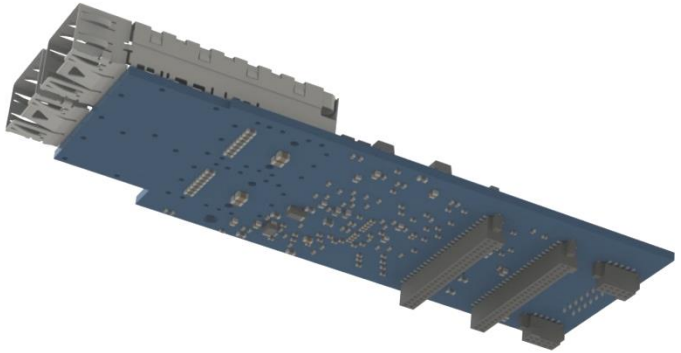
- The DAQ mechanics is modular and scalable.
- For the October, 2018 beam tests the DAQ comprised of 2 crates.
  - 14 RDOUT boards and 1 SYNCH board.



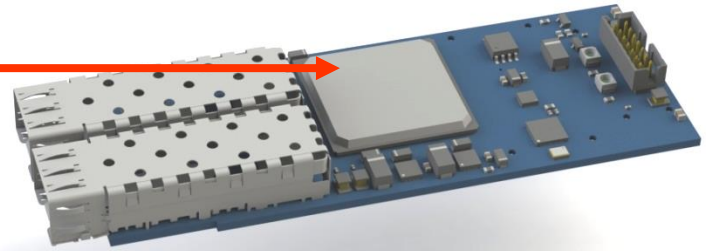


Key components of the DAQ

CMS optical Readout Module(oRM)



A common FPGA, “Optical Receiver Module”(oRM), was used in both the RDOUT and the SYNCH boards. These were previously used in the CMS trigger and had outlived their lifetime. Hence they were available at no cost!

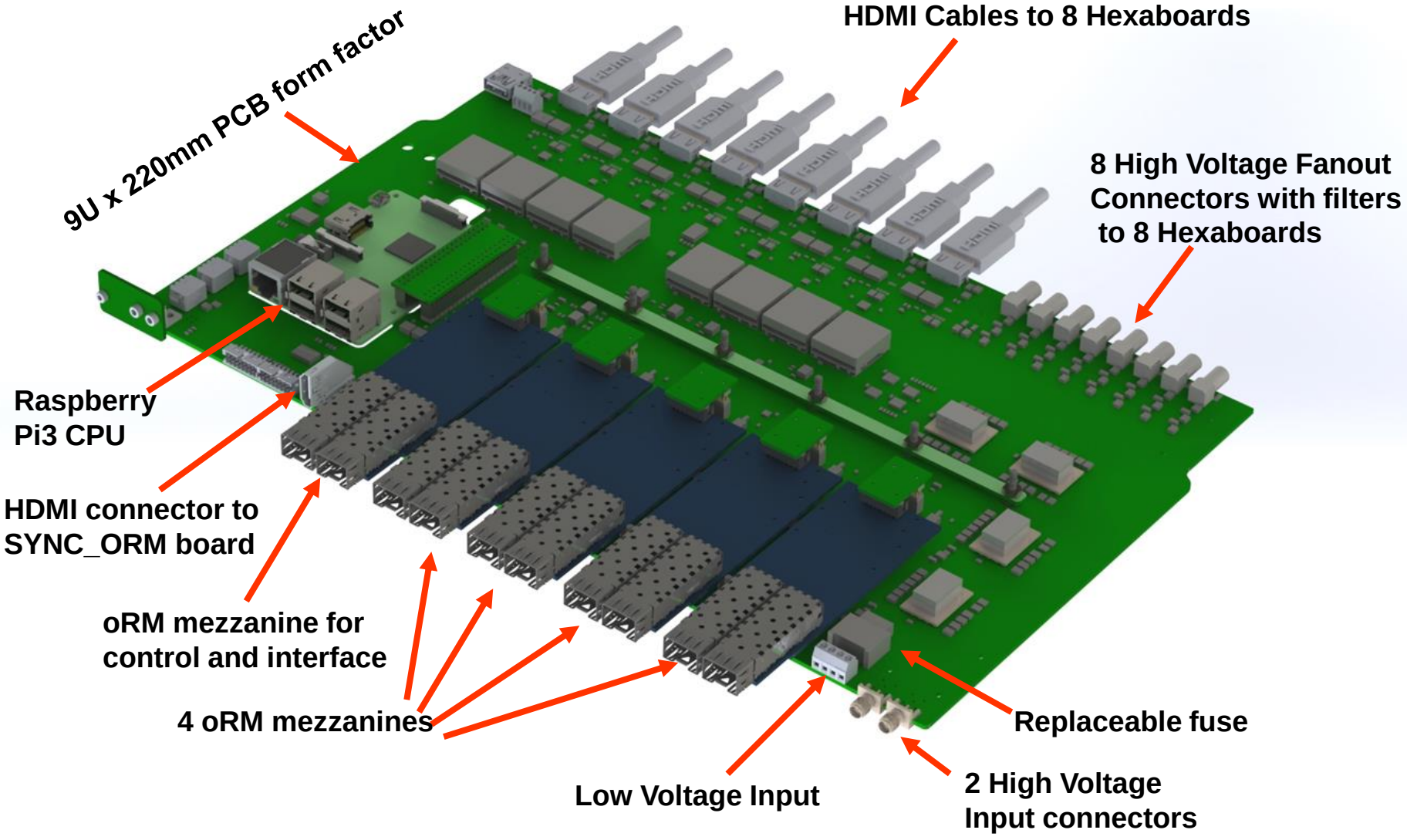


- Xilinx Kintex-7 XC7K70T-1FBG676C
  - 4.8 Mbits of block RAM
  - Two 6.6 Gbps bidirectional serial ports
  - 128Mbit FLASH memory for configuration

- The relevant firmware was written in Verilog.

- SFP to RJ-45 Adapter for direct connection from FPGA to GbE Switch.

RDOUT Board layout

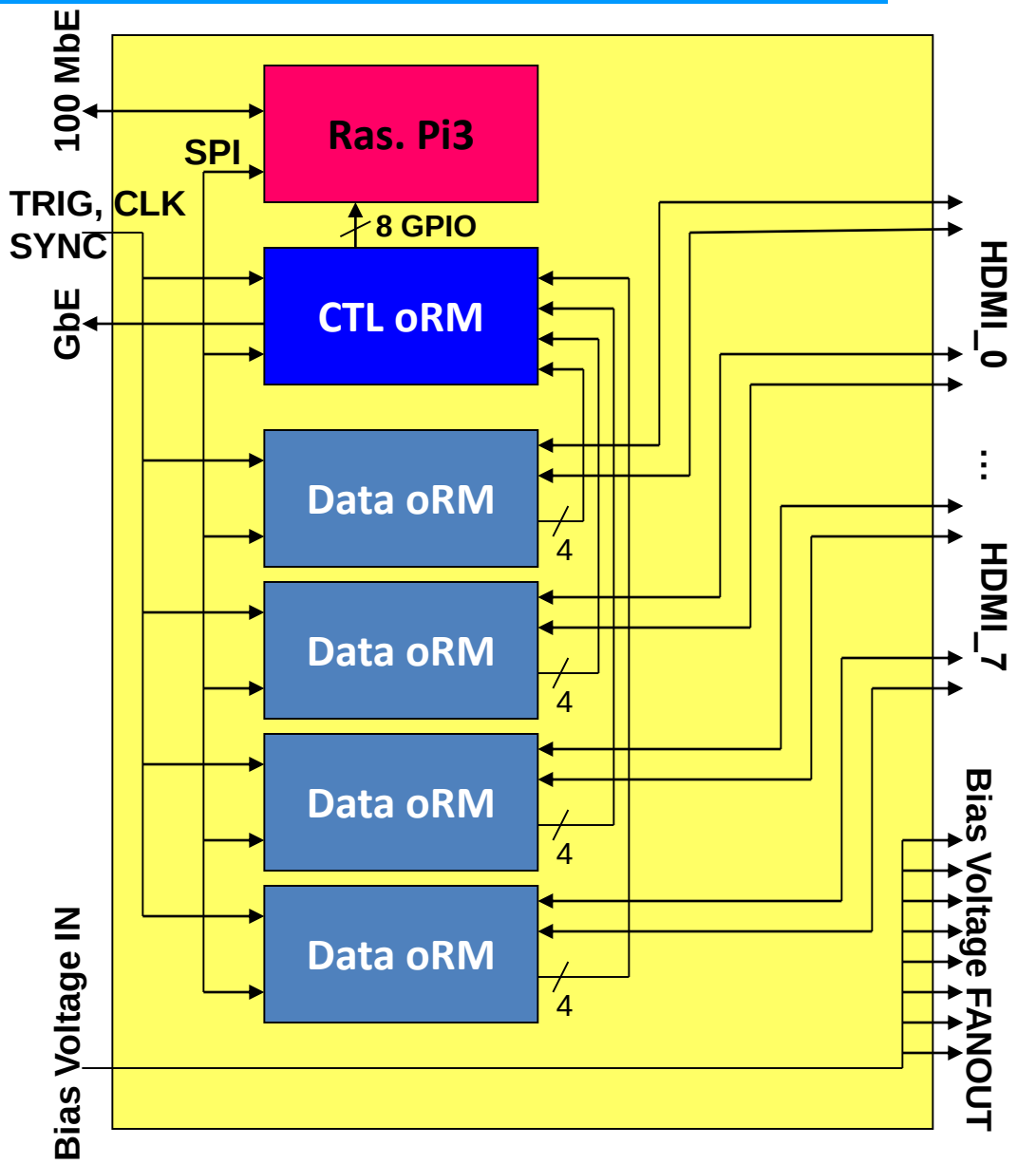


RDOUT Board

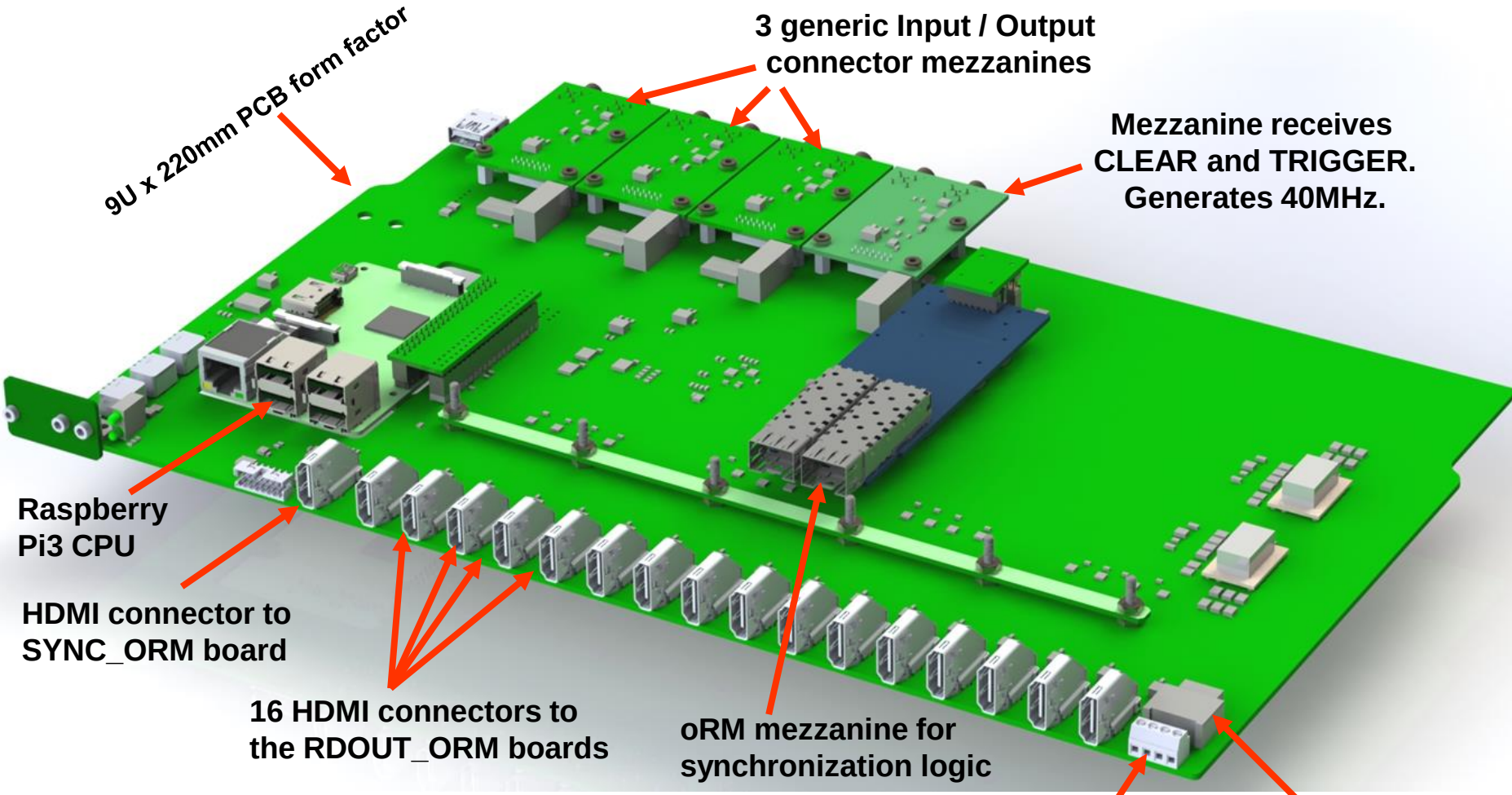
- Each readout board hosts 5 oRMs.
  - 4 “Data” oRMs read the data from up to 8 detector modules.
  - The 5th oRM controls the readout sequence, and “packs” the data from the Data oRMs
    - It is interfaced to the system host using the IPBUS protocol.

- A RPi, connected to the system host via ethernet, configures the ASICs on the HGCAL modules and also performs the slow control.
  - On completion of the readout after receiving a trigger a “readout done” signal is sent to the SYNCH board by the RPi.
  - The RPi can optionally perform the full readout operation at a slow rate(~ 1 Hz).

- The RDOUT board also distributes the low and bias voltages to the detector modules connected to it.

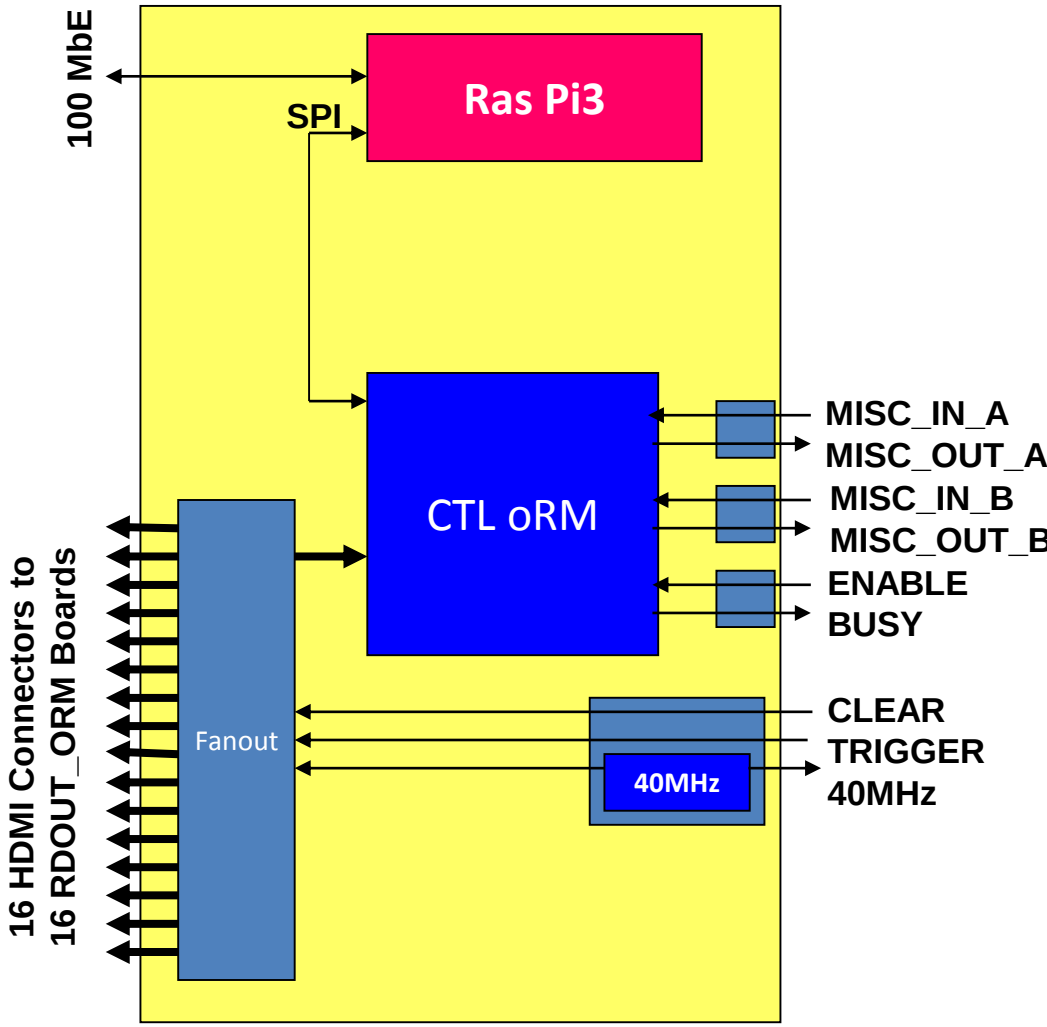


SYNCH Board layout

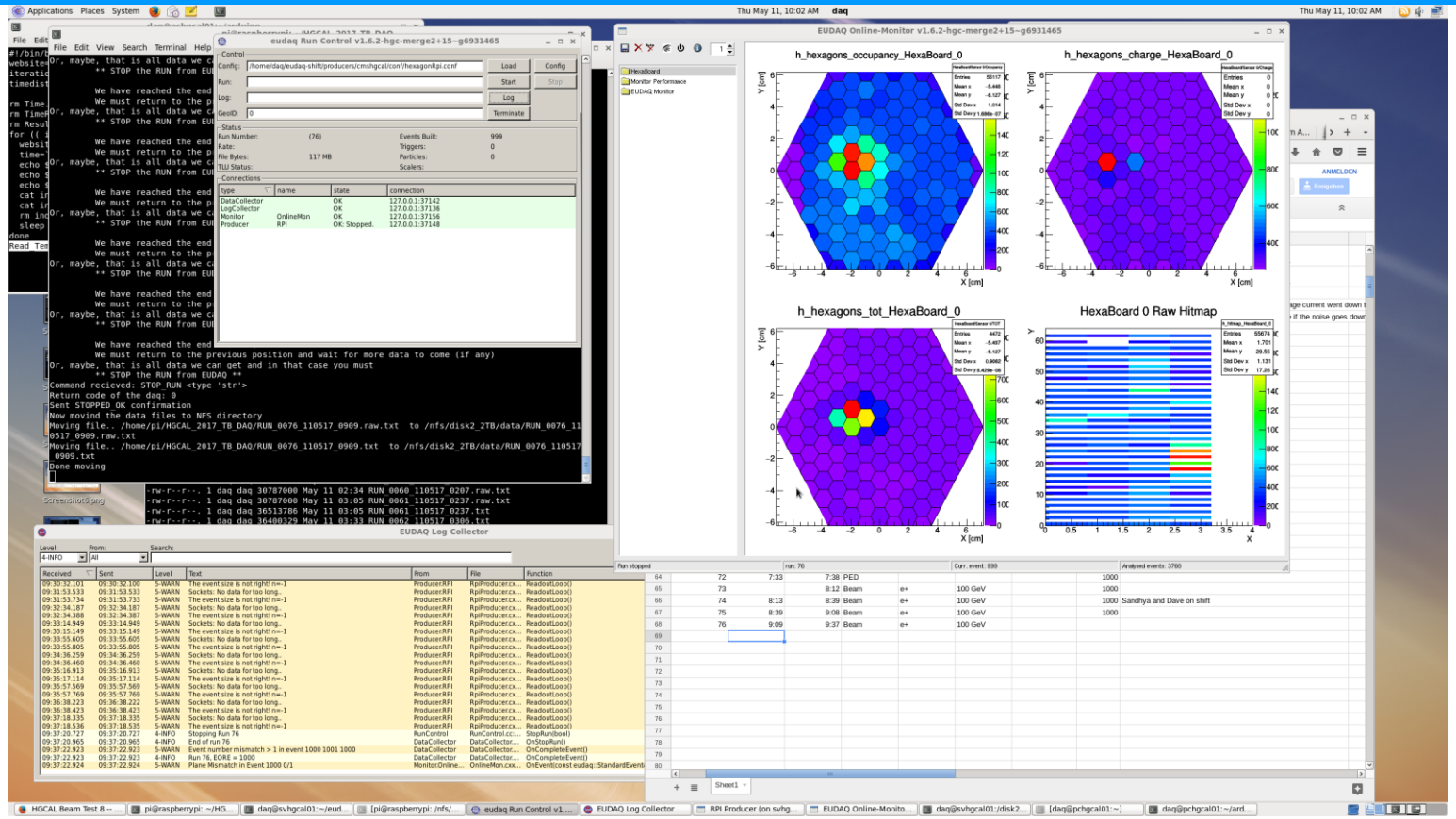


SYNCH Board

- Multiple RDOUT boards are operated in synchronization with the help of the SYNCH board, which hosts one RPi and one oRM.
- The SYNCH board forwards a copy of the trigger to all sub-detectors that are being operated together(RDOUT boards, DWCs and AHCAL).
- The SYNCH board distributes the 40 MHz system clock to the RDOUT boards.
- It receives a “readout done” signal from each of the RDOUT boards.
- While operating jointly with the AHCAL it received a veto from it.



System host and DAQ software



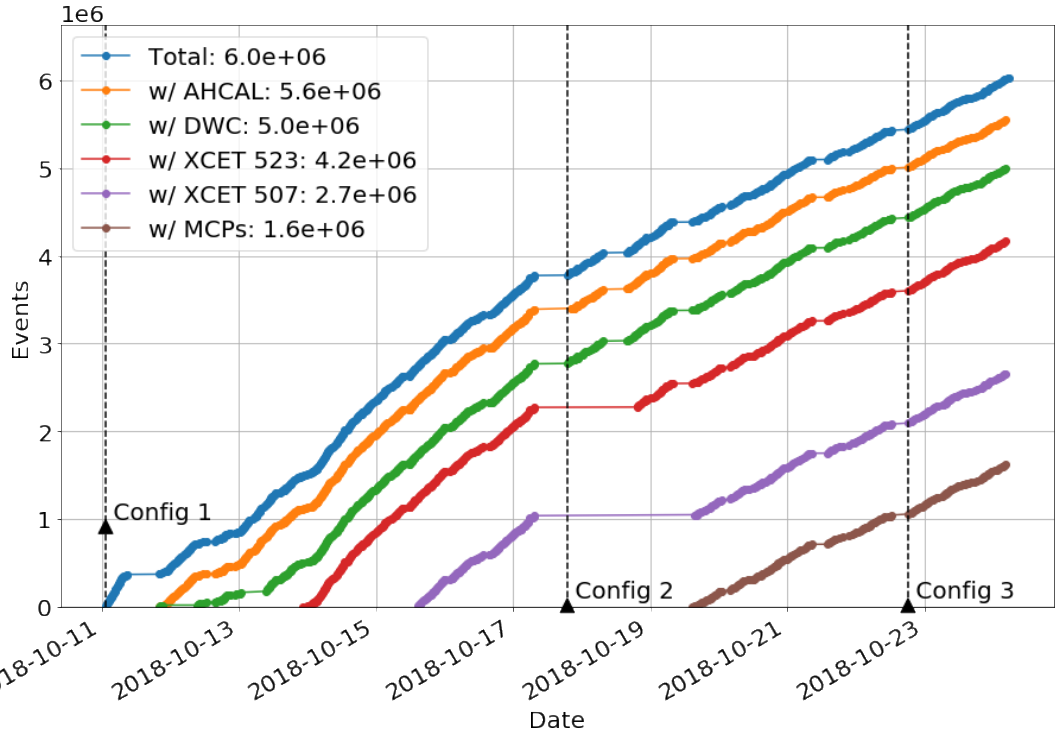
- The system host performs the overall run control, data readout, data storage and DQM.

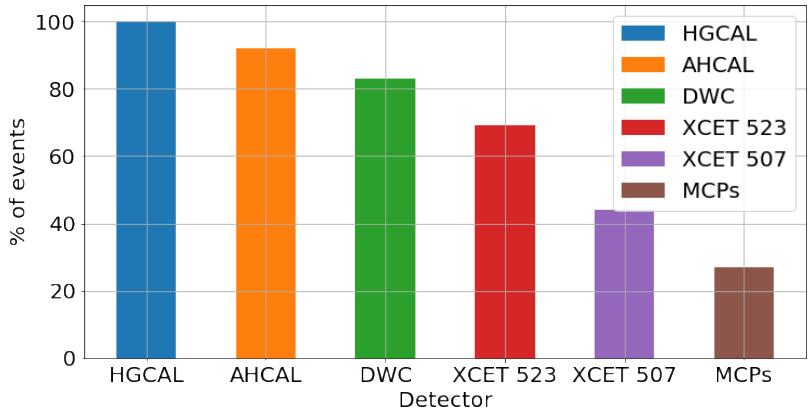
- The HGCAL DAQ software was developed in the EUDAQ framework.
  - Ensures all DAQ software(AHCAL DAQ, HGCAL with IPBUS, VME modules and their optical readout) are centralized in the same framework.
  - Enables a common DQM.

DAQ operations: scalability, throughput

- The DAQ is easily scalable.
  - Operated with **1 detector module(256 channels)** in DESY to **94 detector modules(24k channels) readout by 14 RDOUT boards** in CERN!
- The DAQ design allows for up to 12 groups of RDOUT boards, each under the control of one SYNCH board, to be controlled by a master SYNCH board.
- The SYNCH board enables other detectors to be interfaced for joint data taking.
  - The HGCAL prototype has been operated jointly with delay wire chambers, a beam telescope, MCPs, Cerenkov detectors and the CALICE AHCAL(See T. Quast's slides for more details).
- The DAQ was operated at readout rate of 40 Hz.
  - Possible to improve it further to ~100 Hz.
- At this rate the amount of data readout for a typical 5 sec SPS spill for the HGCAL(EE+FH) was **300 Mb.**
  - **~16 Kb per module per trigger; ~ 1.5 Mb for 94 modules per trigger.**
- In future the use of this DAQ can be extended for any system with the order of 20k channels, where the signal from on-detector modules are transmitted on HDMI cables and the readout rate is < 100 Hz.

Data collected





- 6 million events accumulated in multiple detector configurations over 2 weeks.
  - Wide range of energies for electrons and pions from 20-300 GeV.

Summary

- The current DAQ for the HGCAL beam test prototype has been operational since 2017.
- In the latest beam tests held in CERN in October 2018, a total of 94 detector modules were readout.
- Other detectors can be interfaced with this DAQ for joint data taking.
- In future the use of this DAQ can be extended to readout any system where the on-detector signal can be transmitted via HDMI.

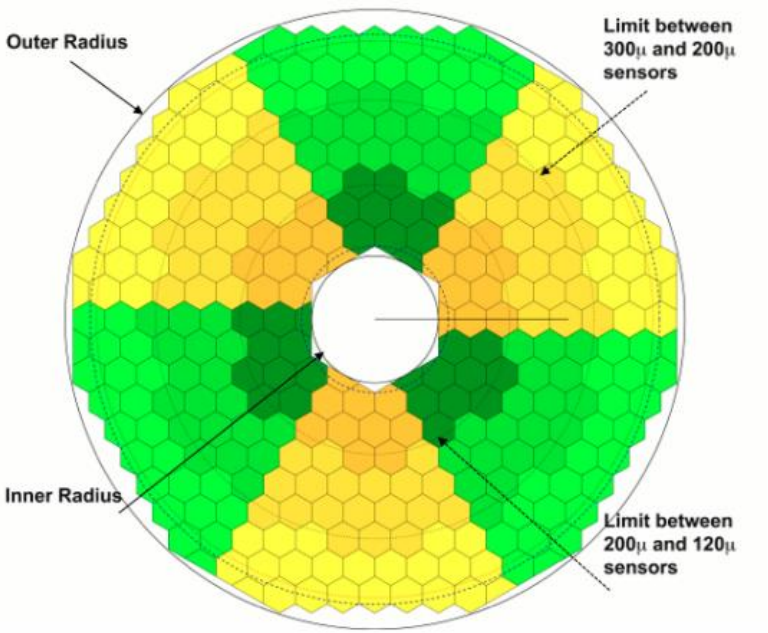
BACKUP

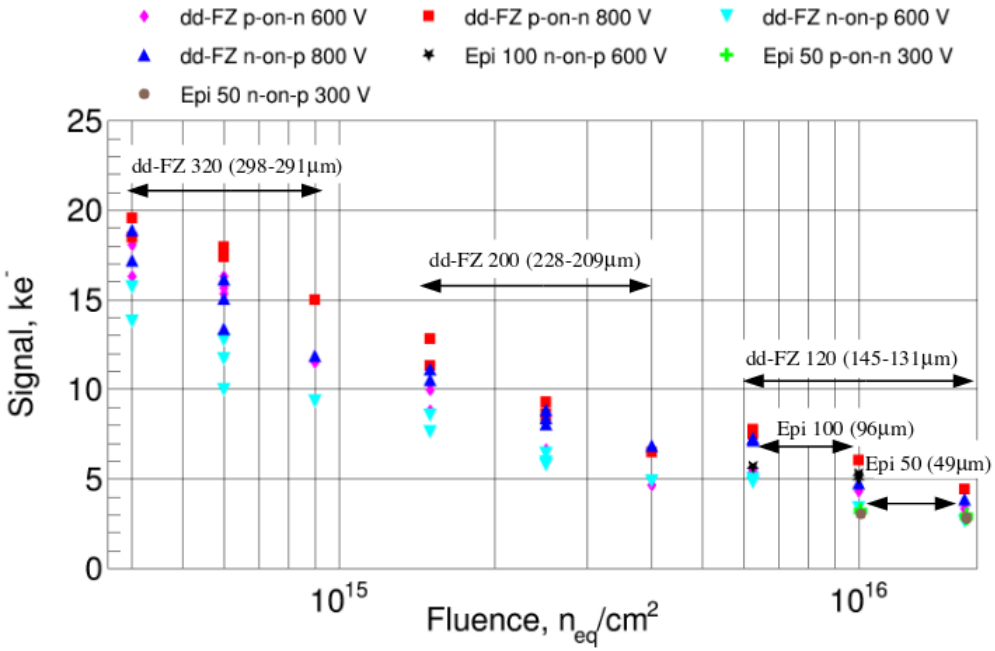
The HGCAL consists of a Si sampling calorimeter

WHY Silicon ?

- Extensive R&D, for the Tracker and Pixel detectors over the last 20 years have led to the development of Si sensors that can sustain the high radiation levels of the HL-LHC
  - Fluence at $|\eta| = 3$ in HGCAL ~ same as inner pixel layer in CMS during HL-LHC.
  - Radiation effects are well understood and reproducible. Can be mitigated by low T operation.
- Fast signal collection(**< 10ns**) and fast timing capability(**~15 ps**).
- High granularity with fast timing, enables 3D tracking which helps mitigate pileup effects(**<pileup> ~140 at a luminosity of $5*10^{34}$ Hz/cm^2**).
- Affordable cost.
- Electronics in 130/65 nm allows low noise and low power readout Front-End(**10-15 mW per channel**).

Si sensors for HGCAL





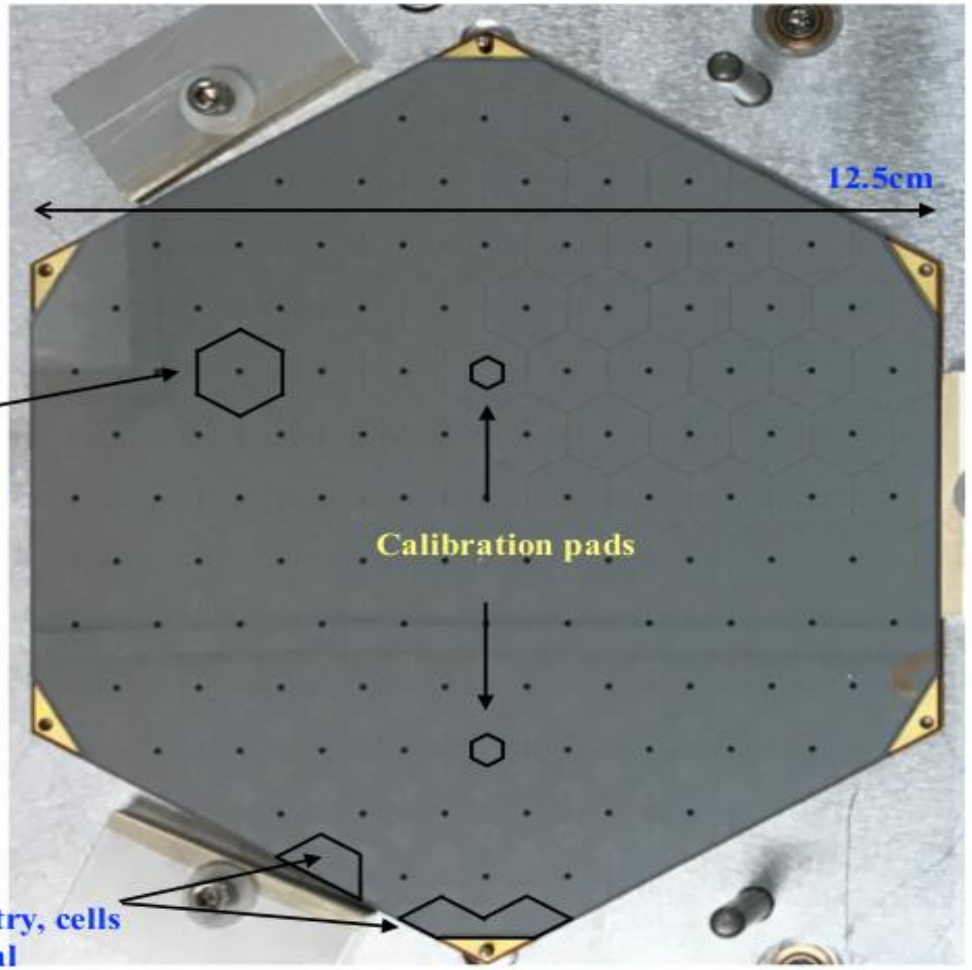
- 8'' hexagonal silicon sensors p/n-type | 192/432 cells .

- **At higher radiation levels its beneficial to use thinner sensors. E-field higher for the same bias.**
- **Higher η region: Sensors with 120 μm depletion depth.**
- **Lower η region: 200 μm & 300 μm**

- **Cell size ~ 1 cm² for 200 μm & 300 μm depletion sensors.**
- **~ 0.5 cm² for 120 μm depletion sensors.**
- **Cell size reduction to maintain moderate capacitance(< 50 pF).**

128 channel Si sensor for beam tests

"p-on-n" with 200/300 μm depletion thickness, made from 6" wafers, Cell size ~ 1 cm^2



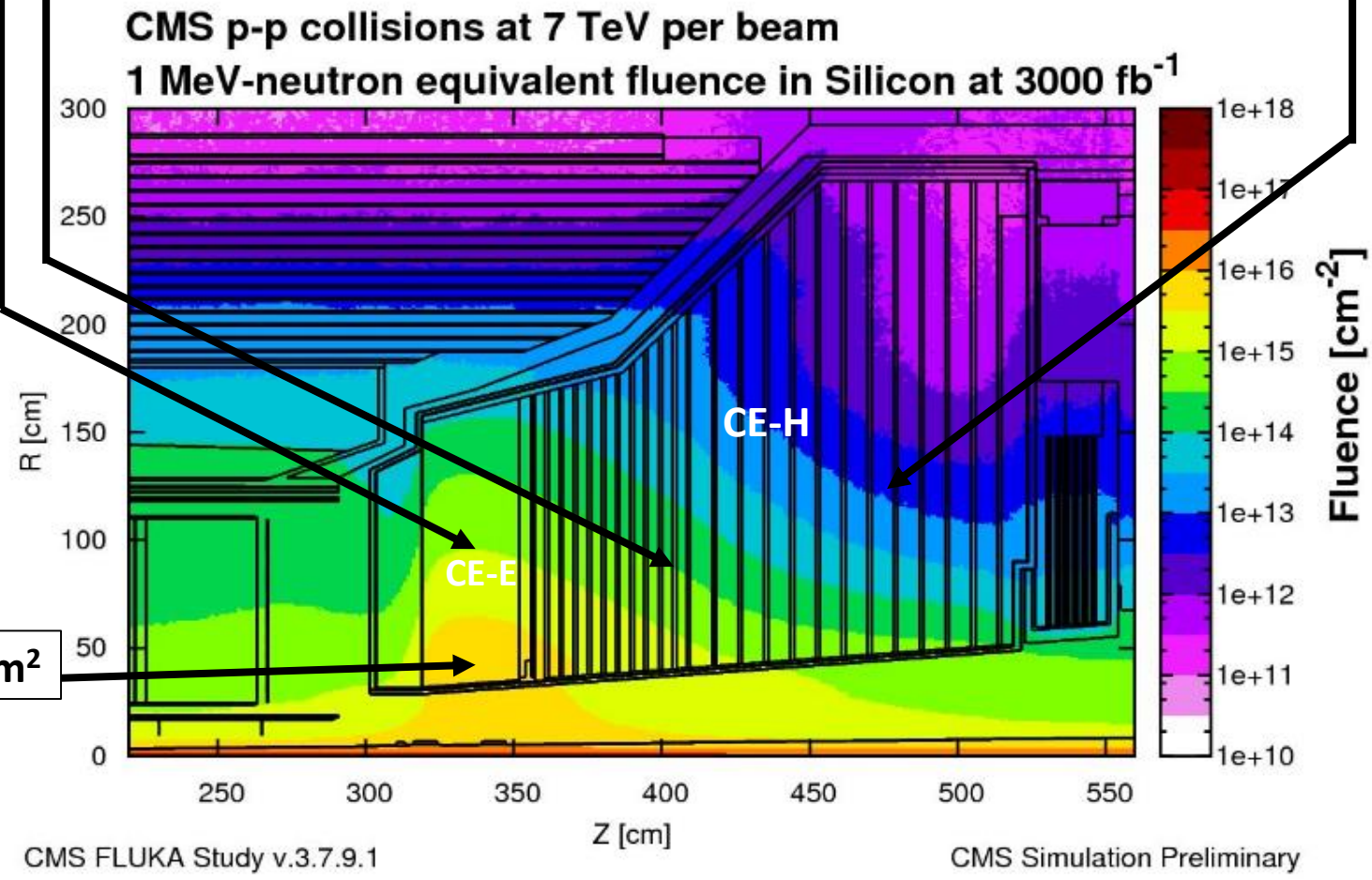
shows one of the hexagonal cell on the wafer

Due to the hexagonal geometry, cells around the edges need special attention

HL-LHC radiation environment

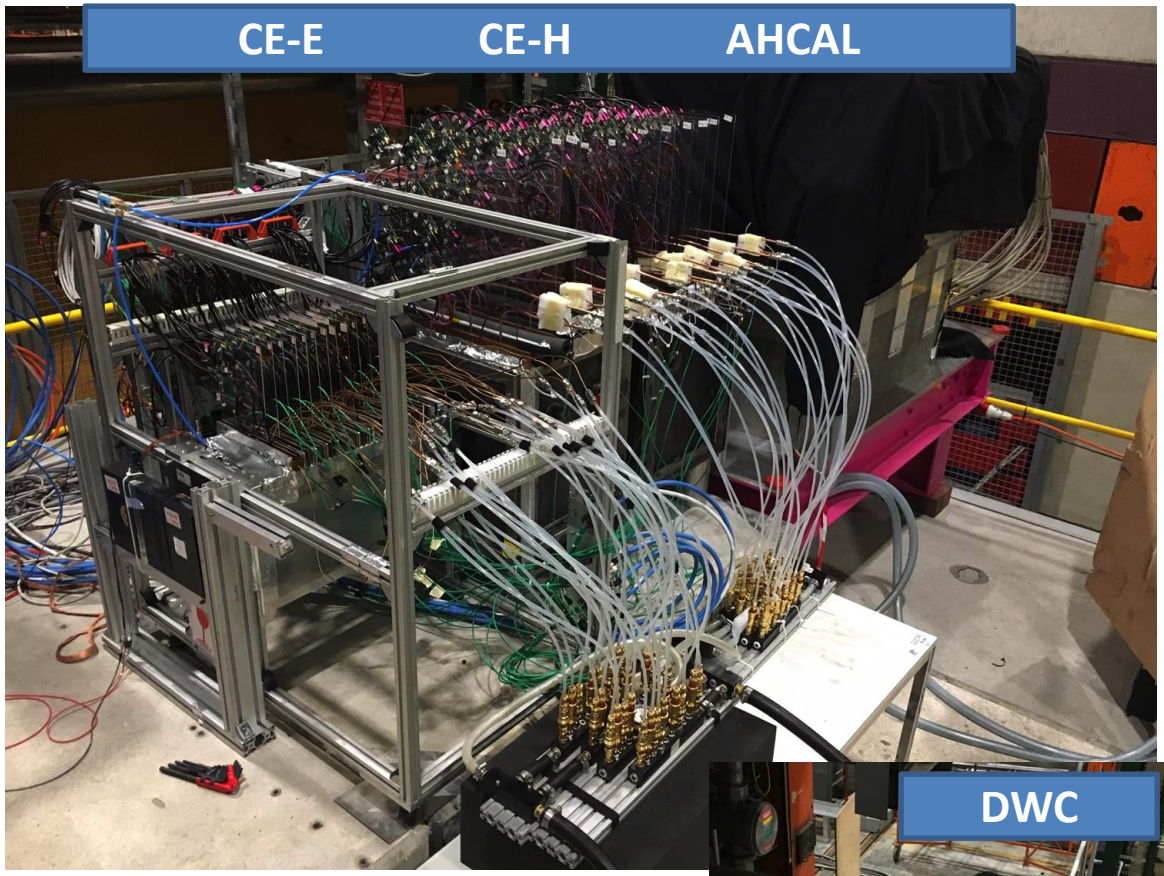
Si sensors in the higher radiation parts of CE-E and CE-H

Scintillator in the lower radiation parts of CE-H

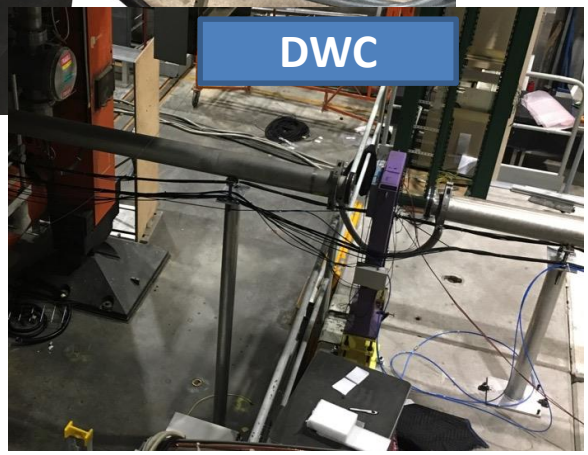


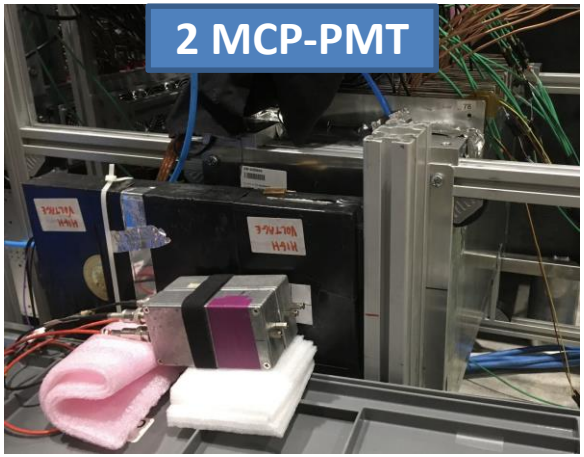
***10^{16}* n/cm^2**

HGCAL October, 2018 beam test setup



- HGCAL: silicon CE-(E) and CE-(H) with 94 modules, up to 40 layers.
- AHCAL: SiPM-on-scintillator tile in 39 layers.
- Delay wire chambers for tracking.
- Cerenkov counters for π/p ID.
- MCP-PMT: Timing ref. (σ ~ 30ps).





RDOUT and SYNCH Board