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# Overview of the modular DAQ hardware designed for beam tests of the HGICAL prototype

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The CMS collaboration has decided to replace the current endcap calorimeters with a new High Granularity Calorimeter (HGICAL) for operations at the High Luminosity LHC (HL-LHC). To validate the design of the HGICAL, prototype detector modules based on silicon pad sensors have been manufactured and tested extensively both in the laboratory and in beam tests. Each prototype module has 128 channels readout by 4 custom ASICs (SKIROC2CMS). The local readout of these ASICs was controlled by a MAX10 FPGA. Signals from the MAX10 FPGAs were transmitted to a modular off-detector DAQ, which was designed for this detector prototype largely using commercially available components.

The basic unit of this DAQ, called a RDOUT board, controlled the readout from up to 8 detector modules. The RDOUT board employed 5 Kintex7 FPGAs, four of which were for the readout itself. The 5th FPGA controlled the readout sequence and interfaced with the system host via Ethernet using the IPBUS protocol. The RDOUT board was also used to distribute the low and bias voltages to the detector modules connected to it.

Multiple RDOUT boards were operated in synchronization with the help of a SYNCH board, which also uses a Kintex7 FPGA. In addition to synchronization the SYNCH board distributed the clock and the external trigger to the RDOUT boards. It also enabled us to interface our DAQ with those of other detectors for multi-detector operations. Every board in the system was equipped with a Raspberry Pi3 for slow control and testing. The core firmware and software for the DAQ were written in Verilog and C respectively, the latter being based on the EUDAQ framework.

The DAQ was designed to be scalable so that up to 12 groups of RDOUT boards, each under the control of one SYNCH board, could be controlled by a master SYNCH board. In the latest beam test held in October, 2018 the prototype detector comprised 93 detector modules with a total of nearly 24000 electronic channels readout by 14 RDOUT boards. Along with the HGICAL prototype, the CALICE AHCAL prototype was operated jointly with a system host running EUDAQ. We present here the design of this DAQ, our experience operating it, and our plans for future operations with the same.

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