

# AIDA-2020

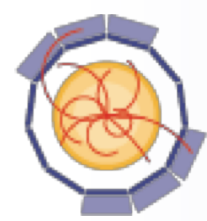
# Trigger Logic Unit (TLU)

David Cussans

BTTB7 , CERN , 17<sup>th</sup> January 2019

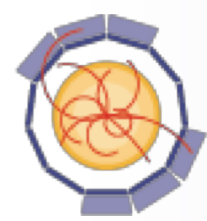


This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.

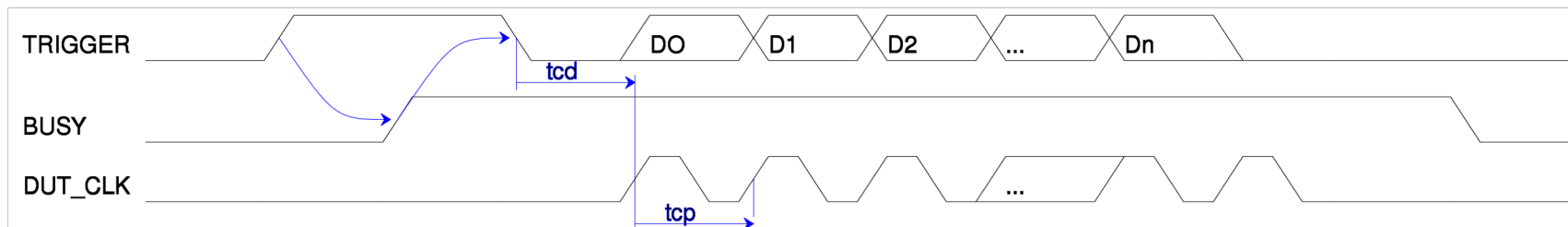
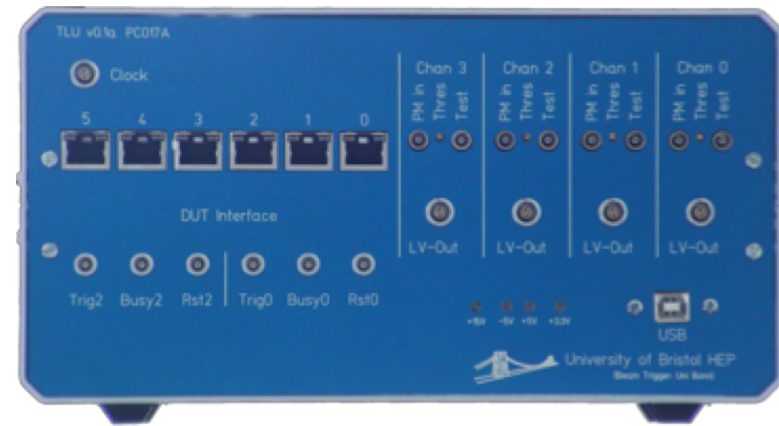


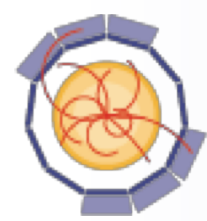
- During beam-test frequently want to:
  - Synchronize a detector under test (DUT) with external signals
    - E.g. scintillators to trigger on beam particles
    - Cherenkov detectors (for PID)
    - Accelerator (e.g. Spill signals, max-energy)
  - Synchronize with other detectors
    - E.g. With beam-telescope





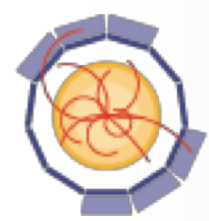
- Originally designed for use with beam-telescope with low beam rate
- Handshake designed to allow independent clocks
  - (Optional) transfer trigger number from TLU → DUT





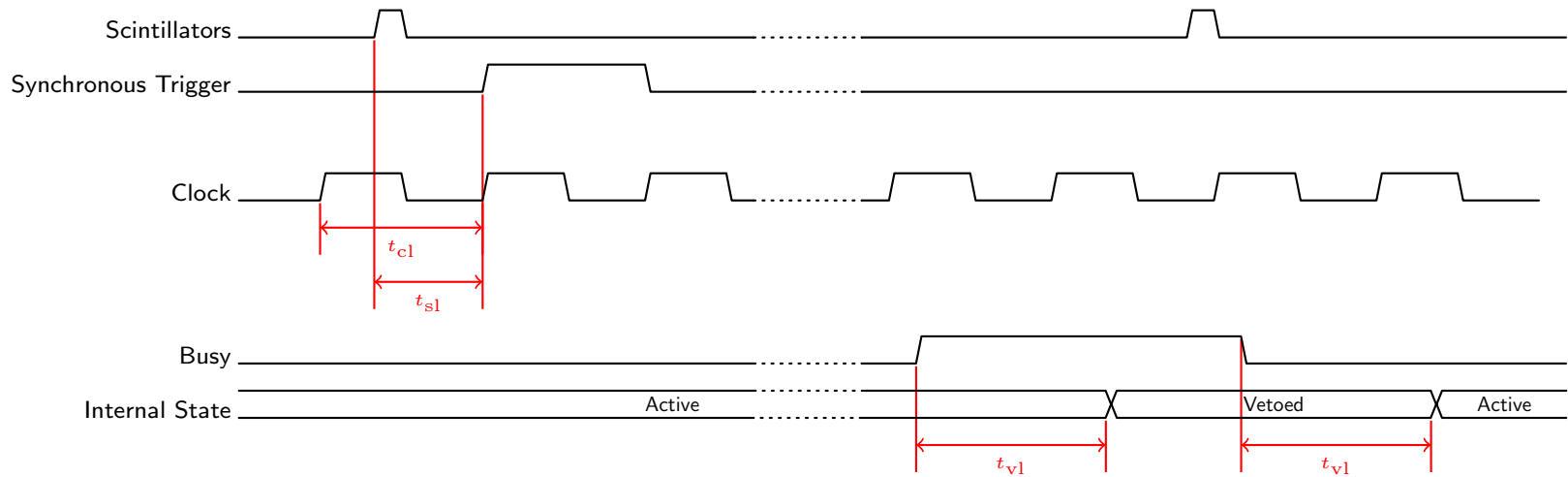
- EUDET TLU designed for ILC tests.
  - Telescope with “rolling shutter” MAPS pixel sensors (Mimosa family).
  - Trigger rate of EUDET system limited by frame readout to ~5kHz
    - → increasing use of beam telescopes by LHC detectors. Want higher trigger rate
  - No common clock → Difficult to interface to self-triggering detectors
    - E.g. some calorimeters.
  - FPGA inside EUDET TLU becoming obsolete.
- → New TLU designed as part of AIDA-2020 project
  - Open hardware, Open firmware (<https://www.ohwr.org/projects/fmc-mtlu>)





# AIDA<sup>2020</sup>

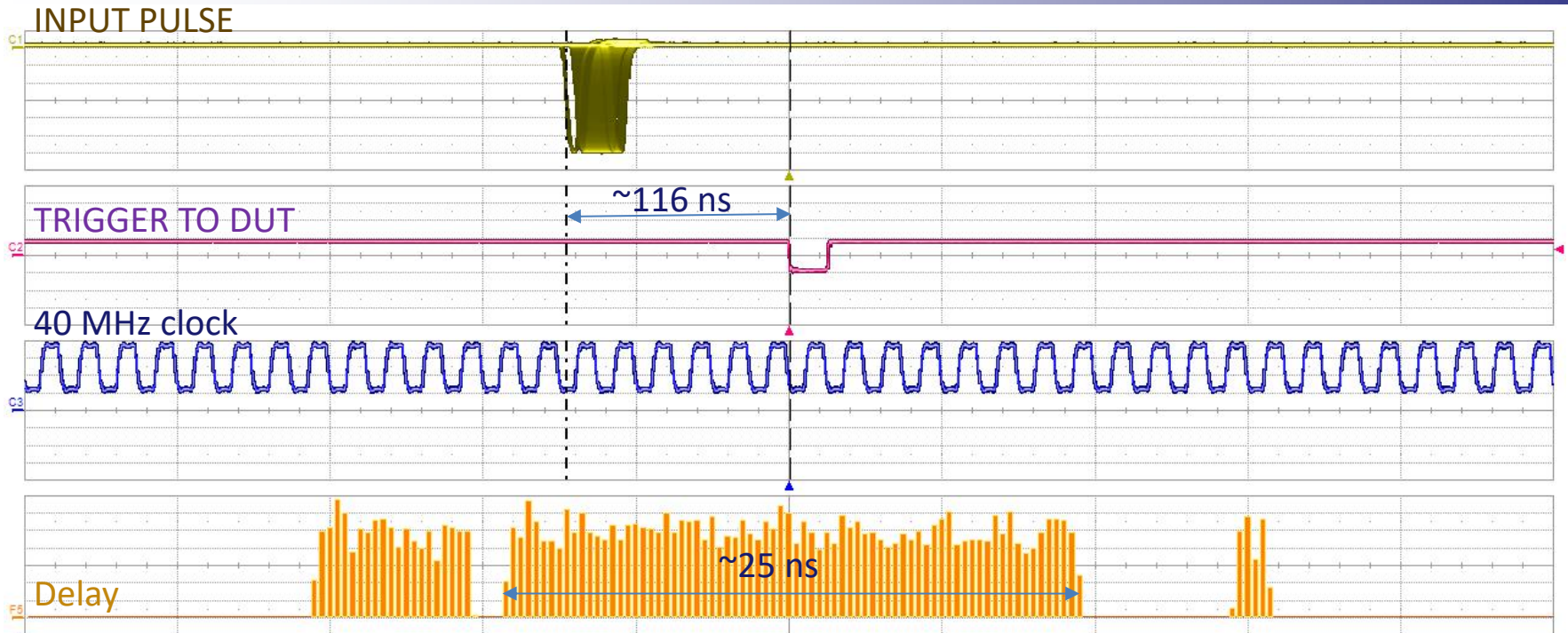
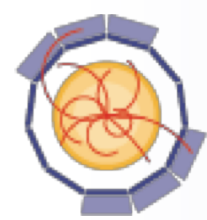
# Synchronous (“AIDA”) Interface



- DUT operates with same clock at TLU
- Allows faster interface
- Cross check by matching time-stamp and trigger number
- AIDA TLU can mix asynchronous (EUNET) and synchronous (AIDA) mode interface



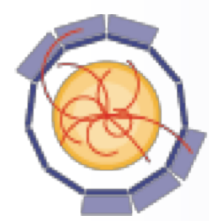
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Measure	P1: dt@lv(C1.C2)	P2: freq(C4)	P3: ---	P4: ---	P5: freq(C4)	P6: ---	P7: ---	P8: ---
value	135.0389 ns	39.6383 MHz						
mean	128.499 ns	40.0063 MHz						
min	114.7949 ns	38.8166 MHz						
max	146.1616 ns	41.2087 MHz						
sdev	7.984 ns	271.6 kHz						
num	14.050e+3	607.737e+3						
status	✓	⚠						

C1	DC1M	C2	DC50	C3	DC1M	F5	hist(P1)
200 mV/div	1.00 V/div	500 mV/div	10.0 #/div				
595.0 mV	0 mV offset	0 mV offset	5.00 ns/div				
			5.000 k#				
Δy	Δy	Δy	Δy				

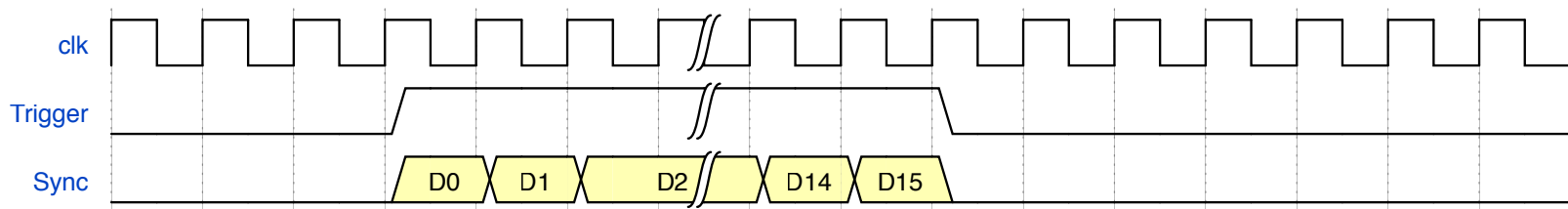
Timebase	0 ns	Trigger	C2 DC
	100 ns/div	Stop	280 mV
20 kS	20 GS/s	Edge	Neg
X1=	-146.10 ns	ΔX=	146.60 ns
X2=	500 ps	1/ΔX=	6.821 MHz



# AIDA<sup>2020</sup>

## Synchronous Interface with Trigger Number

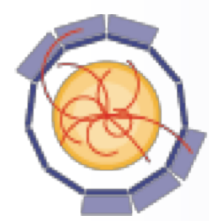
- Synchronous (“AIDA”) interface mode will be extended to transmit trigger number
  - Transmitted by TLU
  - Synchronous with transmitted clock.



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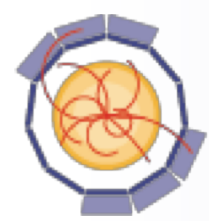




AIDA<sup>2020</sup>

# Desktop Enclosure





# AIDA<sup>2020</sup>

## 19-inch enclosure

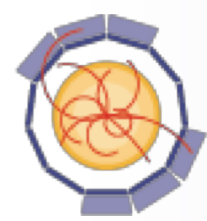


110V –  
240V power

2 x 16  
character  
display

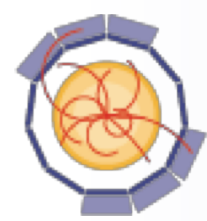


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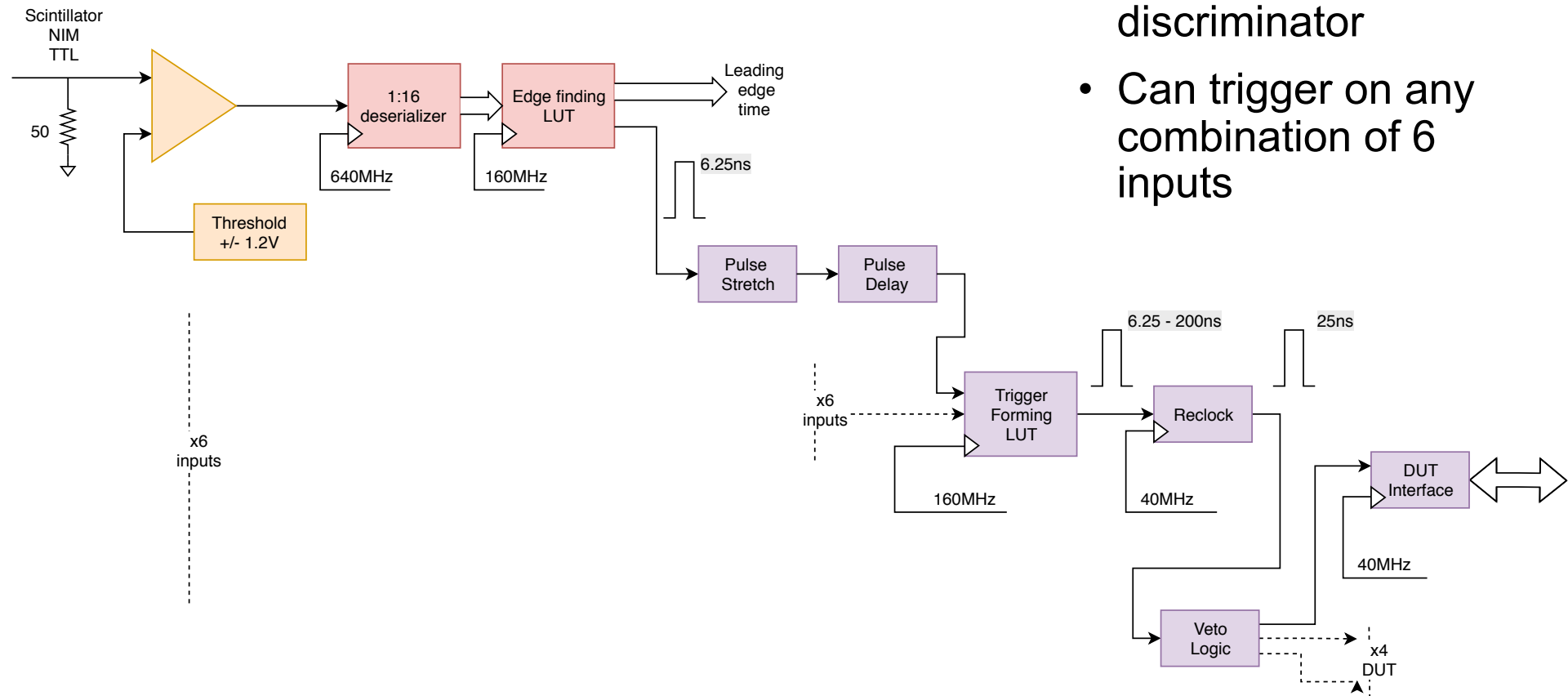


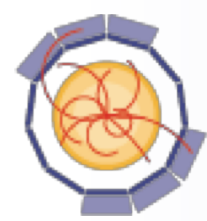
- Four Device Under Test (DUT) Interfaces
  - Five LVDS signals on HDMI connectors
    - ( chosen to be compatible with CALICE)
    - Converted by passive “dongle” to RJ45 interface used by EUDET TLU
    - Converter to/from LVDS available ( thanks to CMS pixel upgrade group)
- Six trigger inputs
  - +/- 5V range
  - Adjustable threshold +/- 1.3V
  - Fully configurable trigger “mask”
- Clock input or output
  - Adjustable frequency, typically 40MHz
  - LVDS clock input. Either on 2-pole “Lemo” or HDMI
- Optical I/O
  - Currently used for protoDUNE
  - Hardware compatible with LHC TTC format





- Simple threshold discriminator
- Can trigger on any combination of 6 inputs

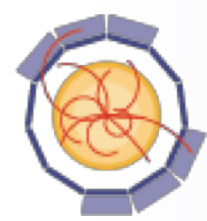




- 19 units produced
  - 10 in benchtop , 9 in 19-inch enclosures
- Units delivered to DESY and CERN
- Available to other groups at Euro 2.2k each.
- Completed porting of firmware from old to new hardware
  - Maintain all functionality from old TLU
  - Tested new functionality (clock generator, discriminators, trigger)
  - Serial encoded clock / sync / trigger over optical fibre implemented for protoDUNE ( not TTC format )



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- Integrated with EUDAQ2:
  - Current version of TLU producer stable and working with EUDAQ2
  - Allows to configure the TLU and read data
  - Tested at CERN and DESY
  - Aiming for up to 1MHz average trigger rate
  - Testing/debugging ongoing

```
Success.
Scan I2C Bus:
  I2C slave at address 0x8 replied but is not on TLU address list. A mystery!
  FOUND I2C slave DAC1
  FOUND I2C slave DAC2
  I2C slave at address 0x2f replied but is not on TLU address list. A mystery!
  FOUND I2C slave EEPROM
  FOUND I2C slave EEPROM
  I2C slave at address 0x54 replied but is not on TLU address list. A mystery!
  I2C slave at address 0x4f replied but is not on TLU address list. A mystery!
  FOUND I2C slave CLOCK
  FOUND I2C slave EXPANDER1
  FOUND I2C slave EXPANDER2
TLU Unique ID : d8be7d7dff3
DAC (0x13) reference set to EXTERNAL
DAC (0x1f) reference set to EXTERNAL
I/O expanders: initialized
S15345 EEPROM:
  5345
Parsing clock configuration file:
  /users/jppgb/eudaq2/conf/newTLU.conf
S15345 Writing configuration (384 registers):
  384/384 Success
S15345 design ID:
  NEWTLU01
Setting HDMI 1 to false
Setting HDMI 2 to false
Setting HDMI 3 to false
Setting HDMI 4 to false
Setting HDMI 1 clock source:
  S15435
Setting HDMI 2 clock source:
  S15435
Setting HDMI 3 clock source:
  S15435
Setting HDMI 4 clock source:
  S15435
Clk LMO disabled
Setting DAC channel 0 = 63014
Setting threshold for channel 0 to 1.2 Volts
Setting DAC channel 1 = 63014
Setting threshold for channel 1 to 1.2 Volts
Setting DAC channel 2 = 63014
Setting threshold for channel 2 to 1.2 Volts
Setting DAC channel 3 = 63014
Setting threshold for channel 3 to 1.2 Volts
Setting DAC channel 4 = 63014
Setting threshold for channel 4 to 1.2 Volts
Setting DAC channel 5 = 63014
Setting threshold for channel 5 to 1.2 Volts
TRIGGER PATTERN (for external triggers) SET TO 0xffdeeddf --- 0xffbae550 (Two 32-bit words)
FIFO status:
  EMPTY
  ALMOST EMPTY (1 word in FIFO)
INFO: Configured 2017-04-05 11:40:59.174
QObject::connect: Cannot queue arguments of type 'QVector<int>'
(Make sure 'QVector<int>' is registered using qRegisterMetaType().)
QObject::connect: Cannot queue arguments of type 'QVector<int>'
(Make sure 'QVector<int>' is registered using qRegisterMetaType().)
```

type	name	state	connection
Producer	newTLU	OK	tcp://127.0.0.1:43248



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- DESY, October 2017
  - Interfaced AIDA-2020 TLU with Mimosa telescope
    - Used EUDET (trigger/busy/trigger-number) hand-shake
  - Successfully took data with telescope
    - Demonstrated backwards compatibility with EUDET TLU





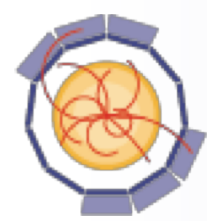
# AIDA<sup>2020</sup> Tests

- CERN, PS (East Area) T9, November 2017
  - Interfaced AIDA-2020 TLU with
    - Mimosa telescope ( EUDET handshake )
    - FE-I4 fast pixel plane ( EUDET handshake )
      - Thanks to Andre Rumler
    - “TORCH” project ( AIDA / Synchronous handshake )
      - AIDA/Synchronous handshake
  - Successfully took data with telescope, FE-I4 and TORCH
  - TLUProducer took data
    - Records time-stamp of each trigger issued ( 25ns )
    - Records fine-grained time-stamp of each trigger input
    - Records which inputs fired ( trigger mask may not demand all inputs fire)
      - Some inputs connected to Cherenkov detectors.

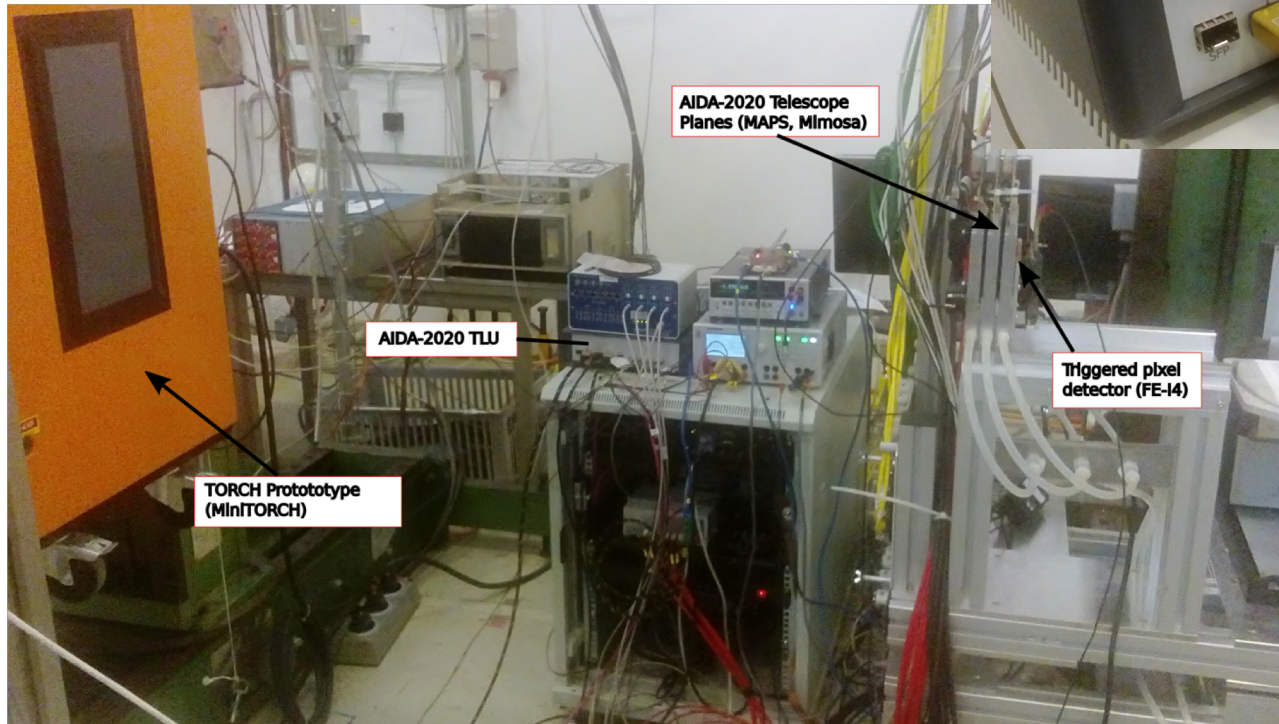


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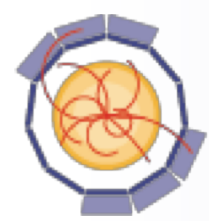




- Used to provide clock and trigger to non-AIDA2020 beam-test readout ( TORCH)



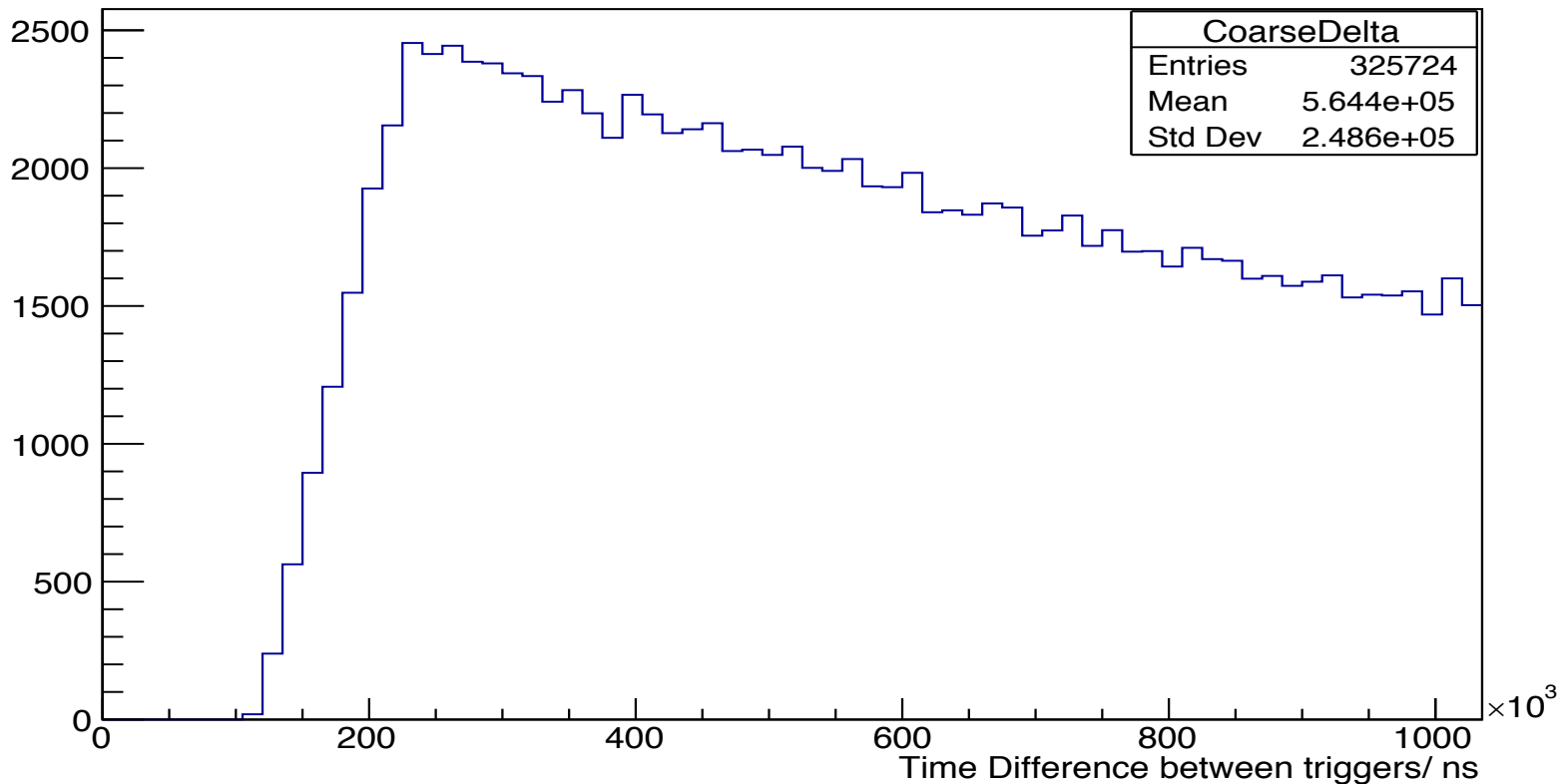
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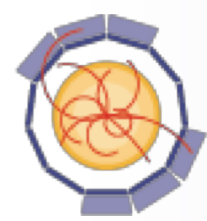


# Difference between timestamps

- Mimosa telescope sets busy until two frames read out (minimum time  $115\mu\text{s}$ , max  $230\mu\text{s}$ )
- ... this is what we are trying to avoid with “mixed mode”

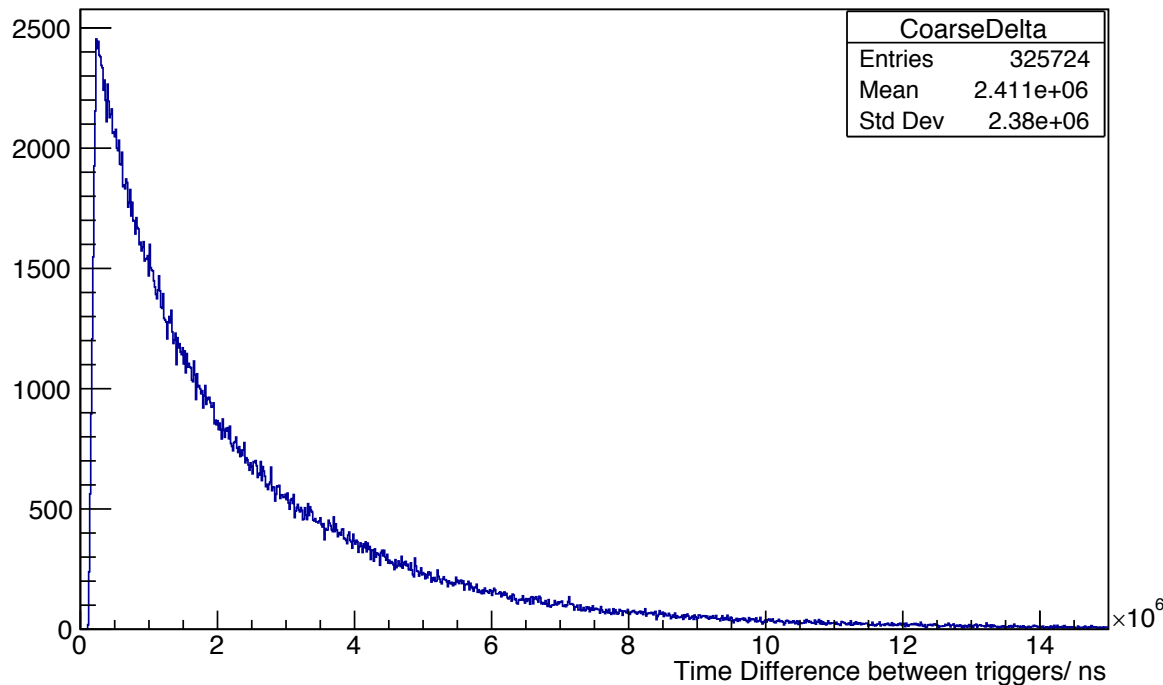
Difference in trigger timestamps





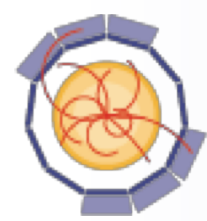
- Telescope scintillators in coincidence with downstream timing detector
- Low trigger-rate
  - Most frames contain a particle, few point to timing detector
- Not quite exponential – gap between spills gives high side tail

Difference in trigger timestamps



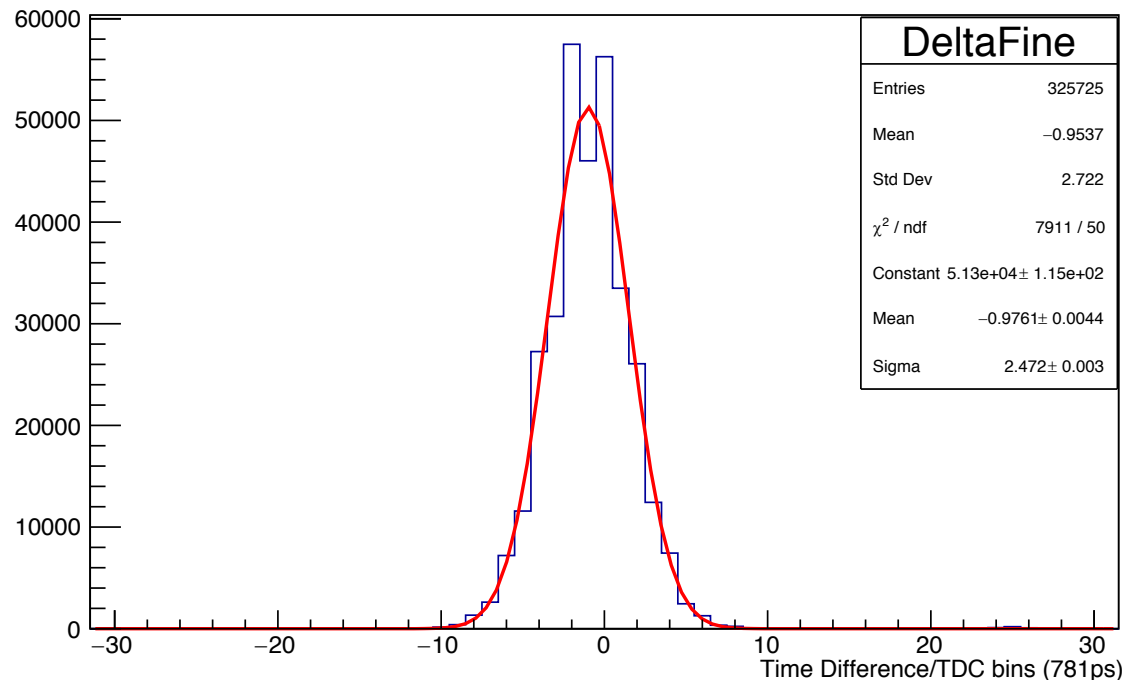
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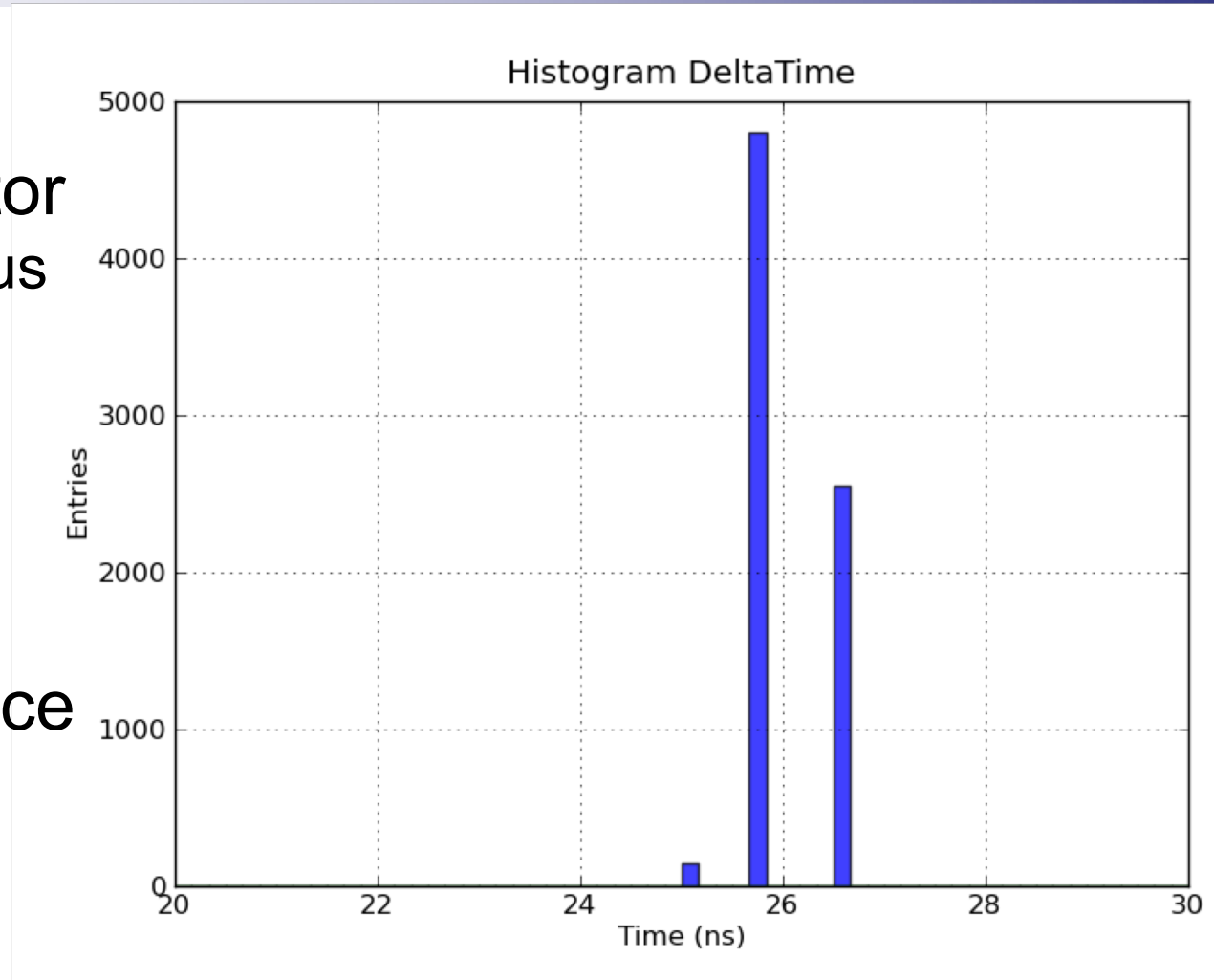


- TLU time-stamps triggers with 1.56ns bins
  - Will be changed to 781ps in later firmware
- Take difference between pulses from two trigger scintillators
  - Telescope scintillators, CERN East Area T9
- Assume errors in quadrature  $\rightarrow$  precision of single scintillator = 1.5ns

Difference in Scintillator Fine Timestamps

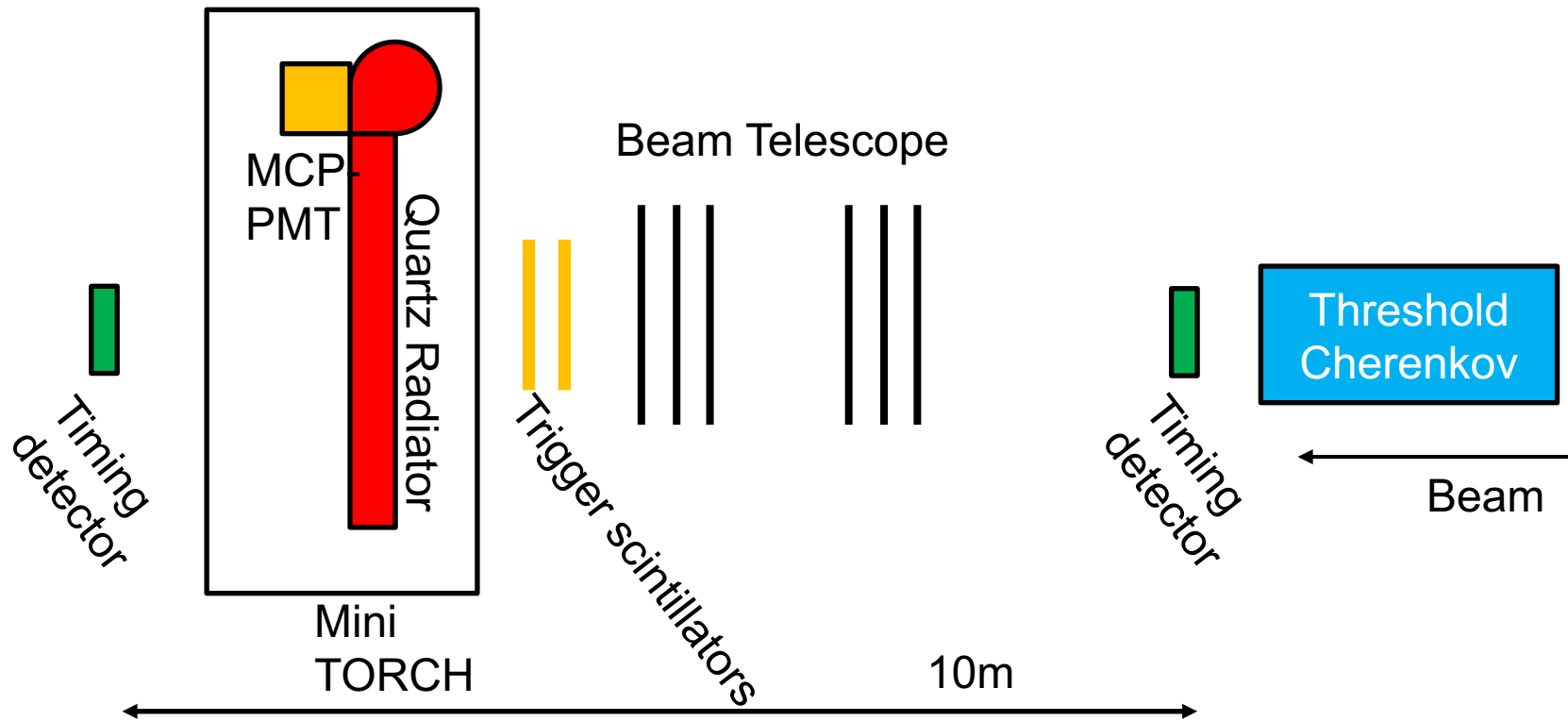


- Signal from pulse generator
  - Asynchronous from TLU clock.
- Feed into two channels with time offset
- Time difference as expected



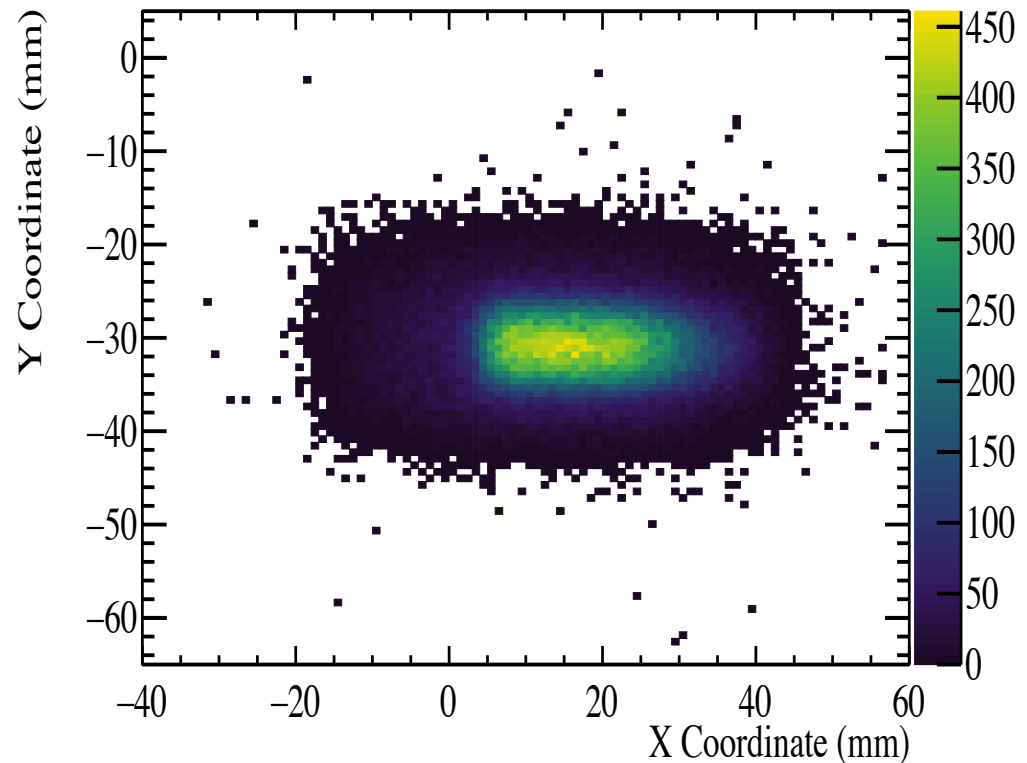
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- TORCH project doing R&D on particle PID by ToF
  - Cherenov light in thin quartz sheet perpendicular to beam
  - Guided by TIR to edges.
  - Read out by pixelated Micro-Channel Plate based PMTs



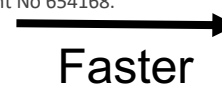
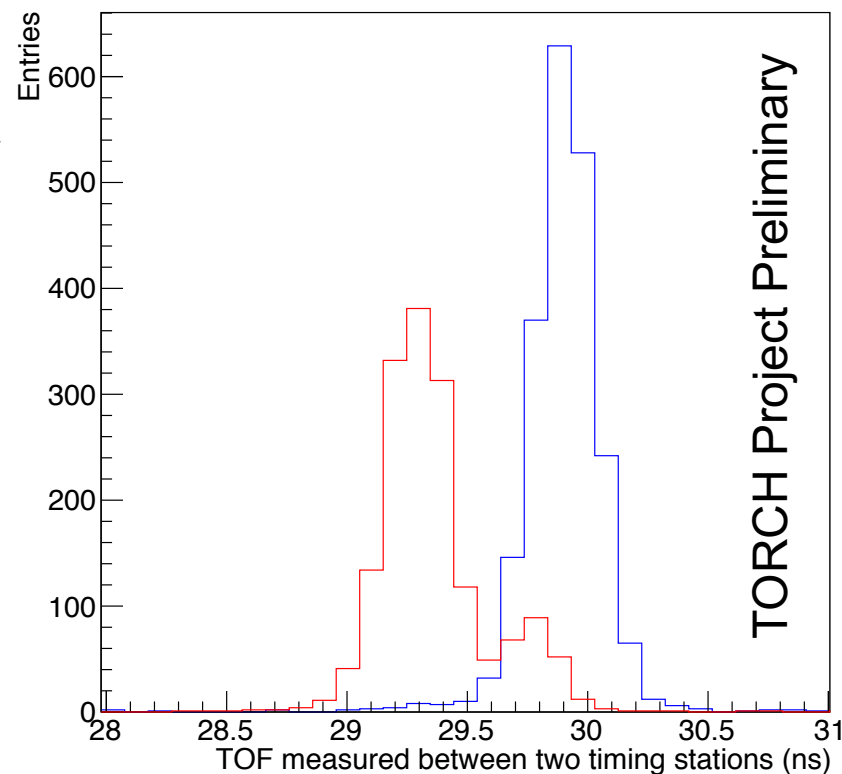
See , e.g.  
<https://doi.org/10.1016/j.nima.2018.10.099>  
<https://doi.org/10.1016/j.nima.2018.12.007>

- Reconstruct data from Mimosa telescope with EU Telescope
- Select events with only one track
  - Average of  $\sim 1.5$  tracks per event
- Extrapolate from telescope to position of timing detector
- See outline of timing detector
- See talk on East Area

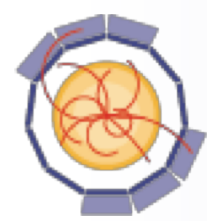


- Aiming to measure single photons with a precision of  $\sigma \sim 70\text{ps}$ 
  - $\rightarrow$  Need to know impact point of particle to  $O(\text{mm})$
- For some analysis want to know particle type ( $p/\pi$ )
  - Time of flight measured by small dedicated detectors
  - Threshold Cherenkov detectors in beam
    - Get signal for  $\pi$ , but not for protons
    - Fed into TLU. Tag event by event
  - Compare ToF with/without Cherenkov tag:

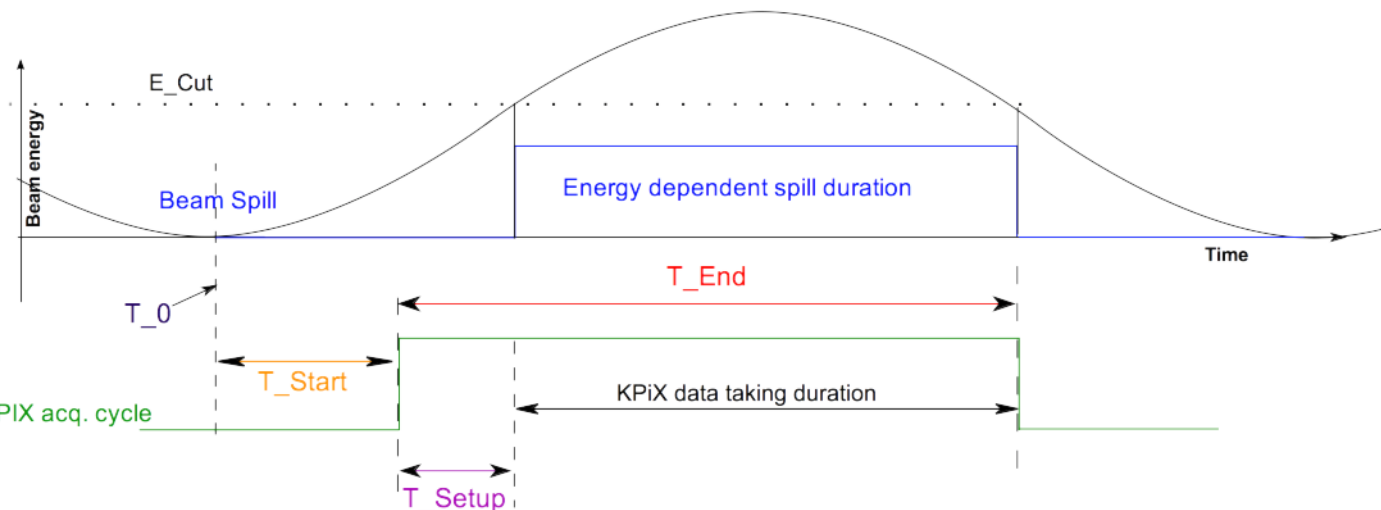
Blue – light in Cherenkov  
Red – no light in Cherenkov

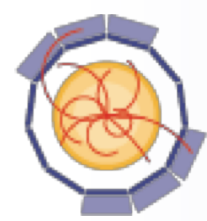






- Readout chip designed for ILC
  - → Short active time, then readout
  - More details [here](#)
- To reduce dead-time, take data only when particles are present
  - Sinusoidal energy ramp in DESY accelerator.
    - Get particles in beam-line only at peak energy of accelerator





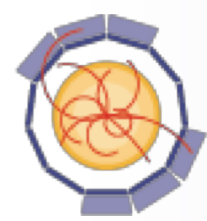
# AIDA<sup>2020</sup>

# Interface to Accelerator

- Provide a “spill” signal to AIDA-2020 Silicon strip tracker (SiTra)
  - See [The LYCORIS Telescope at the DESY II Test Beam Facility](#)
  - Use one of TLU inputs to monitor accelerator signal.
  - Parameters adjustable by setting registers.
  - Could be used at CERN PS/SPS
    - Use WWE , WE, EE
  - Could be used with Calorimeter readout systems
- Firmware tested in lab.

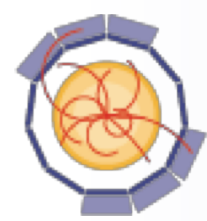


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- Can configure TLU to ignore BUSY from an DUT with EUDET handshake
- E.g. Mimosa telescope + FE-4I:
  - Ignore busy from telescope
  - → Can have more than one trigger sent to FE-14 during frame readout of Mimosa
  - Keep global trigger number (Same trigger number sent out to both Mimosa + FE-14)
  - Whether DUT BUSY vetoes triggers is configurable.
    - For DUT where BUSY vetoes triggers, read out consecutive trigger numbers
    - For DUT where BUSY does not veto triggers, read out non-consecutive trigger numbers ( if >1 particle per frame)
  - Firmware tested in lab
  - Tested at DESY
    - See [Status of the EUDET-type beam telescope infrastructure](#)





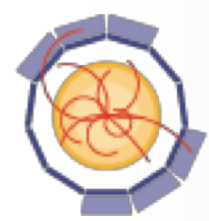
# AIDA<sup>2020</sup>

## Summary

- Two batches “production” AIDA-2020 TLUs have been assembled
  - Contact [David.Cussans@Bristol.ac.uk](mailto:David.Cussans@Bristol.ac.uk) for further requests
- Have tested with Mimosa Telescope and FEI-4
- Have tested simultaneous use of trigger/busy(EUDET) and synchronous(AIDA) interface
- Firmware in place to allow multiple triggers per Mimosa telescope frame
  - Tested in lab
  - Tested at DESY – Mimosa + FE-I4
  - Order(s) of magnitude higher trigger rate from AIDA beam telescopes
- Have tested simultaneous use of trigger/busy(EUDET) and synchronous(AIDA) interface
  - ( Mimosa telescope + FE-I4 ) + TORCH
  - Allows interface beam telescope with CALICE calorimeter.
- Firmware written to interface with DESY accelerator
  - Programmable “spill” signal
  - allow interface with AIDA-2020 Silicon tracker.



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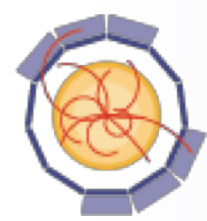
# Backup Slides

- Backup Slides



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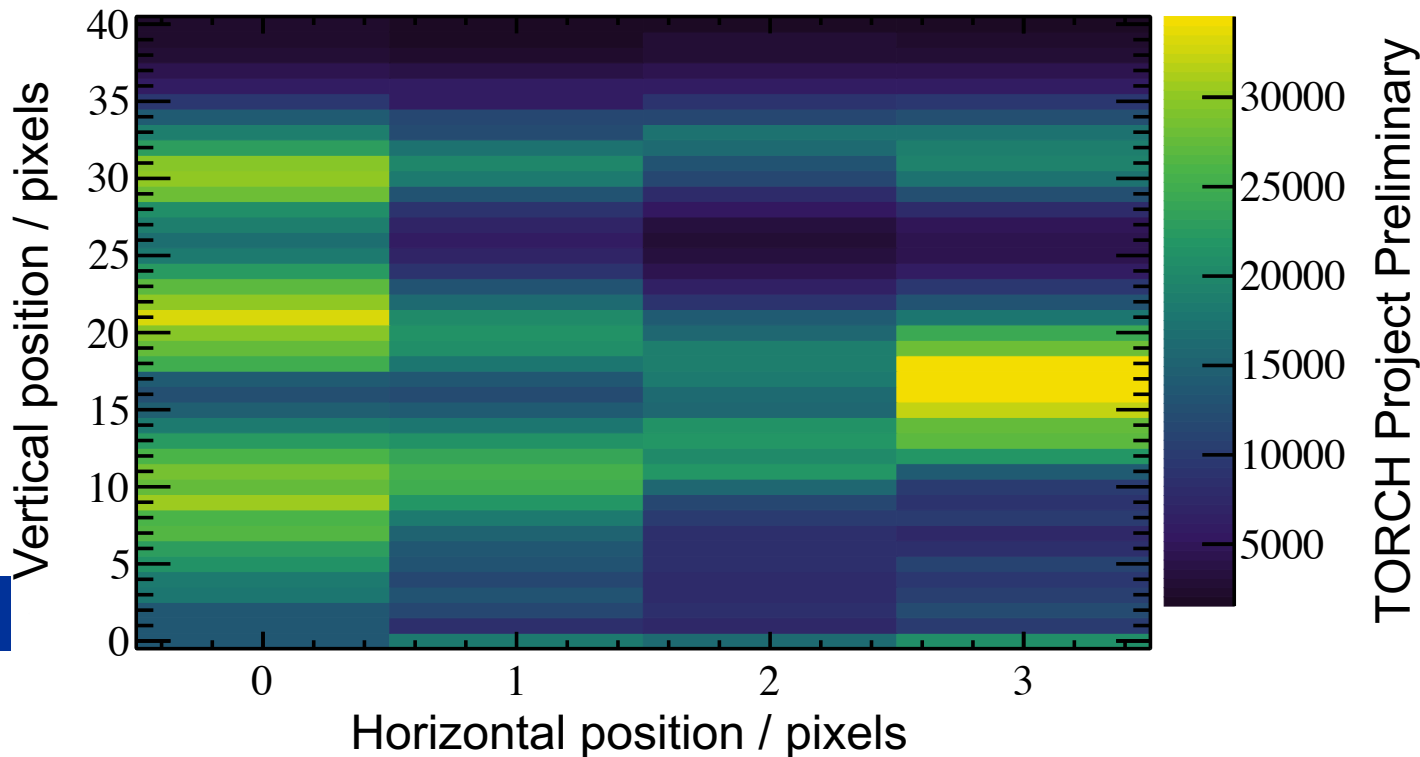


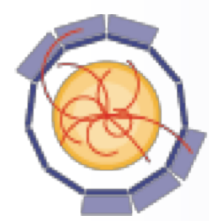


# AIDA<sup>2020</sup>

# TORCH

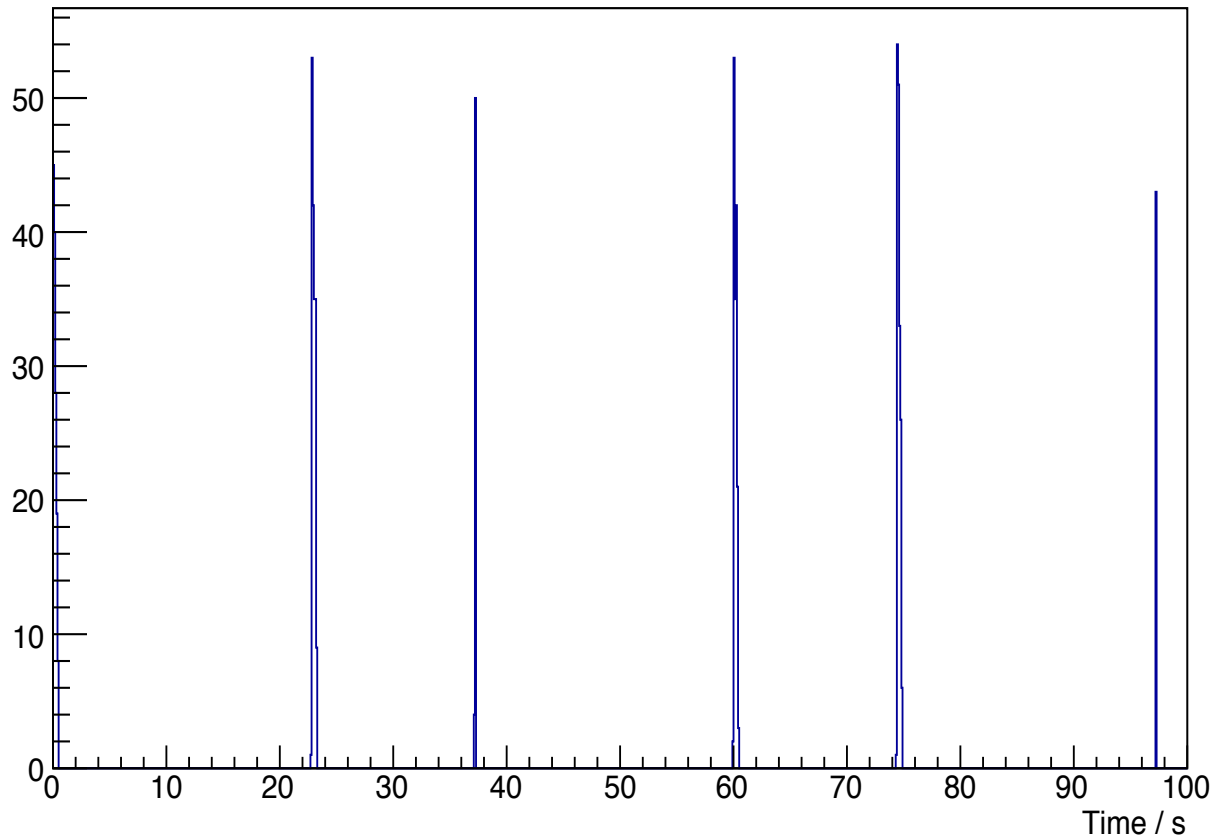
Cone of Cherenkov photons trapped by TIR, guided to end of quartz sheet and focused on to MCP-PMT  
Projection of cone folded by reflection at edges





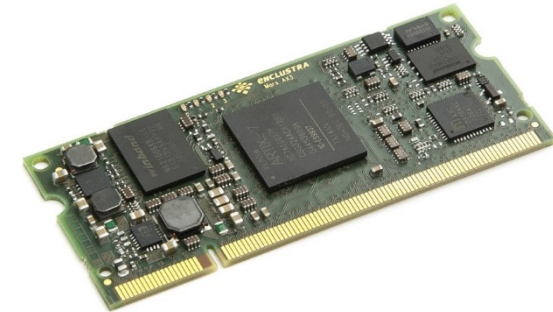
- Trigger time-stamps of first few spills in a run

Trigger times



- Transition from FPGA Xilinx Series 6 (miniTLU) to Series 7 (v1C and later)

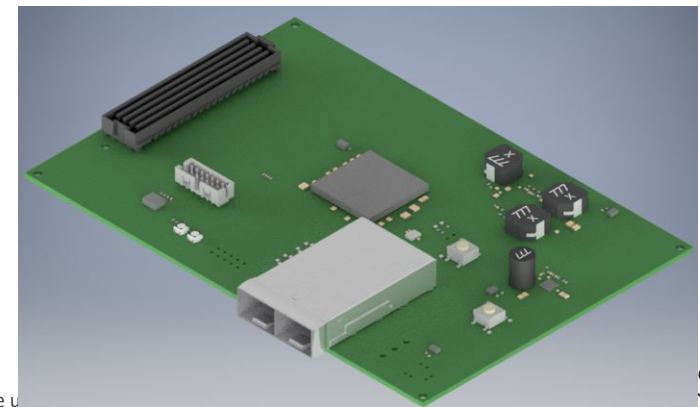
- Currently working on bench with Enclustra AX3 FPGA



- **ARTIX TRIVIAL FMC CARRIER (ATFC)**

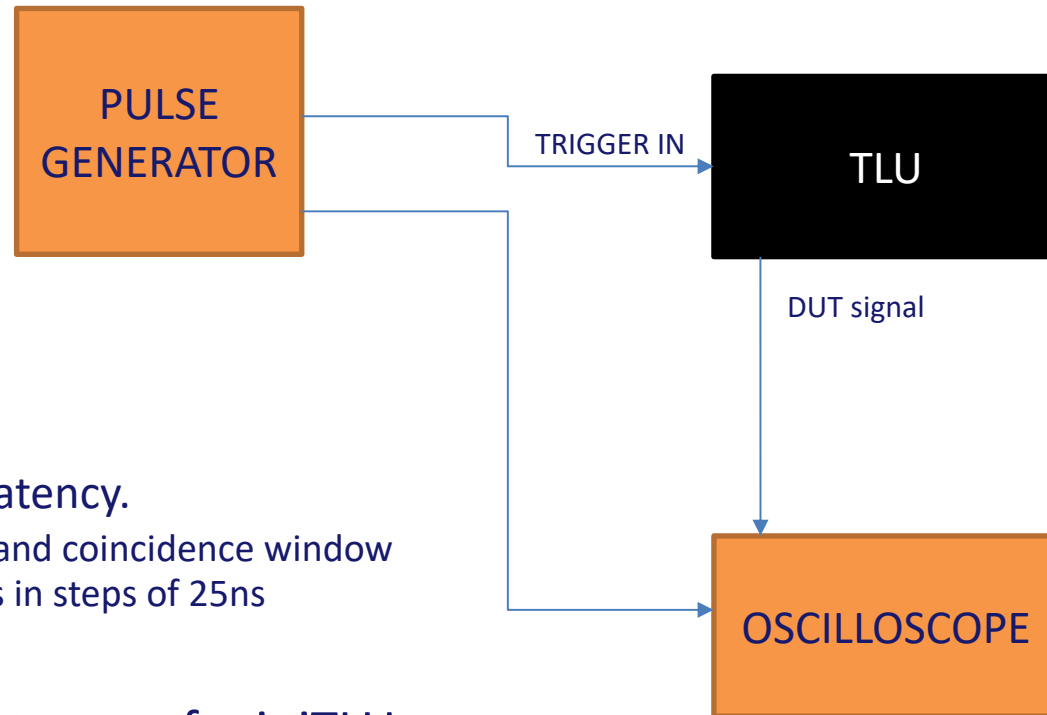
[HTTP://WWW.OHWR.ORG/PROJECTS/ATFC](http://www.ohwr.org/projects/atfc)

- Designed by Samer Al-Kilani (UCL)
- Stand-alone
  - ... but design will eventually be included in TLU
- Bare PCBs produced
- Waiting for components,
  - Then assembly of first two at UCL



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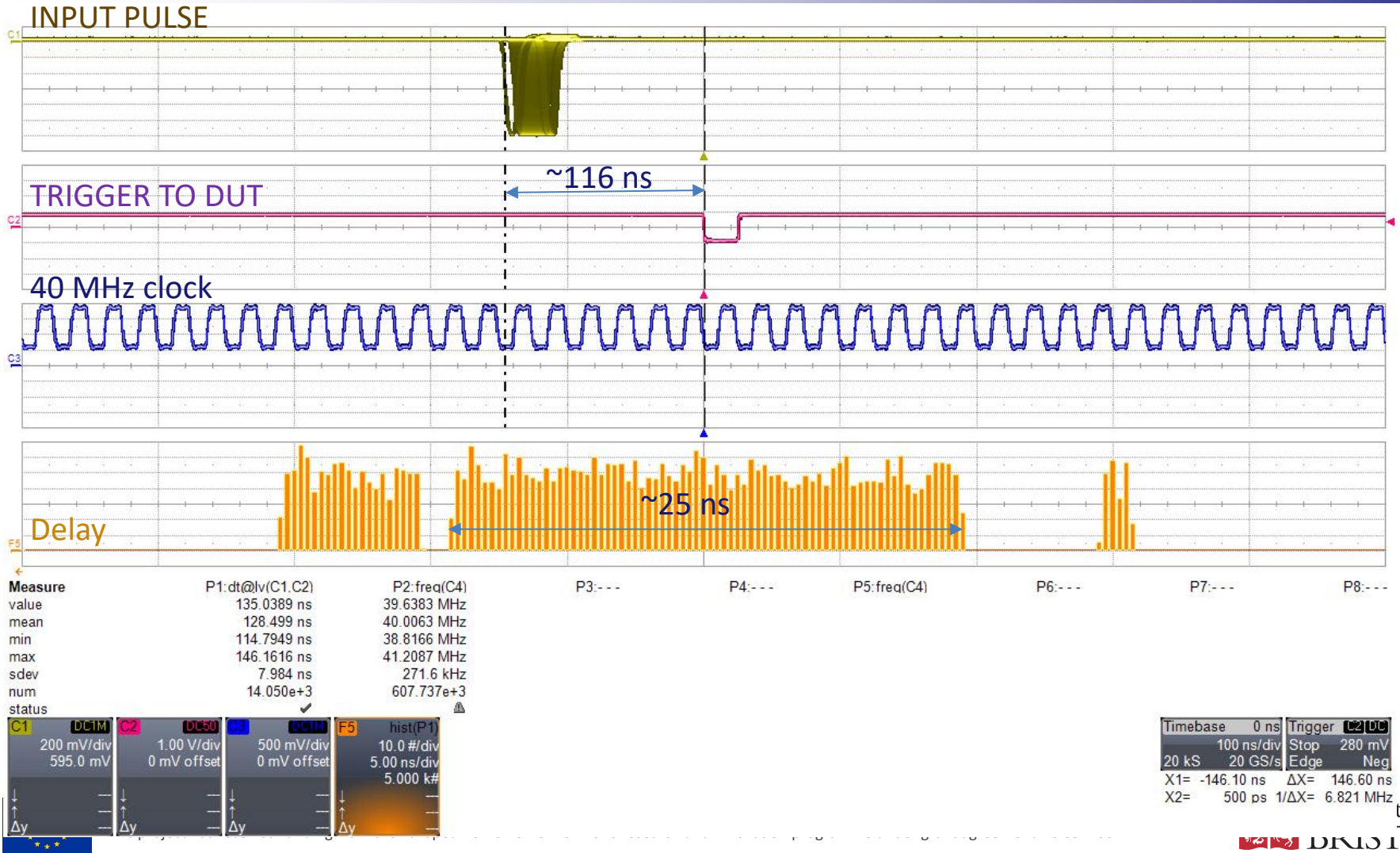
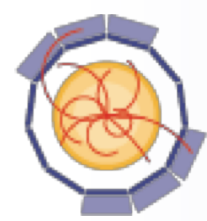


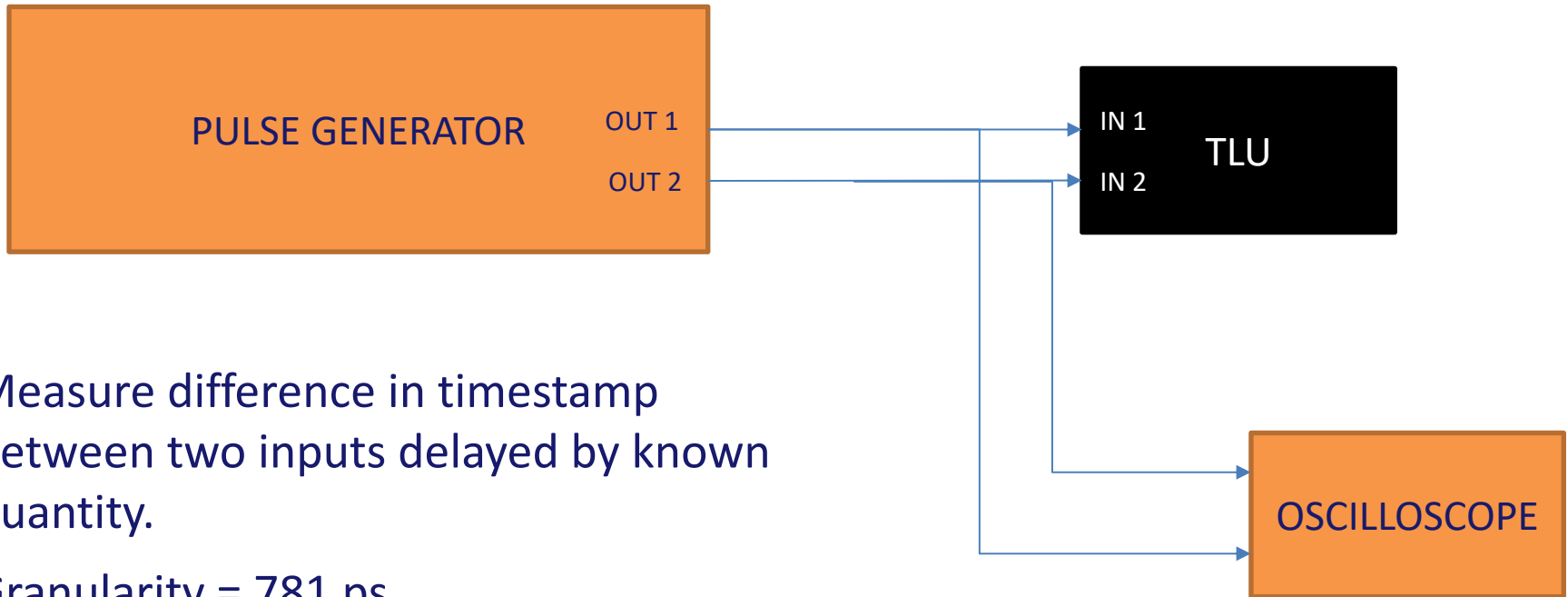


- Testing TLU latency
  - Measuring minimum latency.
    - Latency of each input and coincidence window adjustable up to 400ns in steps of 25ns
- Current firmware direct port of miniTLU
  - Includes multiple registers to suppress meta-stability
  - Not yet optimized to reduce latency



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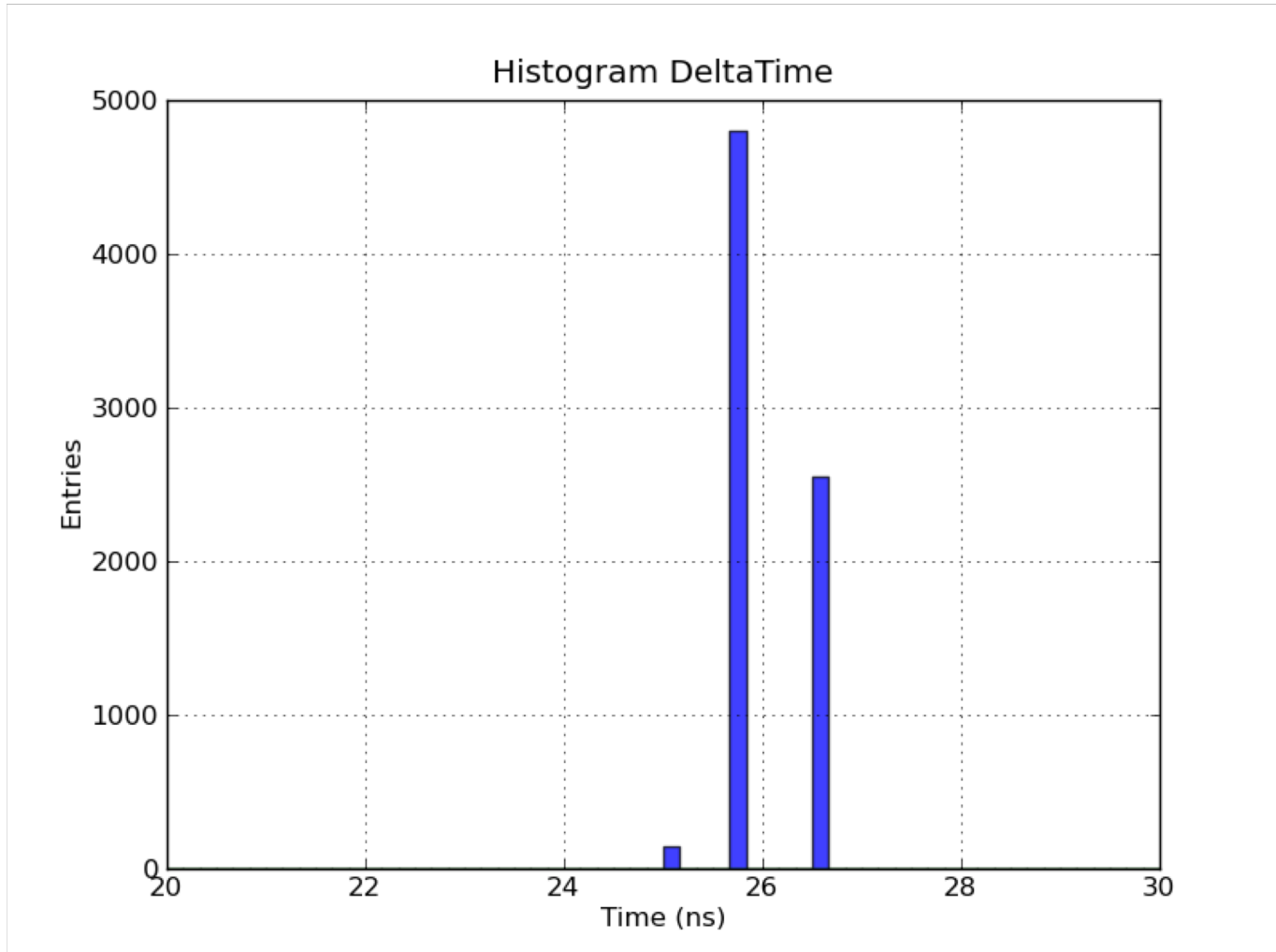




- Measure difference in timestamp between two inputs delayed by known quantity.
- Granularity = 781 ps
- Work in progress



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