Test Beam Studies for the ATLAS Tile Calorimeter Upgrade Readout Electronics

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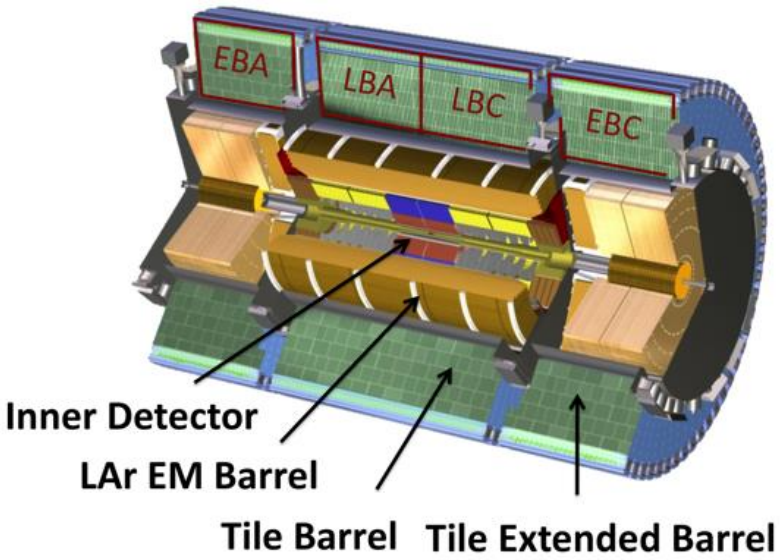
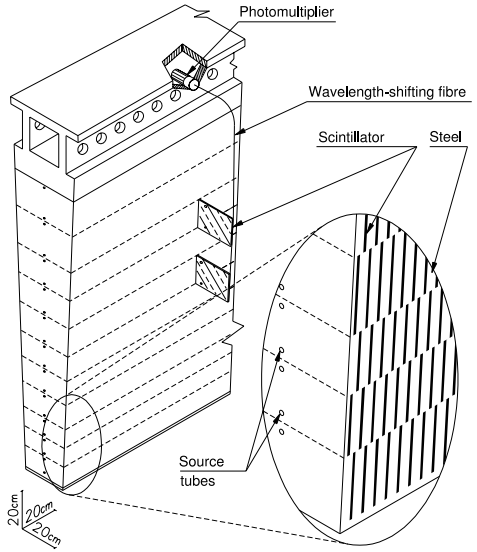
On behalf of the TileCal Upgrade group

ATLAS Tile Calorimeter

- Measures energies of hadrons, jets, τ-leptons and E_T^{miss}
- Segmented calorimeter of steel plates and plastic scintillator tiles which covers the most central region of the ATLAS experiment (up to $|\eta| = 1.7$)
- 4 partitions: EBA, LBA, LBC, EBC
- Each partition has 64 modules
  - One drawer hosts up to 48 PMTs

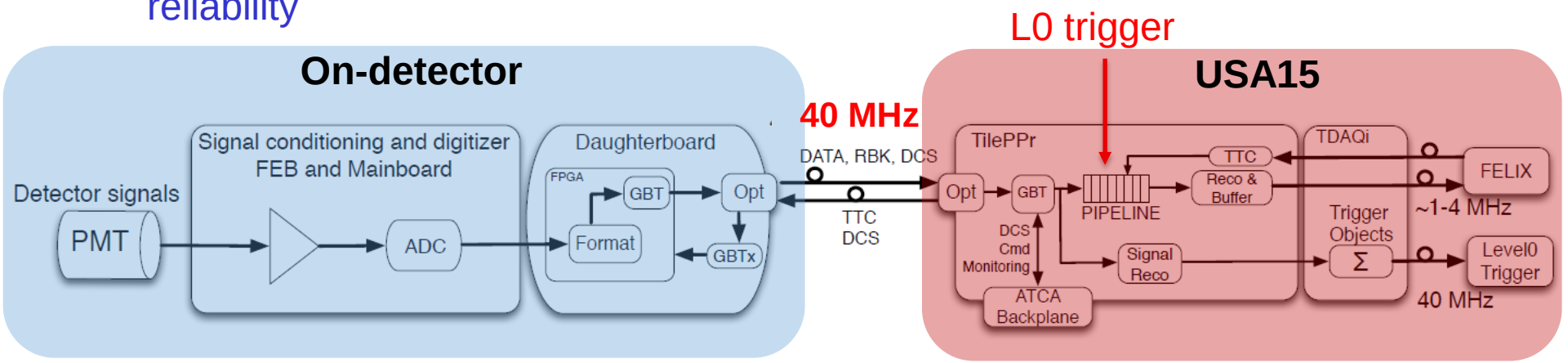




- Light produced by a charged particle passing through a plastic scintillating tile is transmitted to the PMTs
- Scintillator tiles are read out using wavelength shifting fibers coupled to PhotoMultiplier Tubes (PMTs)
- Around 10,000 readout channels

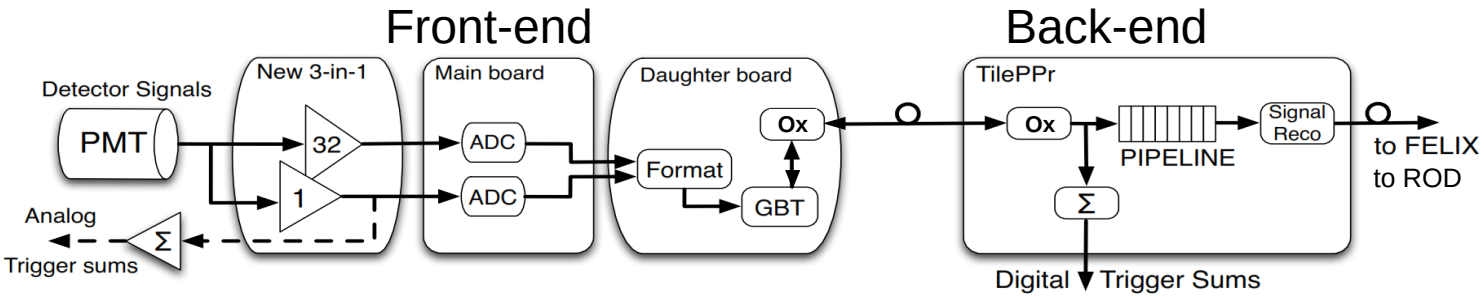
TileCal Phase II Upgrade

- **Complete replacement of on-detector and off-detector readout electronics (2024-2026) for the High Luminosity-LHC (HL-LHC)**
  - Aging of electronics due to time and radiation
  - Current readout architecture is not compatible with the fully digital TDAQ architecture and requirements for Phase II Upgrade
- **New readout strategy for HL-LHC**
  - On-detector electronics will transmit digitized data to the off-electronics at the LHC frequency (40 MHz) → 40 Tbps to read out the entire detector!
  - Buffer pipelines are moved to off-detector electronics
  - Redundancy in data links and power distribution → improvement in the system reliability



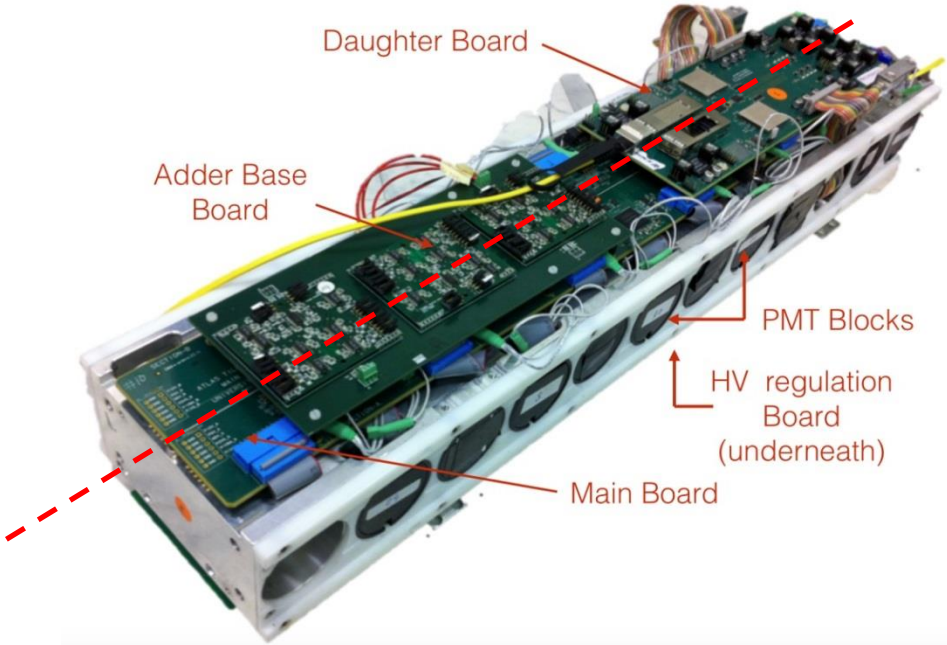
Demonstrator project and plans

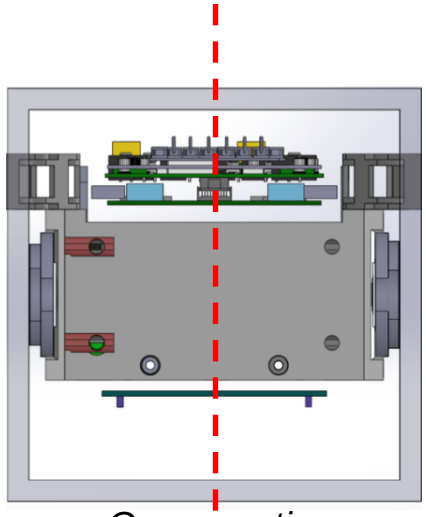
- Evaluation the new readout schema and trigger system interfaces
- Plans for the Demonstrator project
  - Seven test beams from 2015 and 2018
  - **Insertion of Demonstrator module into the ATLAS detector this Spring**
  - Operate during the Long Shutdown 2 and after undergo evaluation for Run3
- Readout architecture for HL-LHC keeping backward compatibility with the legacy system
  - Back-end electronics (PreProcessors) receive digitized data at 40 MHz + distributes the sampling clock to the detector
  - PreProcessors will send triggered events to the legacy Read Out Drivers (RODs) and to the **F**ront **E**nd **LI**nk e**X**change (FELIX)
  - Provide analog trigger signals to the current ATLAS trigger system



Demonstrator module

- The **Demonstrator module** is composed of 4 mini-drawers (48 PMTs). Each mini-drawer have 2 independent read out sections **for redundant cell readout**
  - 12 PMTs + 12 front-end boards reading out 6 TileCal cells
  - 1 × MainBoard: operation of the front-end boards
  - 1 × DaughterBoard: data high speed link with the back-end electronics
  - 1 × High Voltage regulation board: Remote or Internal options
  - 1 × Adder base board + 3 adder cards: trigger analog signals
  - 1 × Low Voltage Power Supply (LVPS): low voltage power distribution

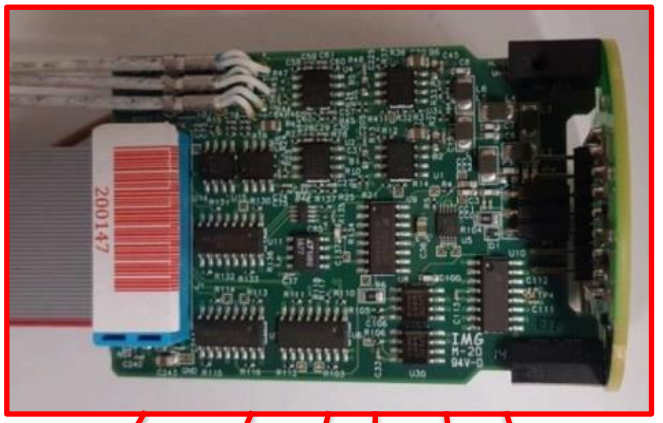




Cross section

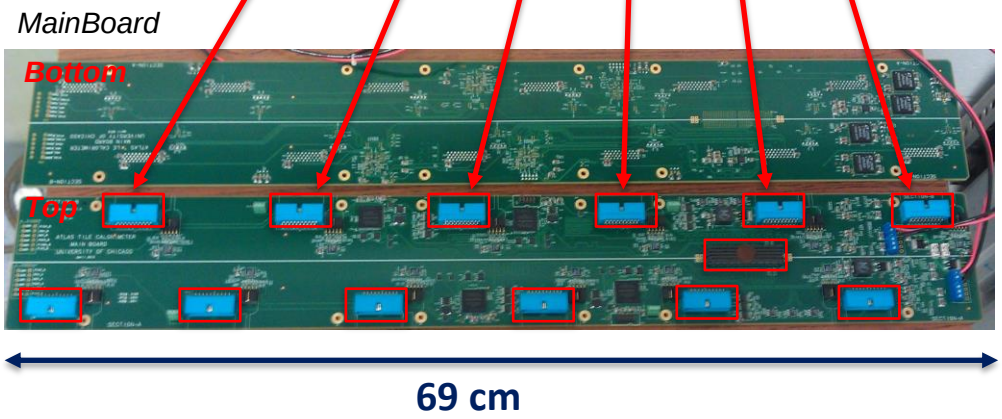
Front-End Boards and MainBoard

- **Front-end boards:** Upgraded 3in1 cards
  - **PMT pulse shaping**
  - Shaper with bi-gain output : 2 × LG + 1 × HG
  - Improved noise and linearity
  - Improved calibration circuitry
  - Final version: FENICS cards tested during the last testbeam (November 2018)



FENICS cards

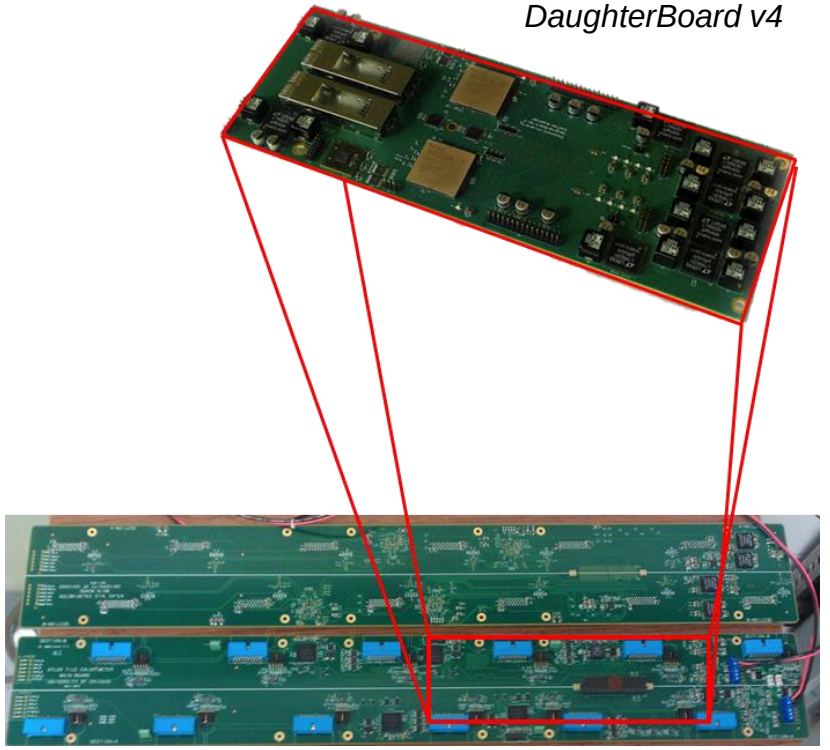
- **MainBoard**
  - **Digitize analog signals coming from 12 FEBs**
  - Routes the digitized data from the ADCs to the DaughterBoards
  - Digital control of the FEBs
  - HG and LG, 12-bit samples @40 Msps
  - TID, NIEL, SEE tests performed



DaughterBoard

- **High-speed link with the back-end electronics**
  - Data collection and transmission
  - Clock and command distribution
  - Data link redundancy
- Daughterboard version 4
  - 2 × Xilinx Kintex 7 FPGAs
  - 2 × QSFP modules (~40 Gbps each)
  - 2 × GigaBit Transceiver (GBT) chips
- **New version 5 being qualified**
- TID tests with ~ 9 MeV electron beam
- SEE and SEL tests done with 58 MeV and 226 MeV proton beam
  - Soft error rate is low → Triple redundancy
  - No destructive effects observed

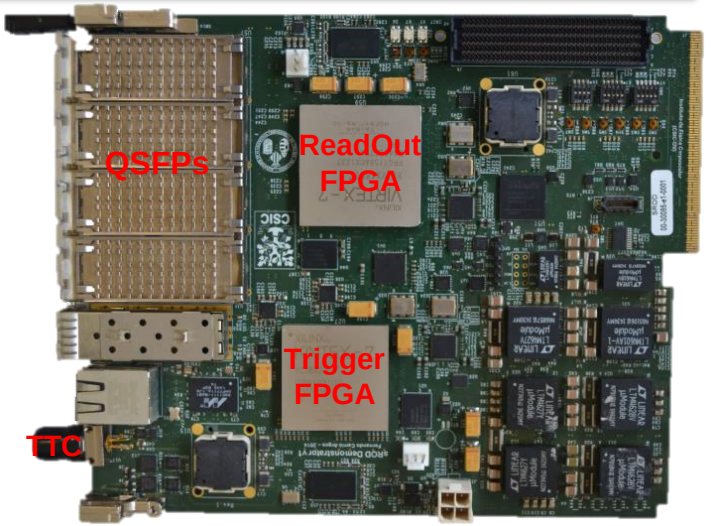
DaughterBoard v4



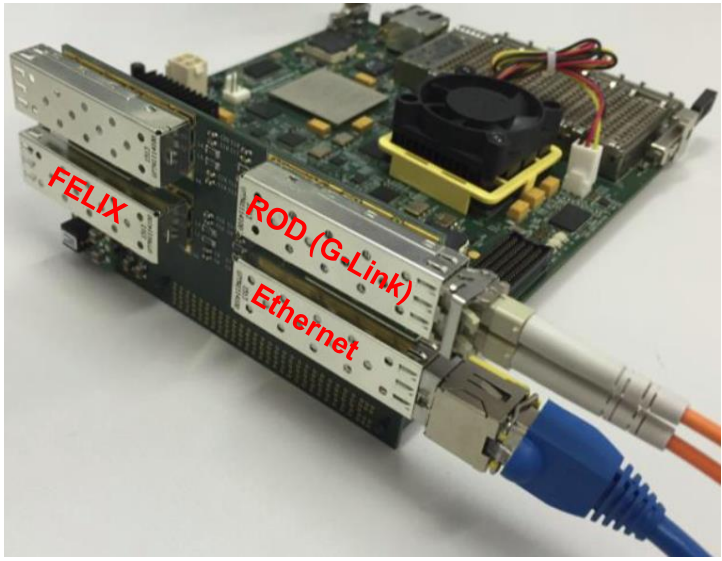
MainBoard

TilePreprocessor Demonstrator

- **First element of the back-end electronics**
  - Data processing and handling from detector
  - Clock distribution towards the modules
  - Detector Control System data distribution
  - Interfaces up to 4 mini-drawers (one module) through the DaughterBoards → **160 Gbps!**
- **Fully functional prototype**
  - Xilinx Virtex 7, Kintex 7, 4 QSFPs
  - Double mid-size AMC (µTCA / ATCA carrier)
  - 1/8th of the full-size PreProcessor for HL-LHC
- Used during the testbeam campaigns to validate the new readout electronics
  - Keeps backward compatibility with the legacy system: TTC system, RODs
  - **Triggered events are transmitted to FELIX system**



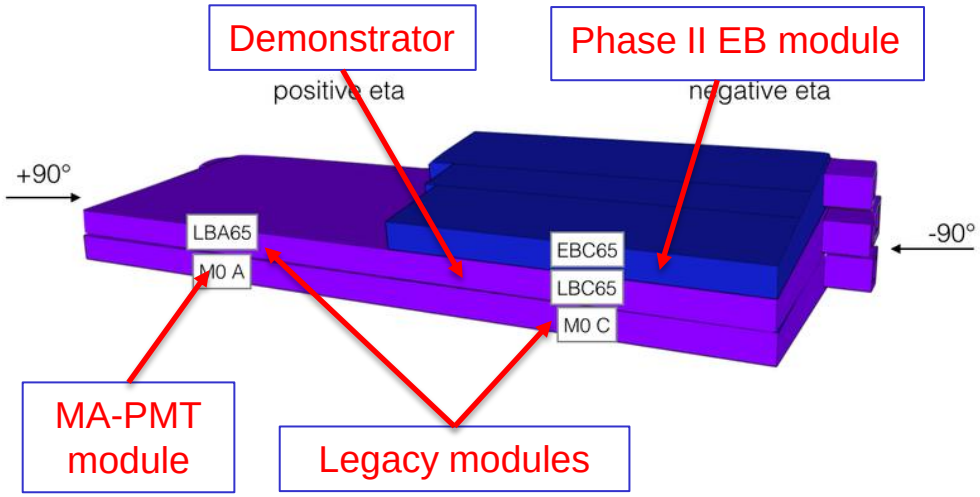
PPr Demonstrator



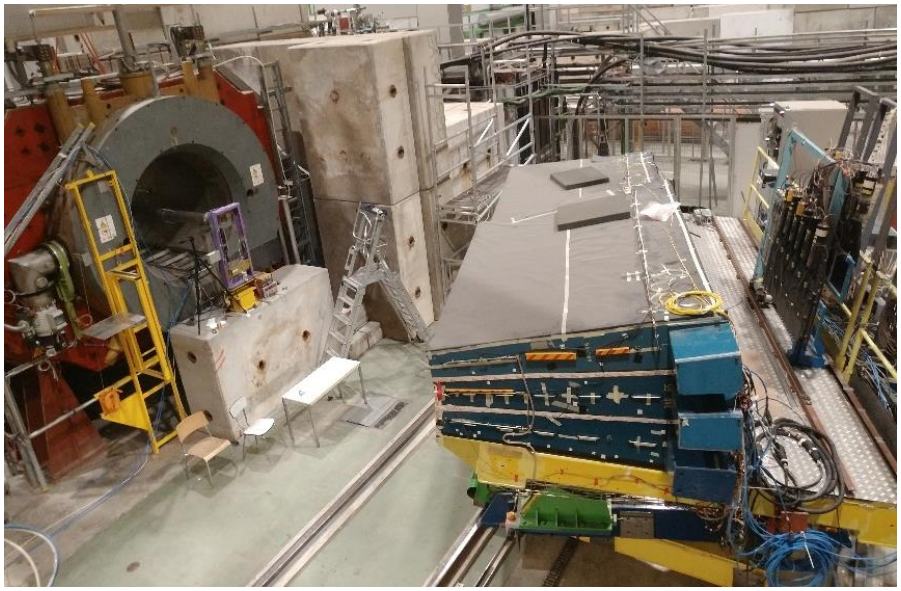
PPr Demonstrator + backplane

Test Beam setup

- Located at the **S**uper **P**roton **S**ynchrotron (SPS) North Area on the H8 beam line
- Three detector modules equipped with legacy and upgraded electronics
  - ½ Long Barrel with the Upgraded 3-in1 cards → **Demonstrator module**
  - 1 Ext. Barrel with the FENICS cards → Phase-II EB module
  - 1 Long Barrel with legacy electronics + ½ Long Barrel with Multi-Anode PMTs

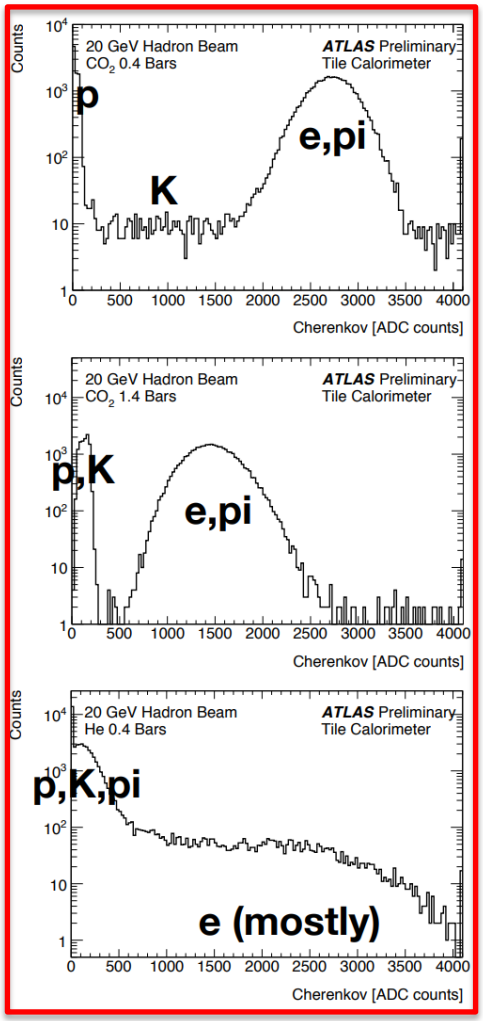


Test beam module configuration (2018)



Test beam setup at H8 line

Beam Line Elements

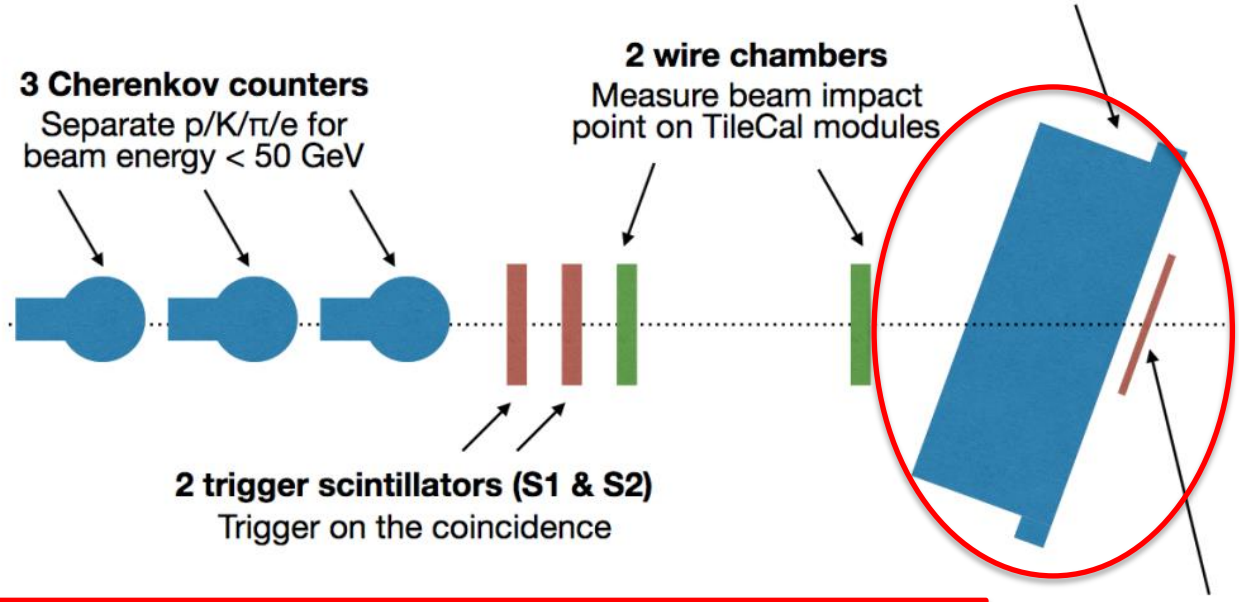


Beams of Hadrons, Electrons and Muons were used to study the calorimeter response

TileCal modules
Legacy electronics;
3-in-1 demonstrator;

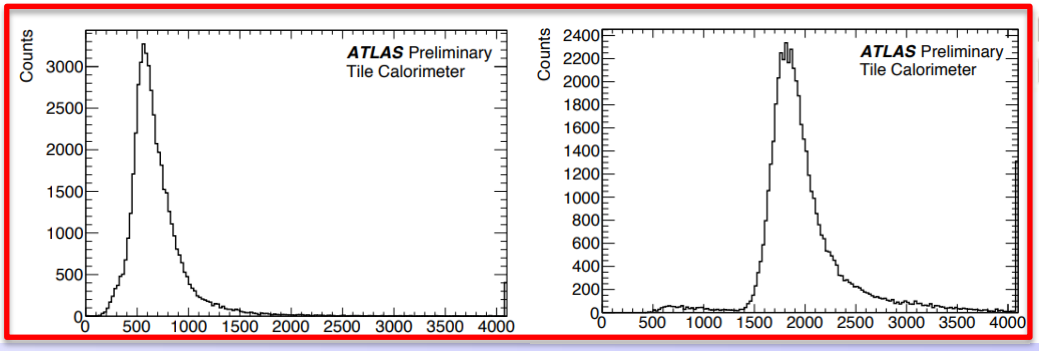
3 Cherenkov counters
Separate p/K/π/e for beam energy < 50 GeV

2 wire chambers
Measure beam impact point on TileCal modules



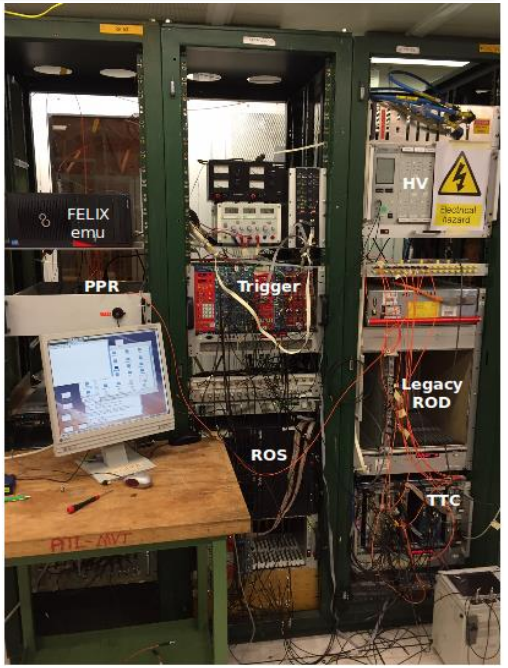
2 trigger scintillators (S1 & S2)
Trigger on the coincidence

Muon hodoscope
Measure the pass-through of muons

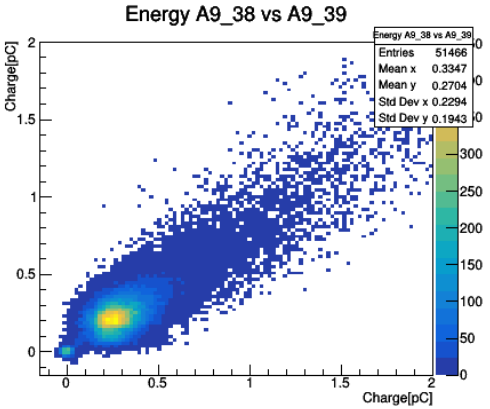


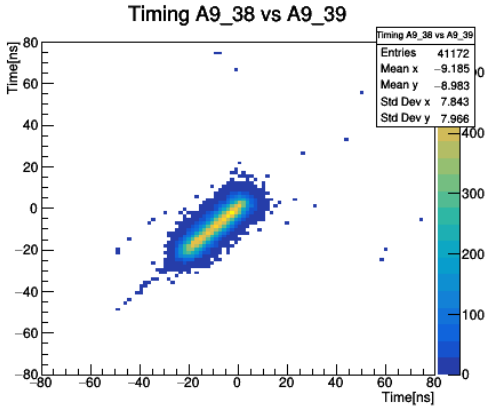
ATLAS TDAQ / DCS Software

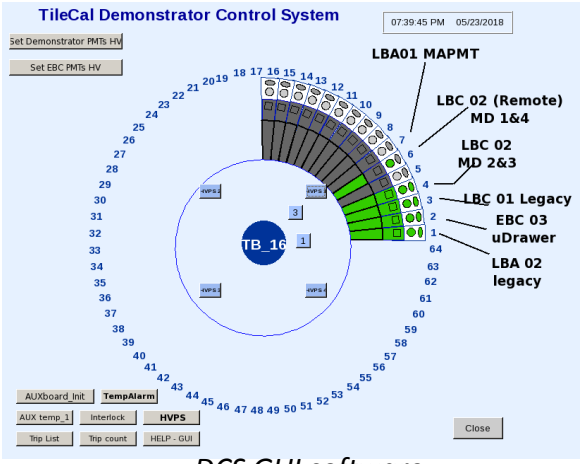
- Fully integrated with the TDAQ software and DCS system
  - Front-end electronics configuration
  - Physics, calibration and laser runs
  - Data taking through FELIX and legacy RODs
  - HV and LV control and monitoring through DCS GUI
- Event Builder stores detector data + beam element data
  - ATLAS software framework (Athena) to reconstruct the energy and time per cell
- **D**ata **Q**uality **M**onitoring (DQM) display software
  - Online data monitoring for validation during data taking
- Standalone software for data links monitoring and fine timing adjustments



Trigger, TTC and Readout racks

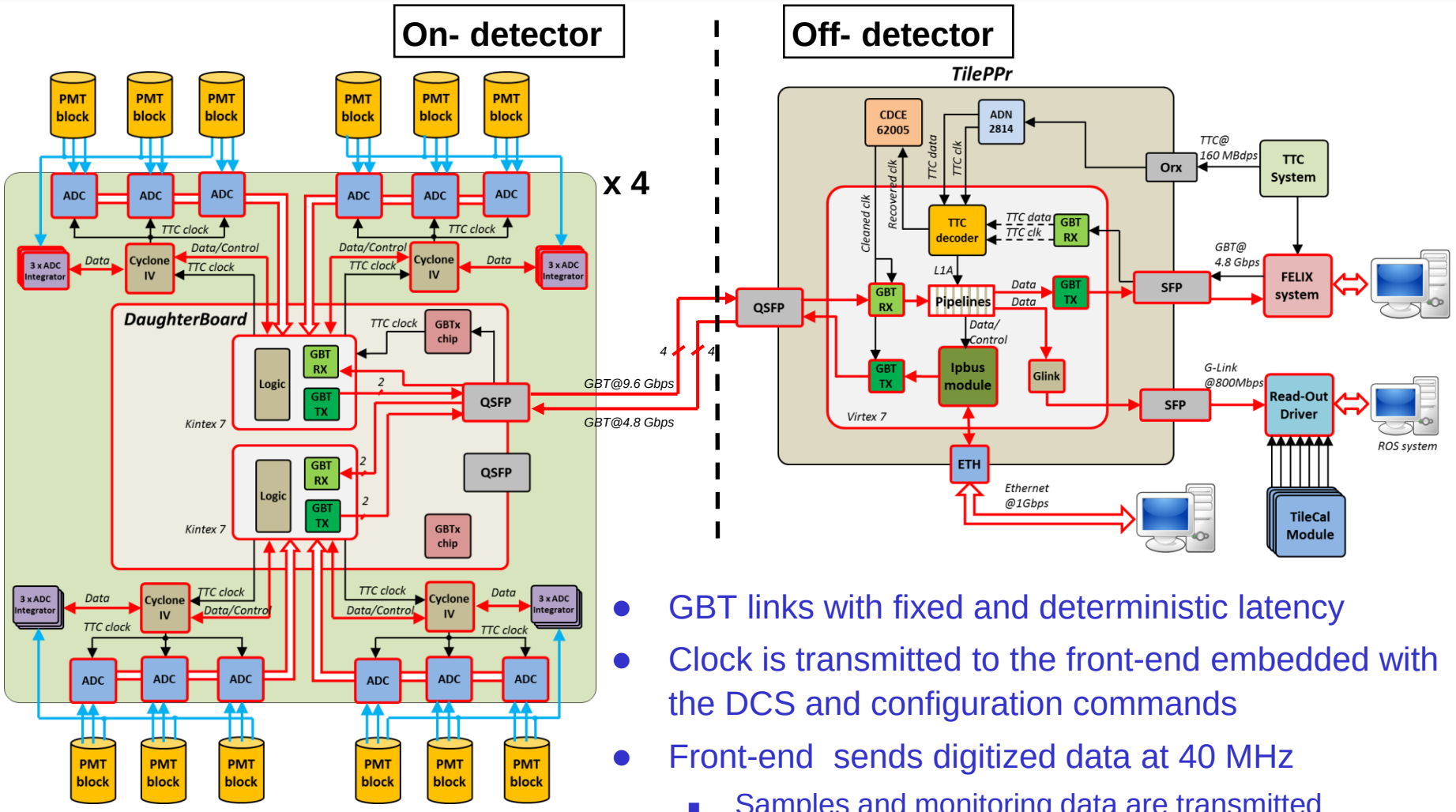






DCS GUI software

Clock and dataflow schema



- GBT links with fixed and deterministic latency
- Clock is transmitted to the front-end embedded with the DCS and configuration commands
- Front-end sends digitized data at 40 MHz
  - Samples and monitoring data are transmitted
- Two independent readout paths:
  - FELIX system / Legacy Read Out Drivers

Summary

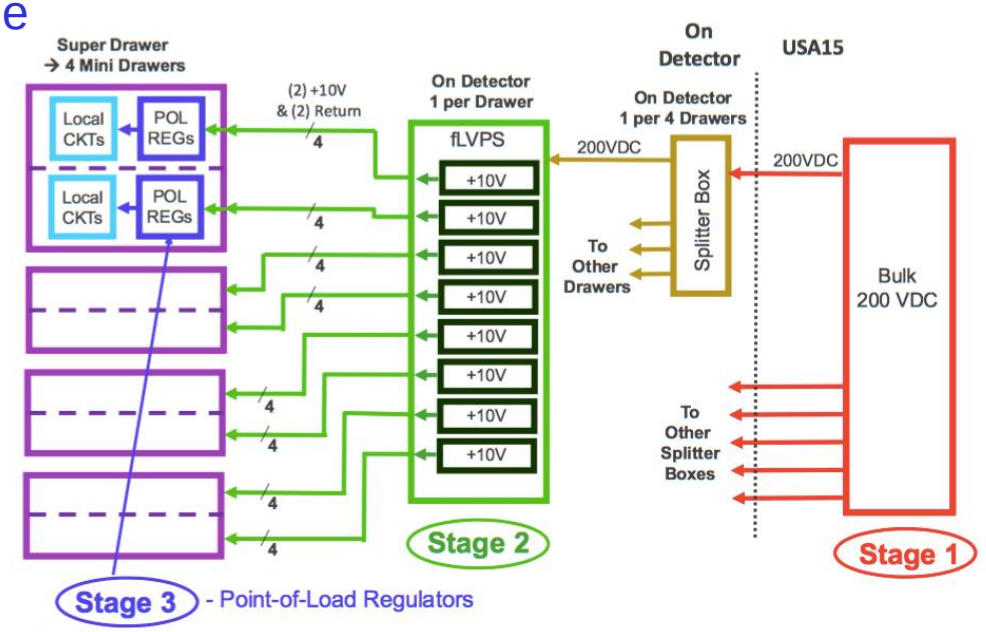
- Complete redesign of the front-end and back-end electronics for Phase II
- Development of readout electronics are progressing very well
  - R&D of prototypes-0 are done
  - New front-end board tested during last testbeam: FENICS cards
  - DaughterBoard v5 being qualified
  - Fully operational PreProcessor Demonstrator prototype
- Seven testbeam campaigns during 2015 and 2018
  - All prototypes extensively tested and showed a good performance
  - Readout electronics implements the clock and data architecture for HL-LHC
- Insertion of the Demonstrator module in the Spring of 2019
  - During the LS2 without affecting the Phase-I upgrade
  - Operate for 1 year until 2020 and after undergo evaluation for Run3
- Some physics results ***in next talk***:
  - *"Studies of the response of the ATLAS Tile Calorimeter to beams of particles at the CERN test beams facility"*

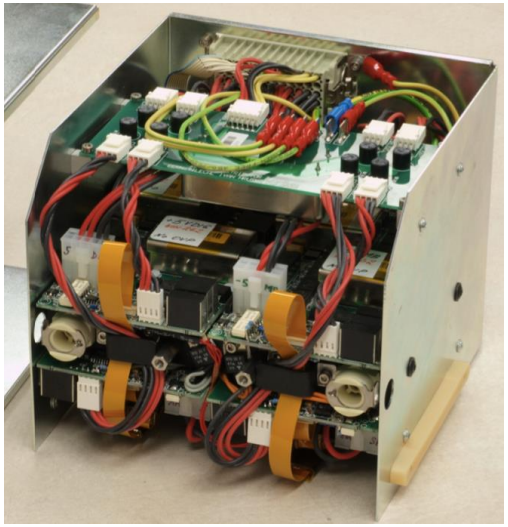

Thank you for you attention!
M0+
DANGER

BACKUP

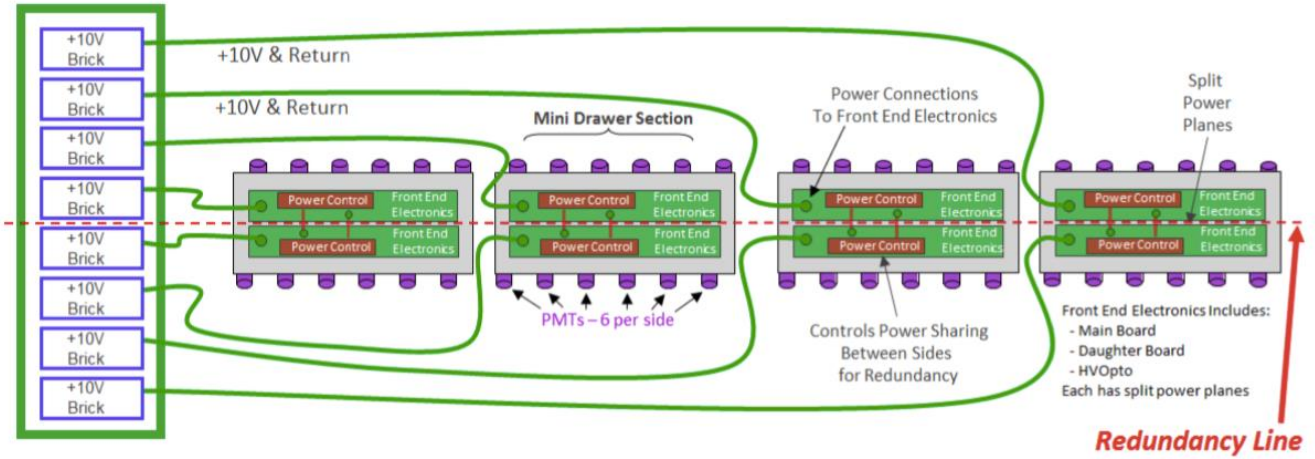
Low Voltage Power Supply

- Three stage power system based on the current LVPS design
- Improvements:
  - Better reliability, lower noise
  - Improved radiation tolerance
  - Number of connections
- **TID radiation tests done**
  - **Still investigating irradiated bricks**
  - **Possible design modification**





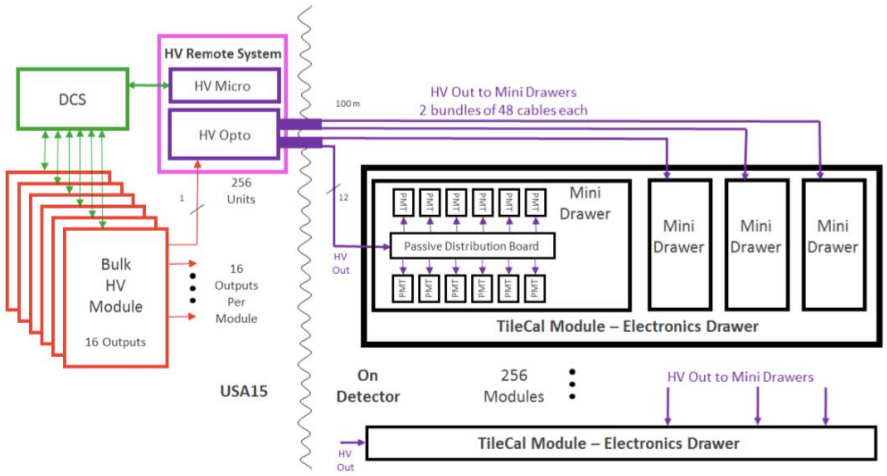
LVPS



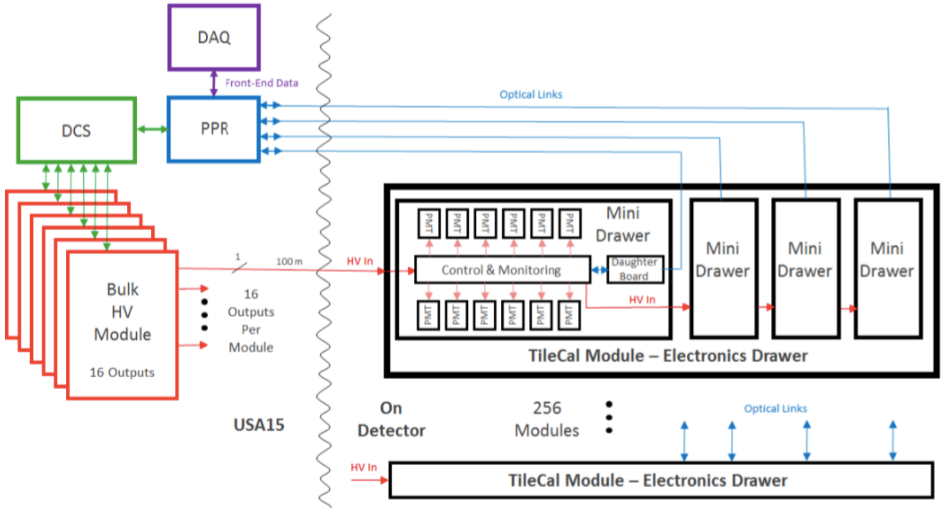
High Voltage distribution

Remote option - Baseline

- High Voltage power supplies and regulators installed in USA15
- **Individual cables per PMT block**
- Advantages: Maintenance, no radiation
- 12-channel version is operational and **used during the testbeam campaigns**



Internal option - Backup



- High Voltage power supplies in USA15 but regulators inside the detector
- **Individual channel control through the DaughterBoard**
- Advantages: Reduced number of cables are required
- Operational and used during the testbeam campaings

TilePPr Demonstrator

TI CDCE62005
- Jitter cleaner

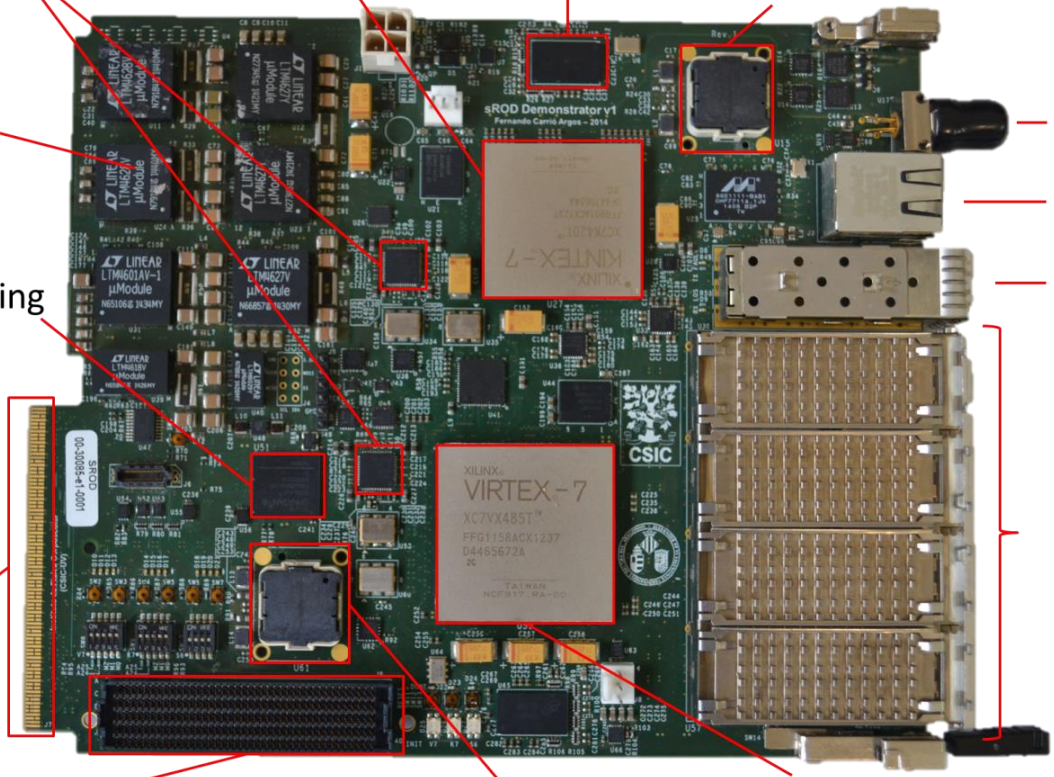
Xilinx Kintex 7
- XC7VX420T

DDR3
512 MB

Avago MiniPOD TX
- Interface with the Level 0 trigger system

Power
modules

Xilinx Spartan 6
- XC6SLX16
- Power monitoring
- Slow control



AMC connector
- 5 GbE ports
- 1 PCIe port
- 4 SerDes ports
- IPMI

4 QSFP modules
- 16 GBT TX @ 4.8 Gbps
- 16 GBT RX @ 9.6 Gbps
- Communication with the front-end electronics

FMC expansion

Avago MiniPOD RX

Xilinx Virtex 7
- XC7VX485T