ATLAS New Small Wheel Micromegas Testbeam System

Christos Bakalis

National Technical University of Athens
Brookhaven National Laboratory

7th Beam Telescopes and Test Beams Workshop

January 14 – 18 2019, CERN

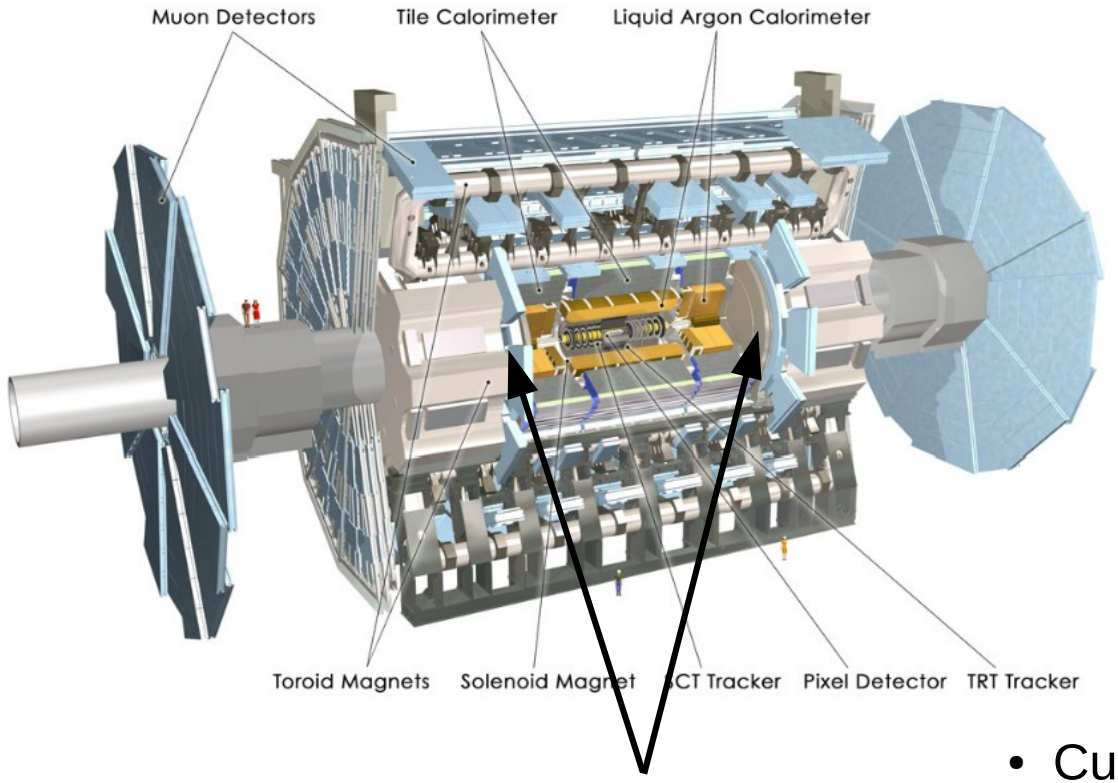
Outline

BROOKHAVEN NATIONAL LABORATORY

- Introduction
- Micromegas in Testbeam
- DAQ – The VMM Application-Specific Integrated Circuit (ASIC)
- DAQ – The FPGA Readout Scheme
- Results/Summary

Introduction

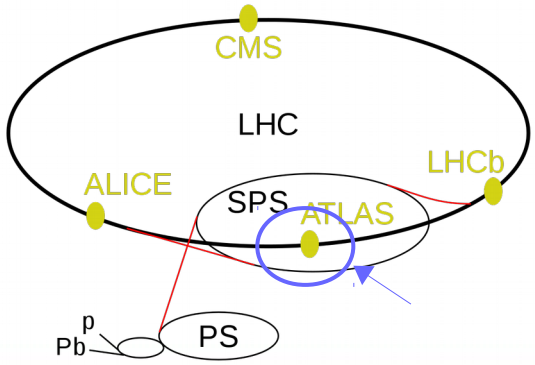
ATLAS and its Problematic Small Wheel



Small Wheels (SW) comprised of CSCs and MDTs

The ATLAS detector

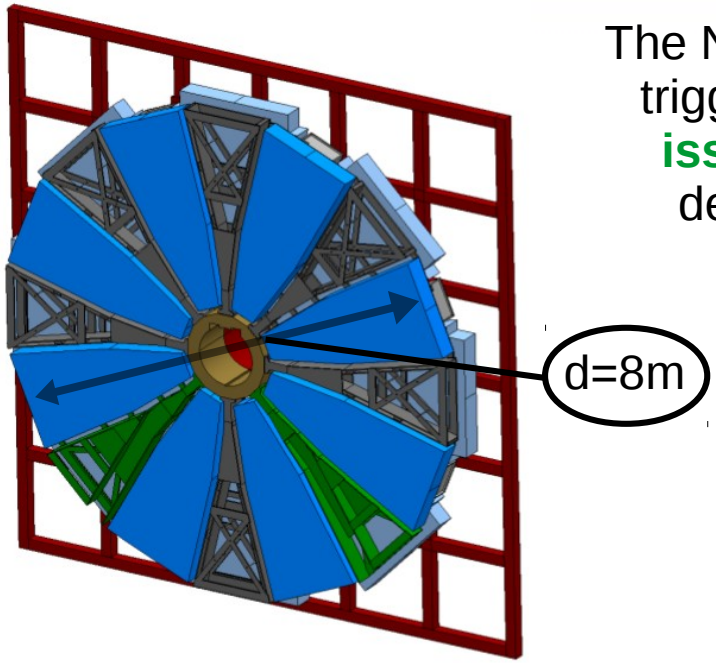
Diameter: 25 m
Length: 46 m
Barrel toroid length: 26 m
Overall weight: 7 000 tonnes
~ 100 million electronic channels
~ 3 000 km of cables



- Currently, **~90%** of the muon triggers in the end-cap region are **fake**
- **Tracking performance** in the SW will be **degraded**, as the background rate increases with luminosity

Introduction

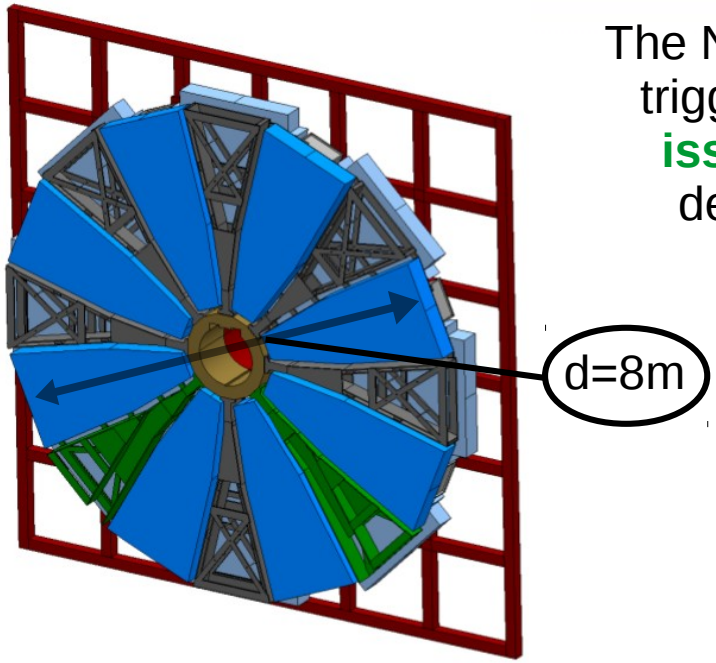
New Small Wheel – The Detectors



The NSW will provide high precision muon track reconstruction **and** trigger information to ATLAS, at high rates, thus **eliminating the issues** of the present SW. It will be installed during LS2. NSW detectors will be small-strip Thin Gap Chambers (sTGC) and Micromegas (MM). Both are filled with gas.

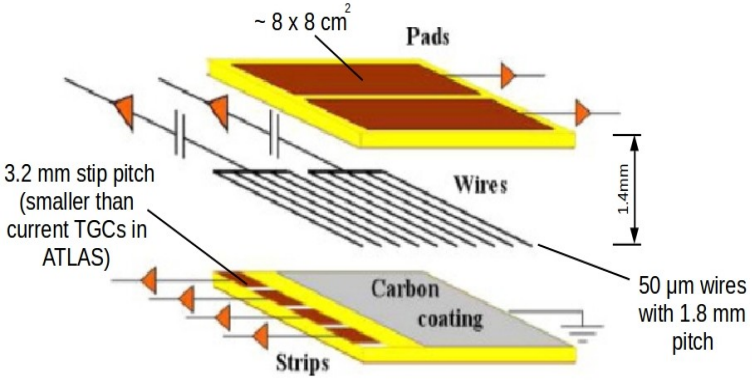
Introduction

New Small Wheel – The Detectors

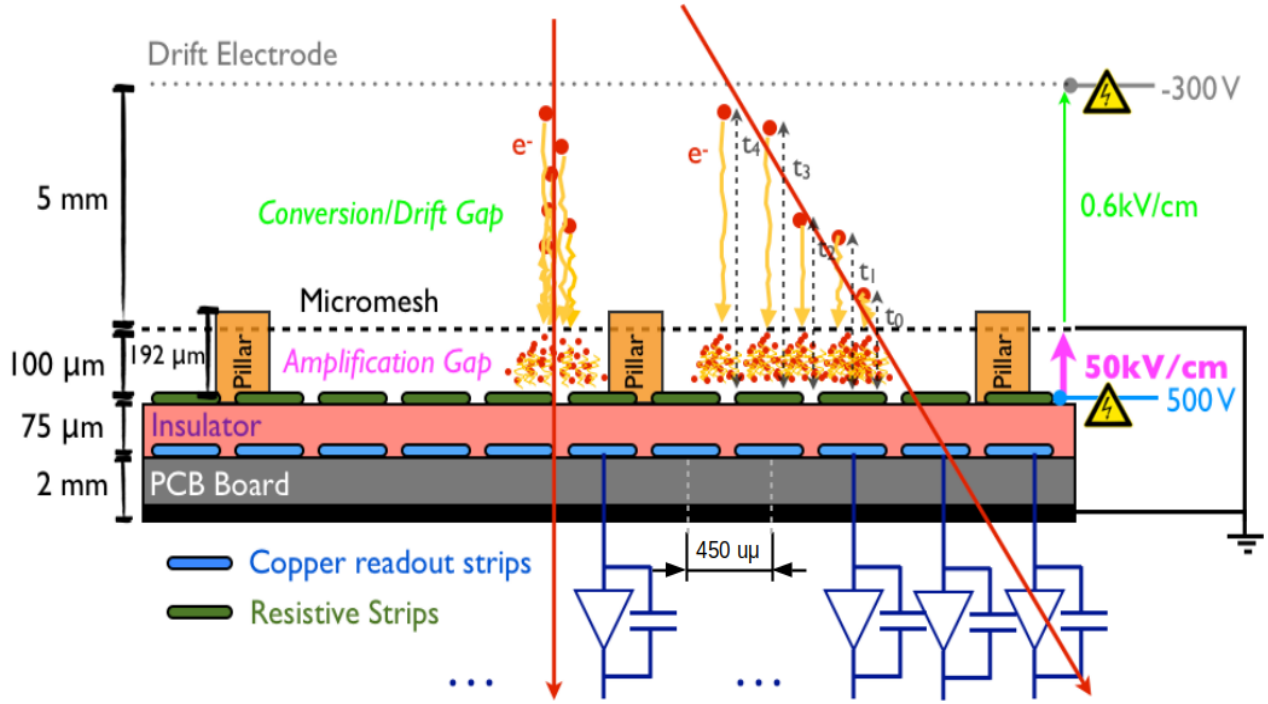


The NSW will provide high precision muon track reconstruction **and** trigger information to ATLAS, at high rates, thus **eliminating the issues** of the present SW. It will be installed during LS2. NSW detectors will be small-strip Thin Gap Chambers (sTGC) and Micromegas (MM). Both are filled with gas.

sTGC: Mainly for trigger, also for precision tracking



MM: Mainly for precision tracking, also for trigger



MM in Testbeam

Goals

- A 1-month-long testbeam was scheduled, in order to fully test a **large** MM prototype for the first time using the **final** front-end ASIC – the VMM. The main goals were:

MM in Testbeam

Goals

- A 1-month-long testbeam was scheduled, in order to fully test a **large** MM prototype for the first time using the **final** front-end ASIC – the VMM. The main goals were:

- To determine the **operation parameters** of the detector and its front-end chip

  - Too high HV results in **sparking**, but a too low voltage leads to **poor efficiency**. Is there a sweet spot?

  - What is the effect of different **gas mixtures** in detector performance?

  - VMM (Front-End ASIC) has plenty configurable parameters that affect data quality → many combinations to explore

MM in Testbeam

Goals

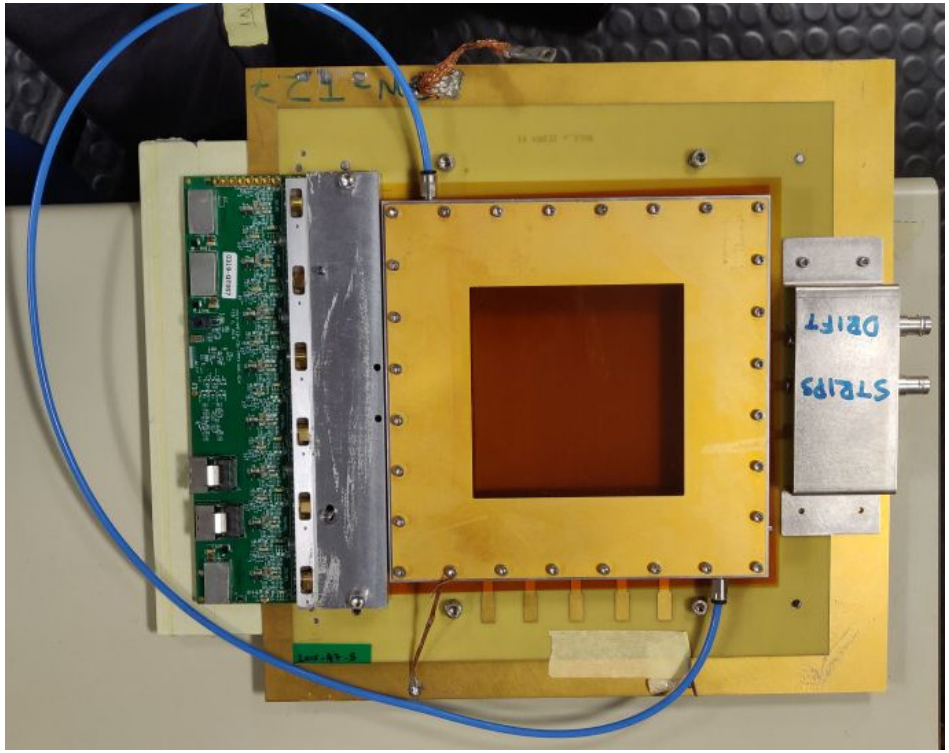
- A 1-month-long testbeam was scheduled, in order to fully test a **large** MM prototype for the first time using the **final** front-end ASIC – the VMM. The main goals were:
- To determine the **operation parameters** of the detector and its front-end chip
  - Too high HV results in **sparking**, but a too low voltage leads to **poor efficiency**. Is there a sweet spot?
  - What is the effect of different **gas mixtures** in detector performance?
  - VMM (Front-End ASIC) has plenty configurable parameters that affect data quality → many combinations to explore
- To validate the large prototype's **spatial resolution** under normal and angled tracks
- Scan the chamber for **dead areas** → give clues for bad chamber construction practices

MM in Testbeam

Detector Prototypes

For the Testbeam, two MM prototypes were used

T-Chamber



Small prototype, small active area of about 10 x 10 cm^2, small capacitance

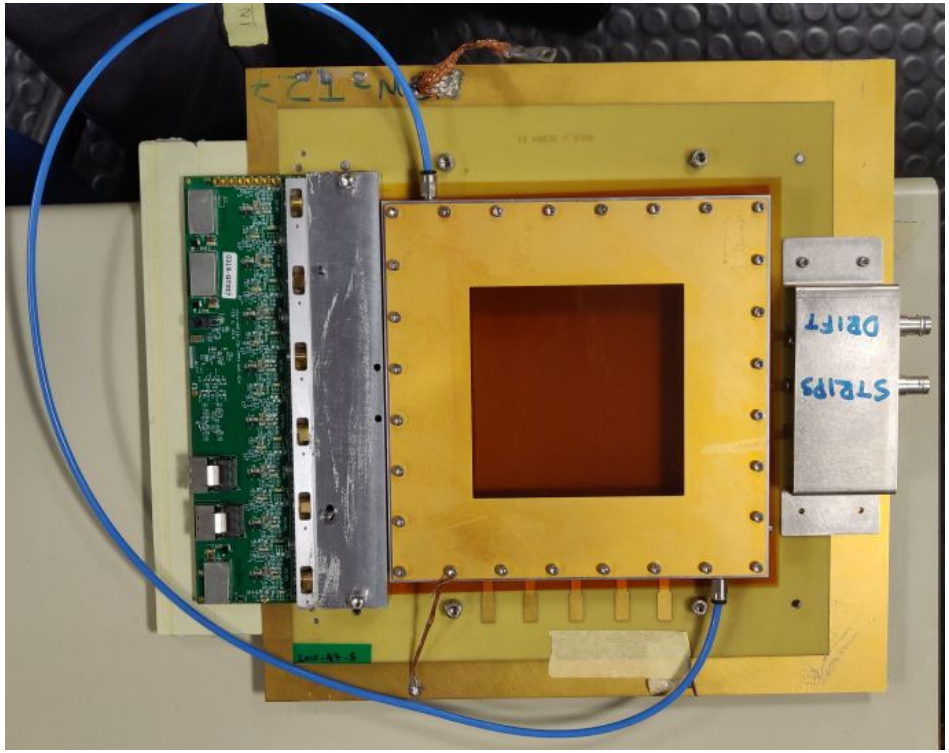
One layer, read-out by one board connected to 256 strips

MM in Testbeam

Detector Prototypes

For the Testbeam, two MM prototypes were used

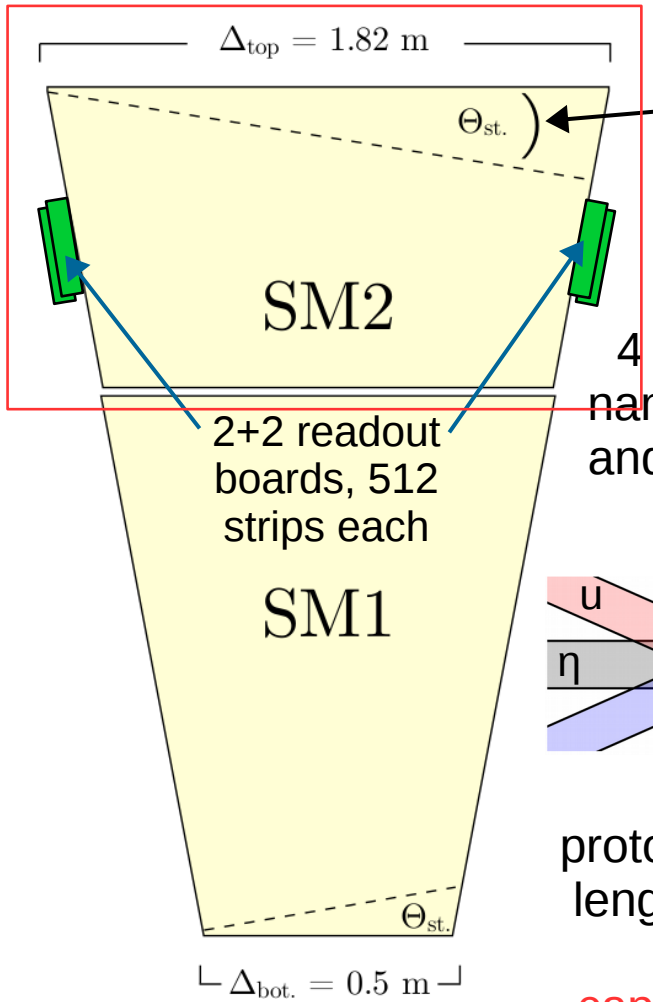
T-Chamber



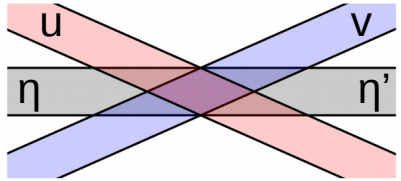
Small prototype, small active area of about 10 x 10 cm^2, small capacitance

One layer, read-out by one board connected to 256 strips

"Small" Module 2 (SM2)



4 layers, two named eta, eta' and two named u, v

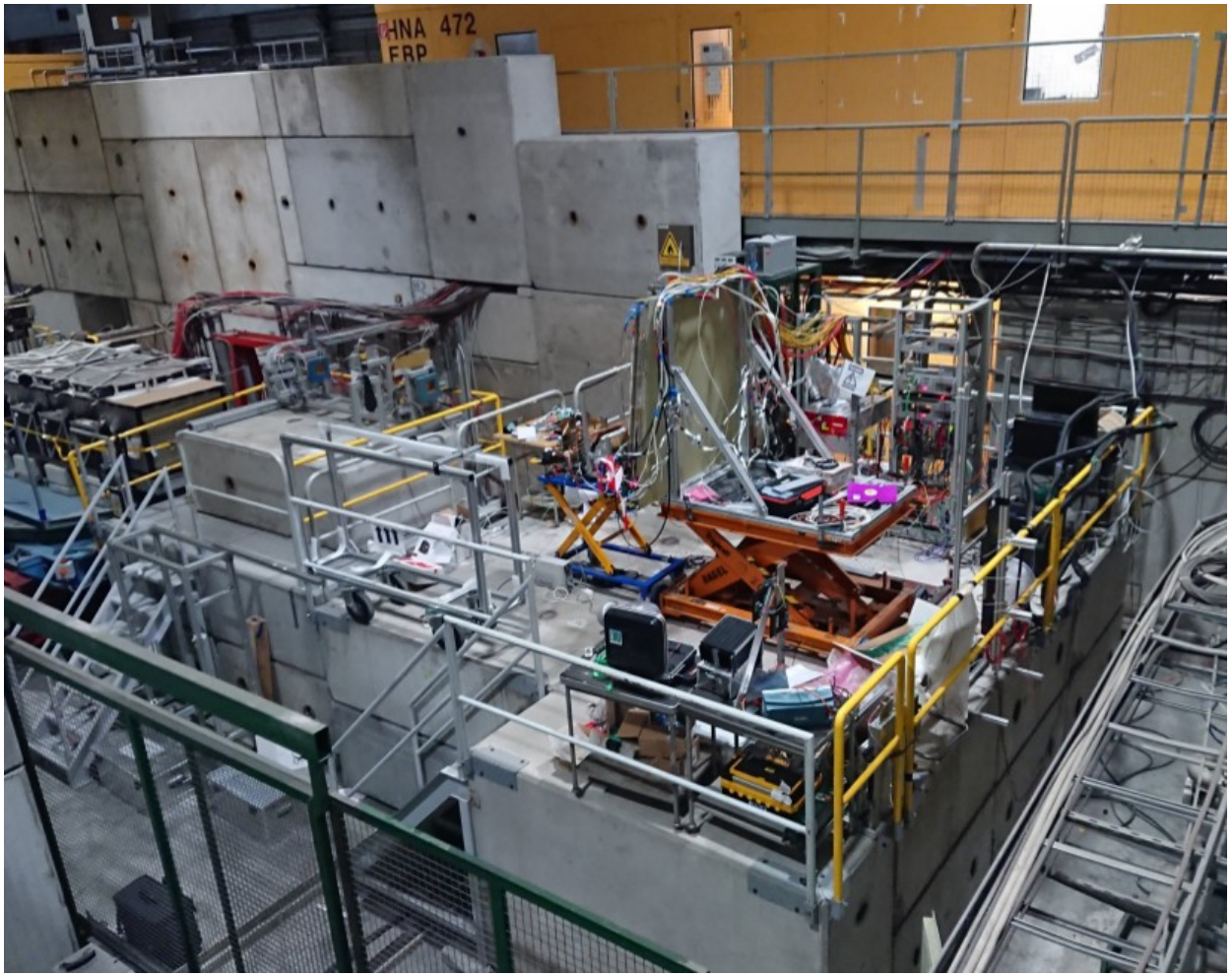


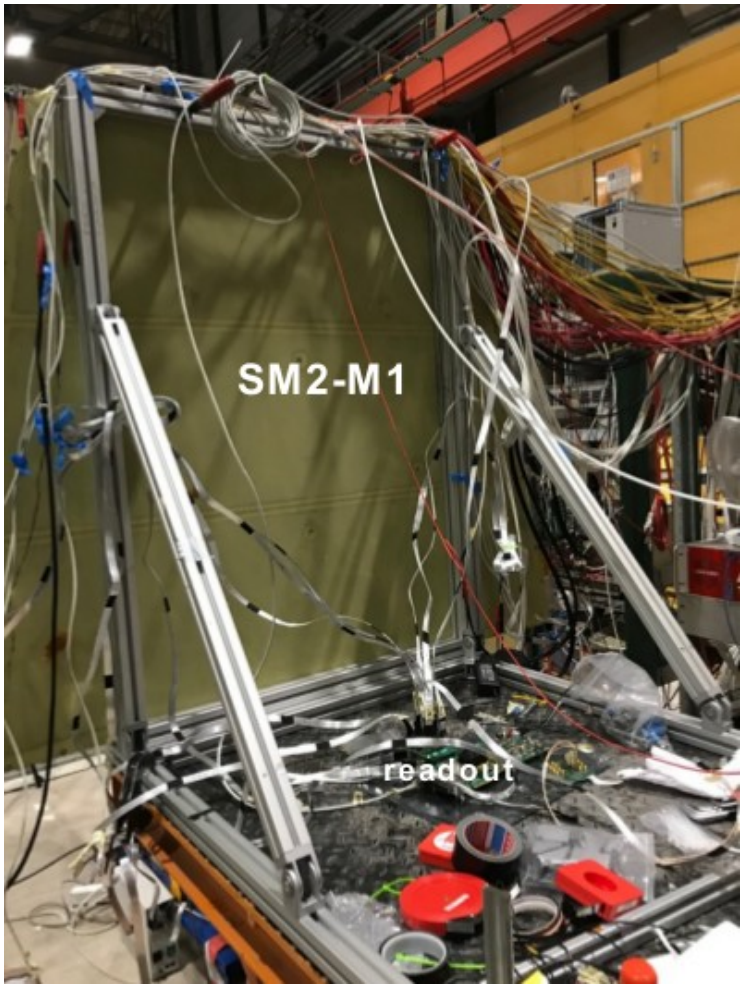
Large prototype, strip length 1.82m, large capacitance

MM in Testbeam

The Setup

Ran at H8C (Prevessin, CERN) from end of June to end of July 2018



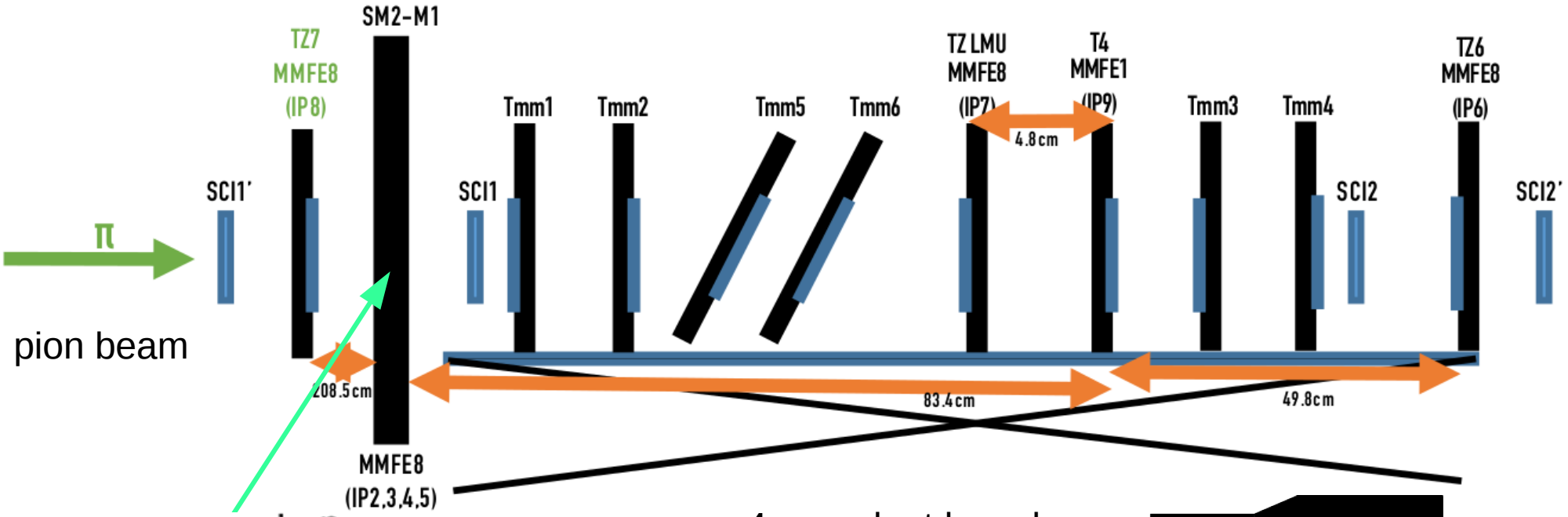


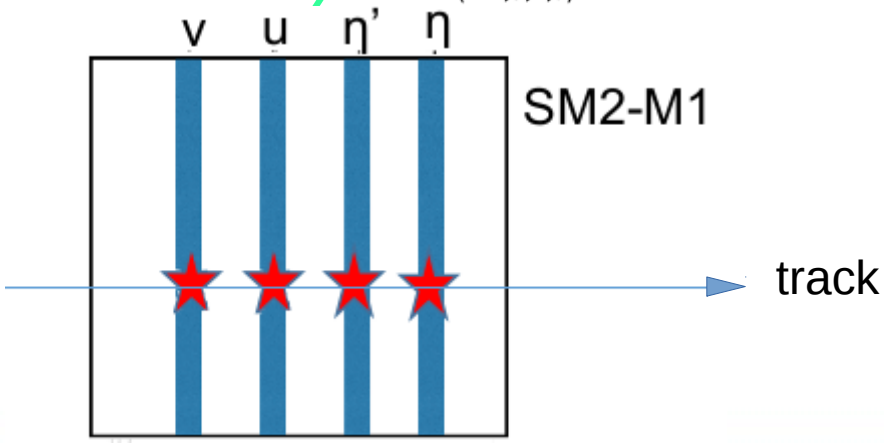
Used several T-chambers for tracking and one SM2

MM in Testbeam

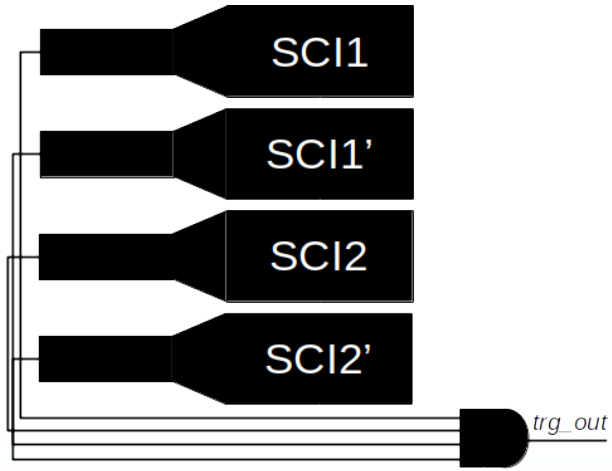
The Setup

Ran at H8C (Prevessin, CERN) from end of June to end of July 2018





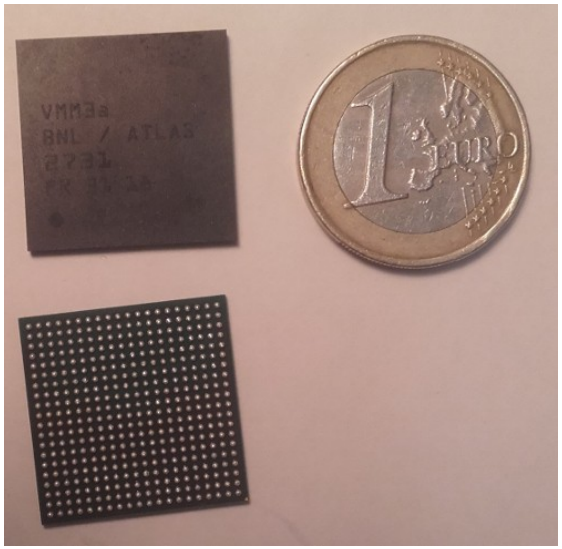
- 4 x readout boards (MMFE8) on SM2
- 4 x readout boards (3 x MMFE8, 1 x MMFE1) on T-chambers
- 4 x scintillators for triggering

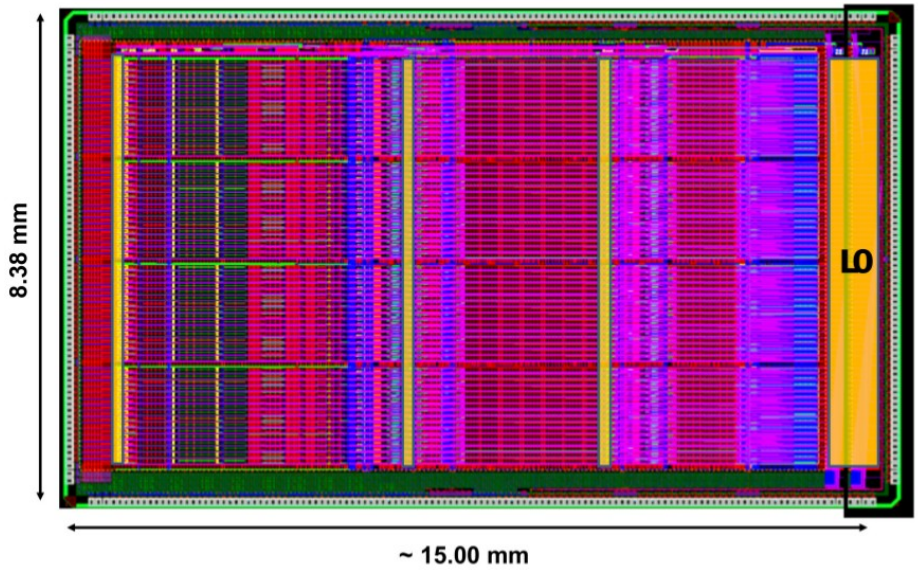


Micromegas Data Acquisition System

VMM ASIC
Overview

- A “sophisticated ADC” packaged in a small chip
  - Will be used to readout both sTGC and MM
- Provides coarse and fine pulse timing measurements
- Provides trigger primitives from both sTGC and MM



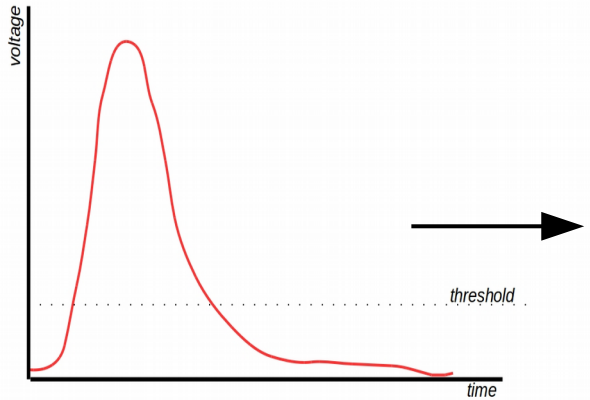


- 130 nm CMOS technology – 6 million transistors
- 64 channels per chip – each channel connects to one readout strip
- ~200 ns dead time per channel
- Timing resolution in the order of few hundred ps
- SEU protection (0.5 Mrad for 10 years of operation, ~60 SEU/y/VMM)

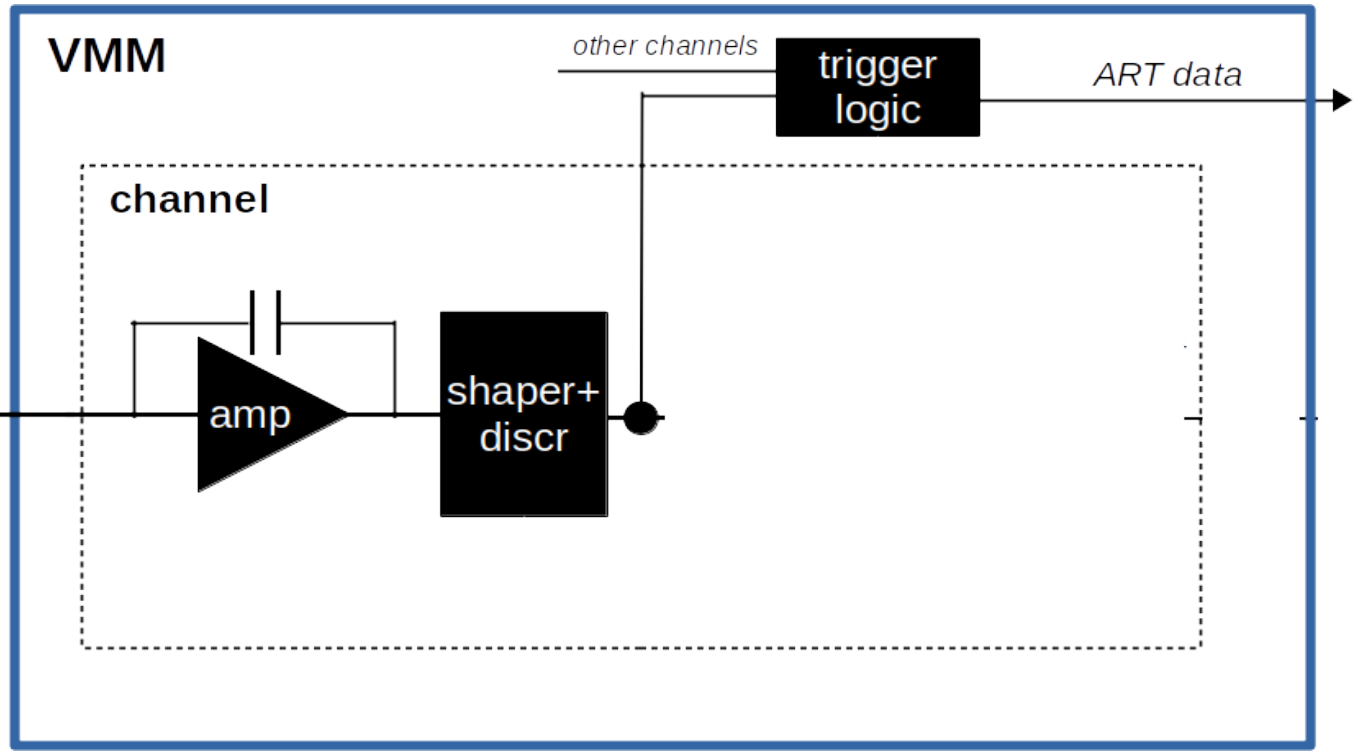
VMM ASIC

Readout and Trigger Outputs

Input pulse from strip
(after shaping)



VMM General Architecture



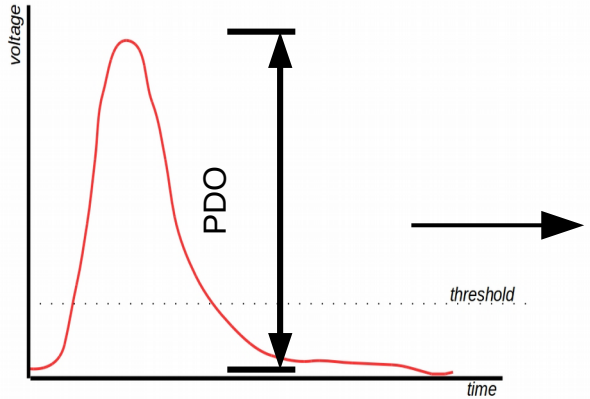
MM Trigger Path Address in Real Time (ART)

1	0	1	0	1	1

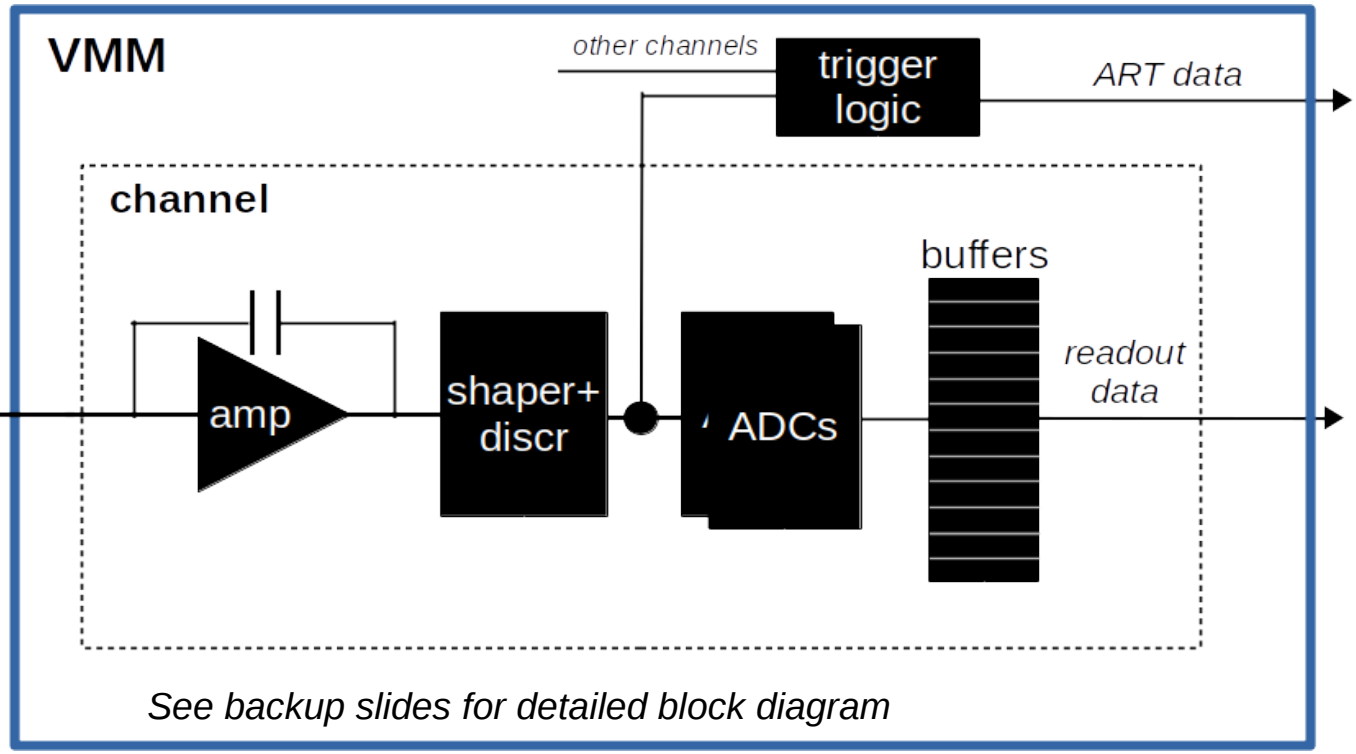
ID of first channel that fired in the chip

VMM ASIC
Readout and Trigger Outputs

Input pulse from strip
(after shaping)



VMM General Architecture



Outputs

(A) Readout Path (slow digitization)

1 0 1 0 1 1	channel_id
0 1 0 1 0 0 1 0	TDO (fine timing)
1 0 1 1 1 1 1 0 1 1	PDO (pulse amplitude)
1 0 1 1 1 1 1 0 1 1 1 0	BCID (coarse timing)

(B) Trigger Path - Address in Real Time (ART)

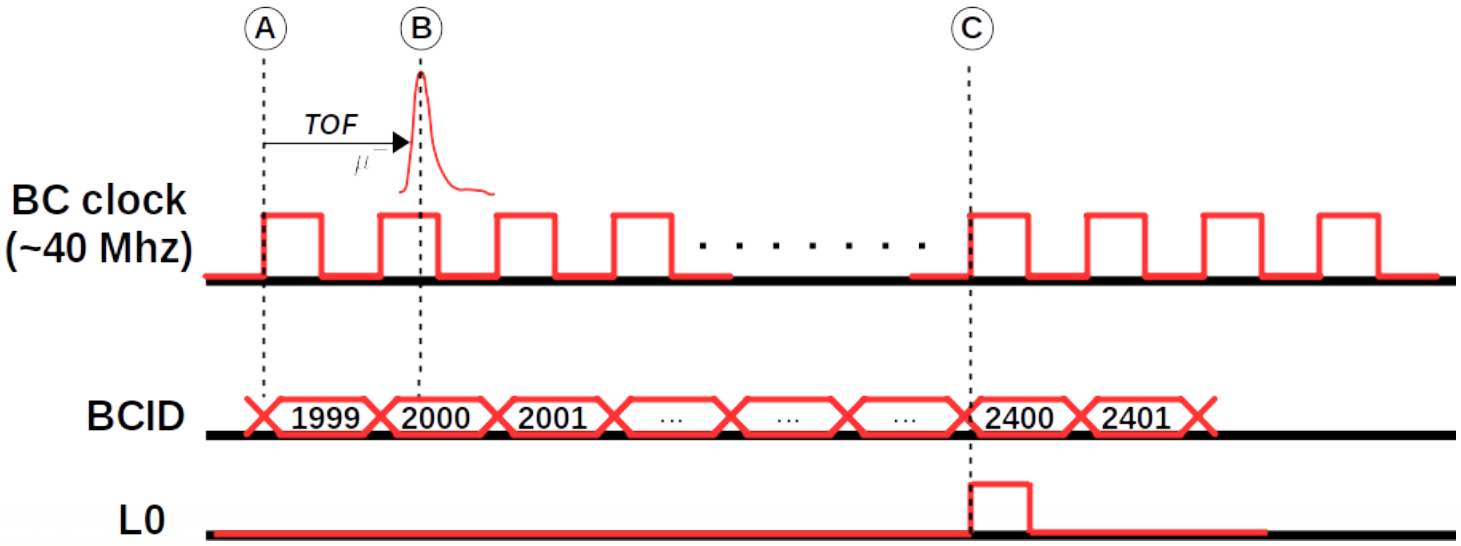
1 0 1 0 1 1	ID of first channel that fired in the chip

VMM ASIC
Level-0 Event Selection in ATLAS

How does the external readout chip select only muon-related data from VMM's buffers and discards other, irrelevant events?

A: Collision at the IP

B: A peak is found after the muon's TOF (~30 ns), and tagged with BCID = 2000 by the VMM. Data get buffered



VMM ASIC
Level-0 Event Selection in ATLAS

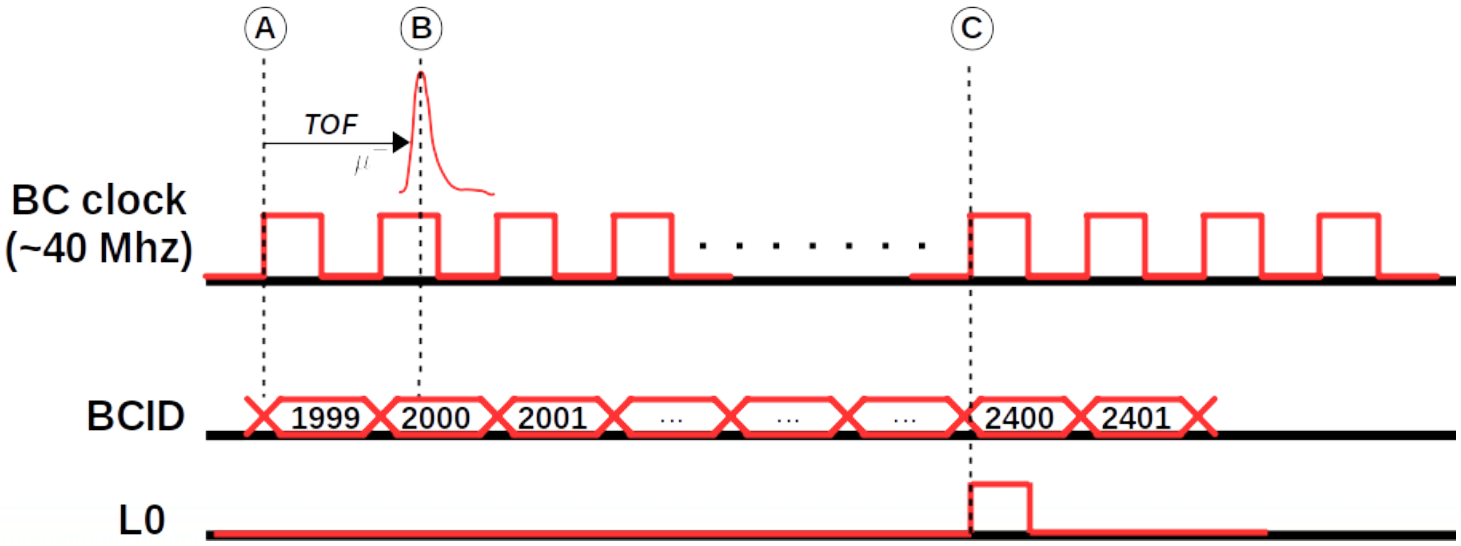
How does the external readout chip select only muon-related data from VMM's buffers and discards other, irrelevant events?

A: Collision at the IP

B: A peak is found after the muon's TOF (~30 ns), and tagged with BCID = 2000 by the VMM. Data get buffered

B→C: A trigger decision is being made by an external source (back-end Trigger Electronics)

C: Level-0 (L0) signal is received by VMM, gets tagged with BCID = 2400



VMM ASIC
Level-0 Event Selection in ATLAS

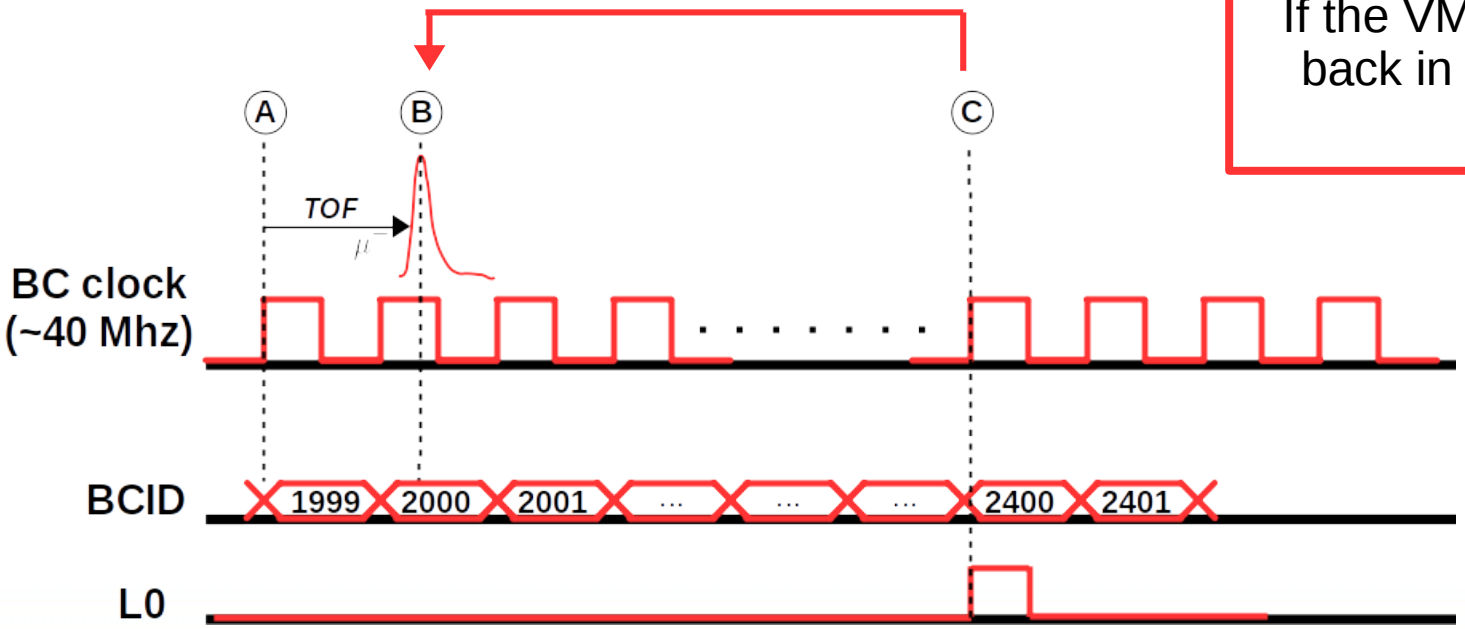
How does the external readout chip select only muon-related data from VMM's buffers and discards other, irrelevant events?

A: Collision at the IP

B: A peak is found after the muon's TOF (~30 ns), and tagged with BCID = 2000 by the VMM. Data get buffered

B→C: A trigger decision is being made by an external source (back-end Trigger Electronics)

C: Level-0 (L0) signal is received by VMM, gets tagged with BCID = 2400



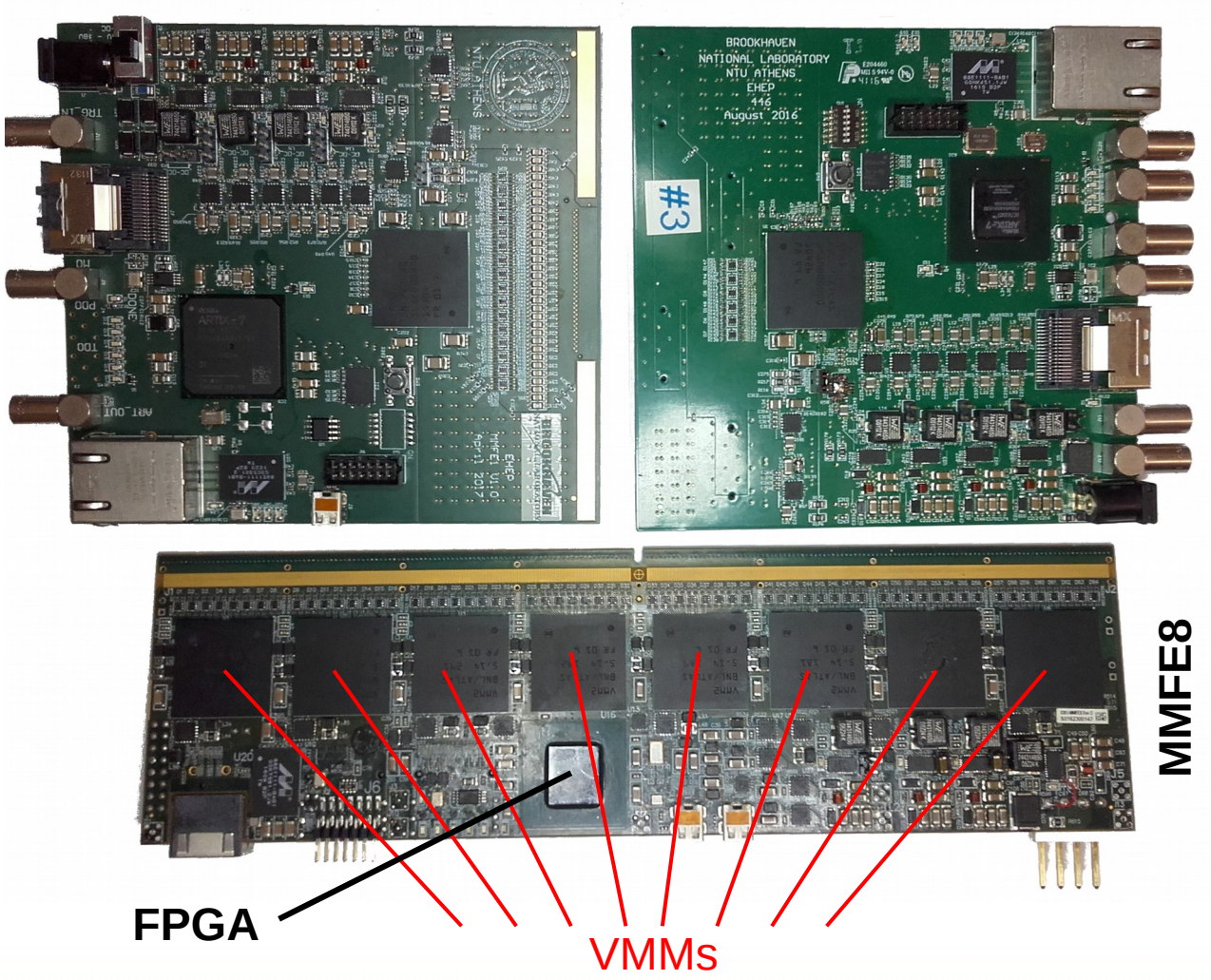
If the VMM is pre-configured to "go back in time" by 400 BCs → data are collected

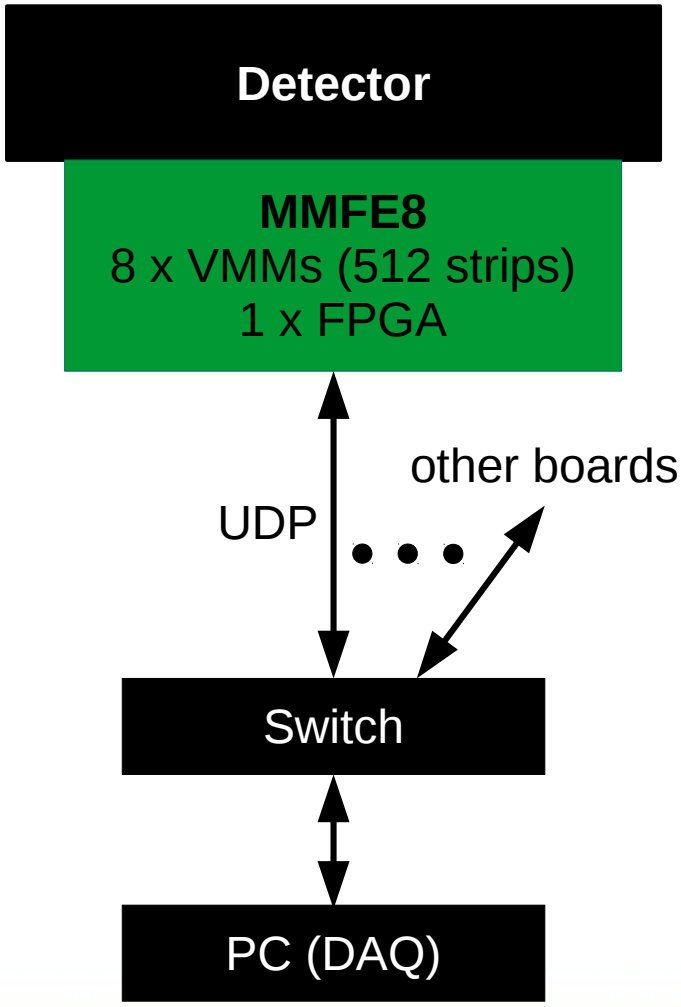
This is the *Level-0 Latency*.
2.5 us max for Phase-I,
10 us for Phase-II

FPGA Readout

The Boards

In absence of readout ASICs, the readout, configuration and calibration of the VMM is performed by an FPGA, that communicates with a DAQ software via UDP

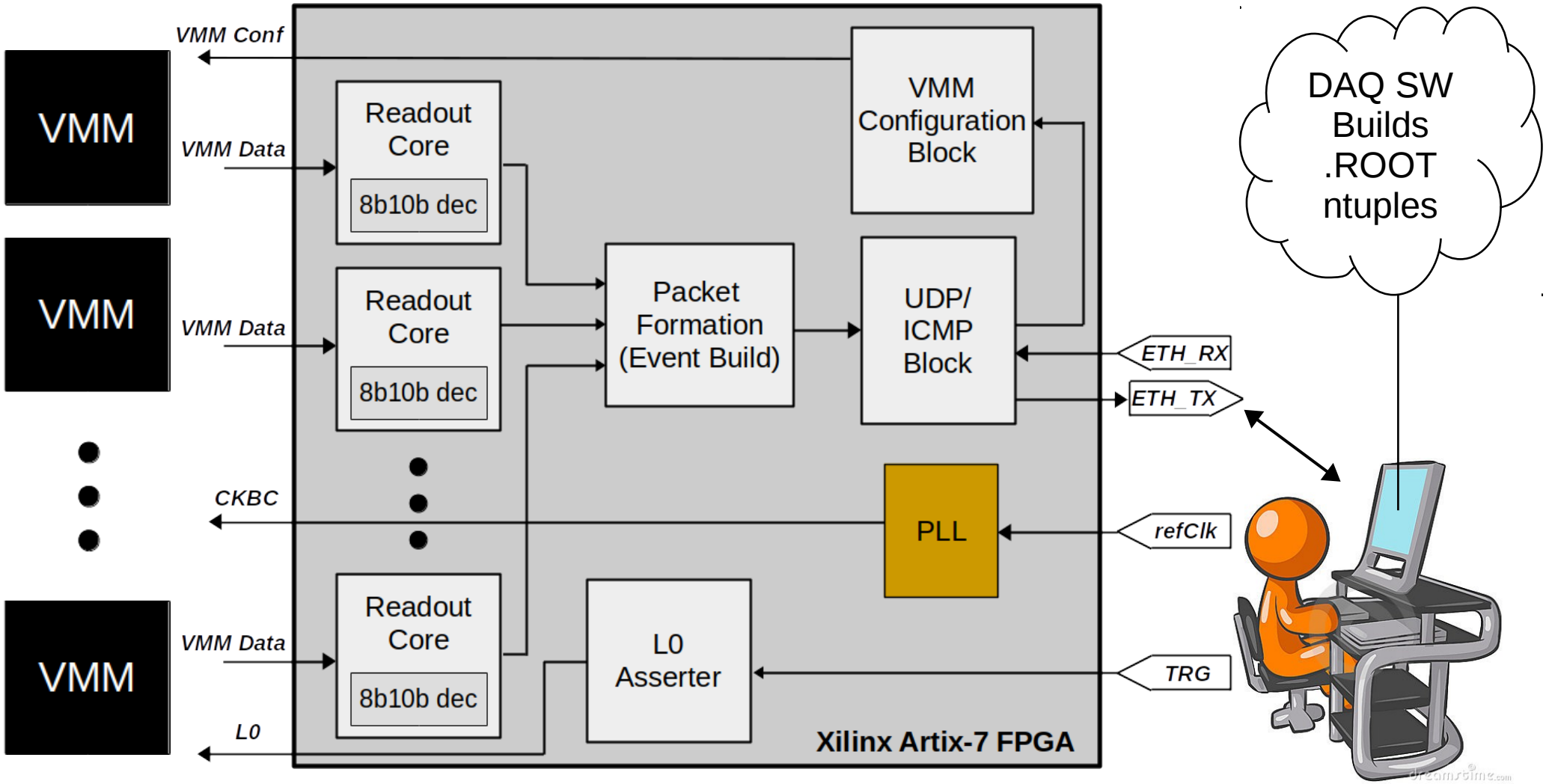




FPGA Readout

Front-End Firmware Block Diagram

Is implemented in all front-end FPGAs

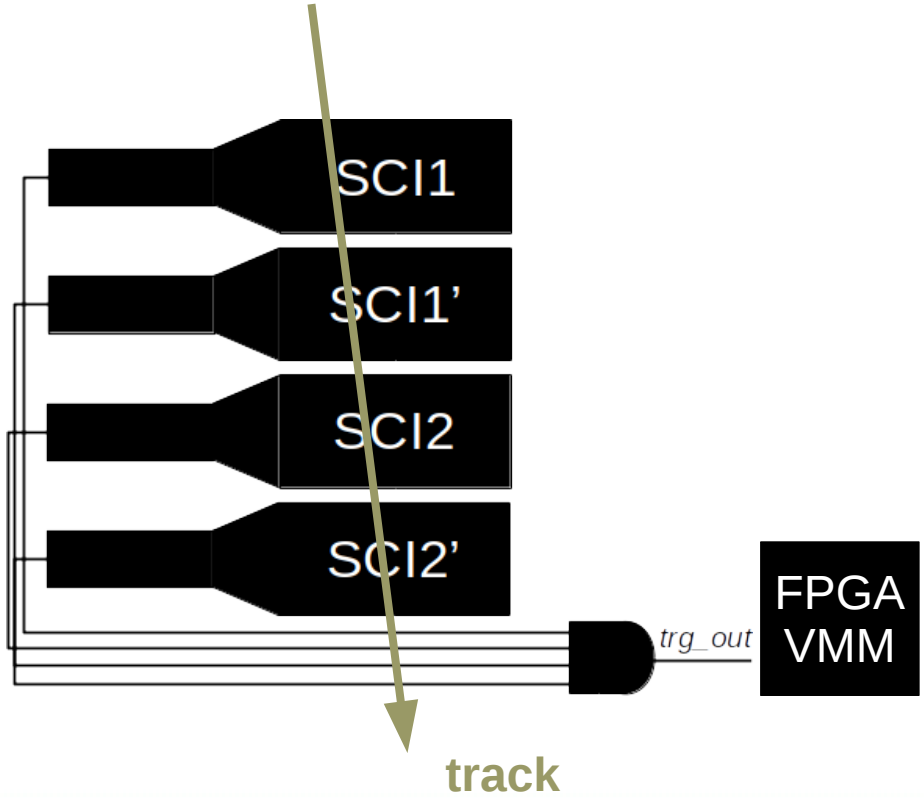


FPGA Readout

Trigger: Using the Scintillators

The standard readout scheme is to input the scintillator trigger coincidence into the FPGA

Standard Scintillator Coincidence Readout

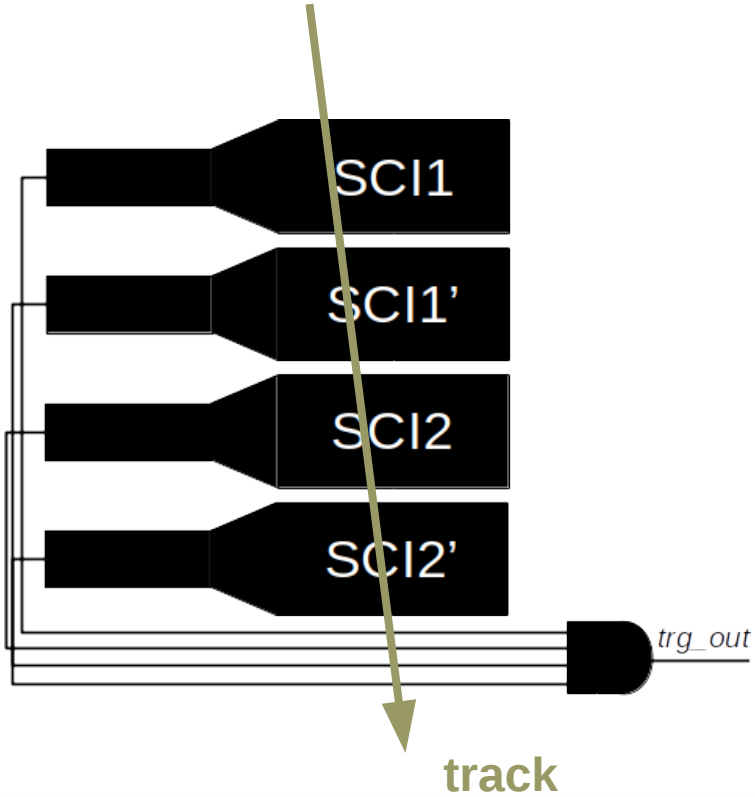


FPGA Readout

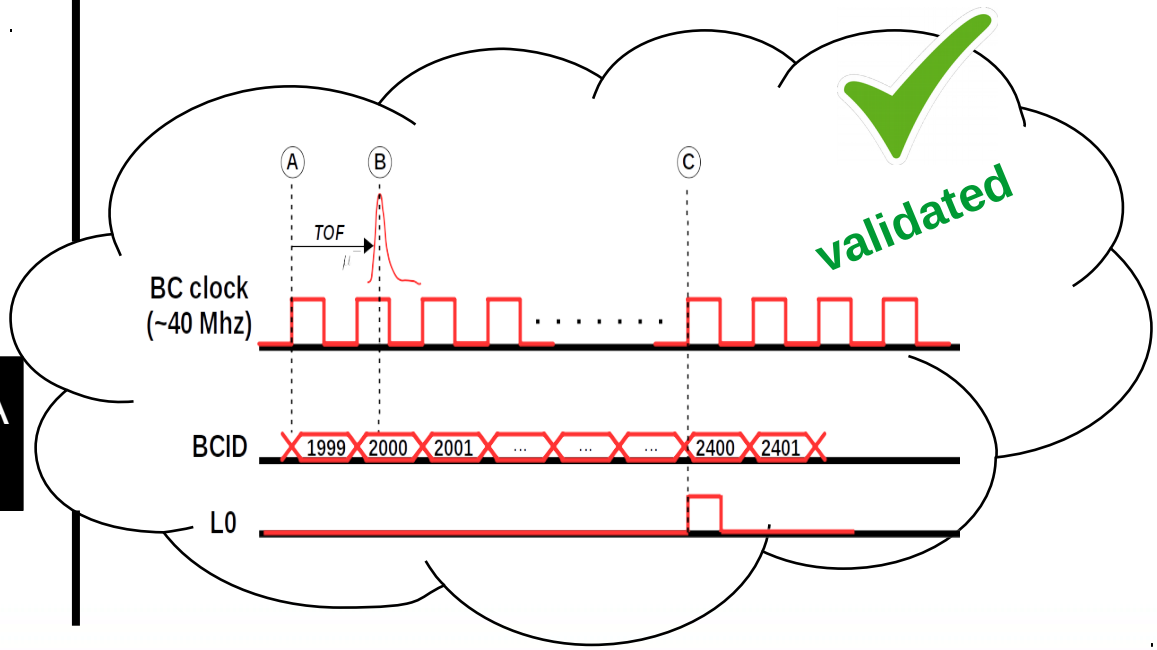
Trigger: Using the Scintillators

The standard readout scheme is to input the scintillator trigger coincidence into the FPGA

Standard Scintillator Coincidence Readout

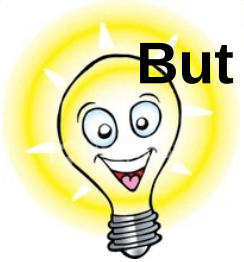


Taking the L0 readout logic of the VMM into account: the FPGA issues the L0 signal upon reception of **external trigger** (scintillator coincidence), selecting **only pion/muon related data**



FPGA Readout

Trigger: An Idea



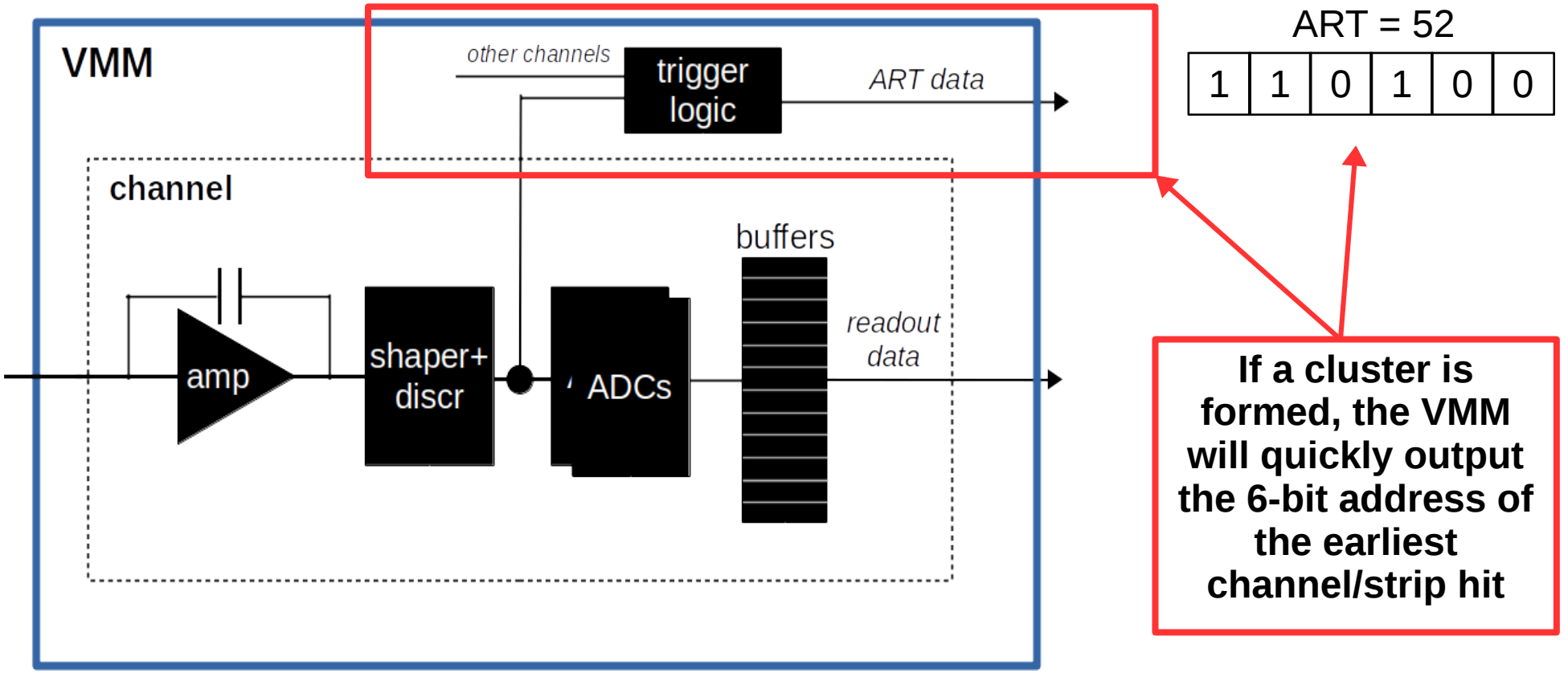
But since the VMMs produce trigger primitives and readout data, why not add them into the “trigger mix” as well?

FPGA Readout

Trigger: Using the VMM for Self-Triggering

But since the VMMs produce trigger primitives and readout data, why not add them into the "trigger mix" as well?

VMM Address-in-Real-Time (ART) Logic

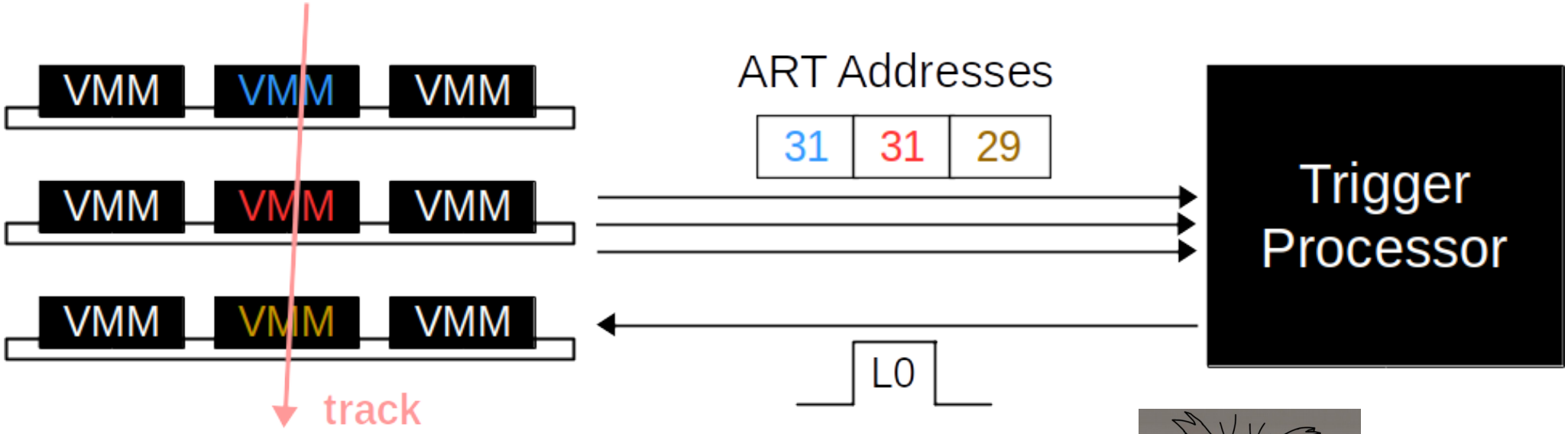


FPGA Readout

Trigger: Using the VMM for Self-Triggering

An example: A particle passes through the SM2 detector, four VMMs output ART addresses → an external device processes the addresses from three VMMs and asserts the L0/trigger signal

“Scintillator-Less” Triggering in Testbeam!

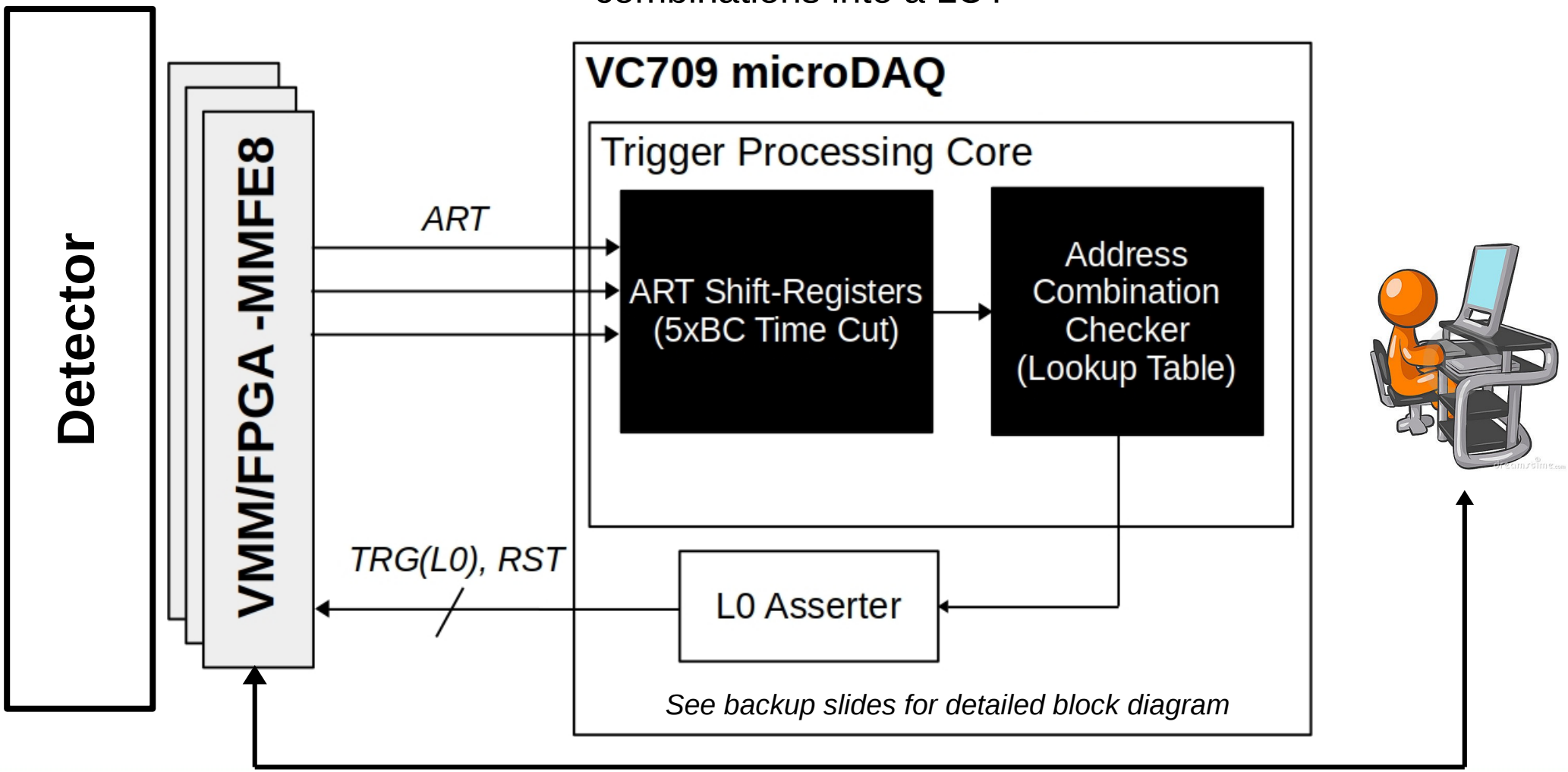


So all we need now is a Trigger Processor….

FPGA Readout

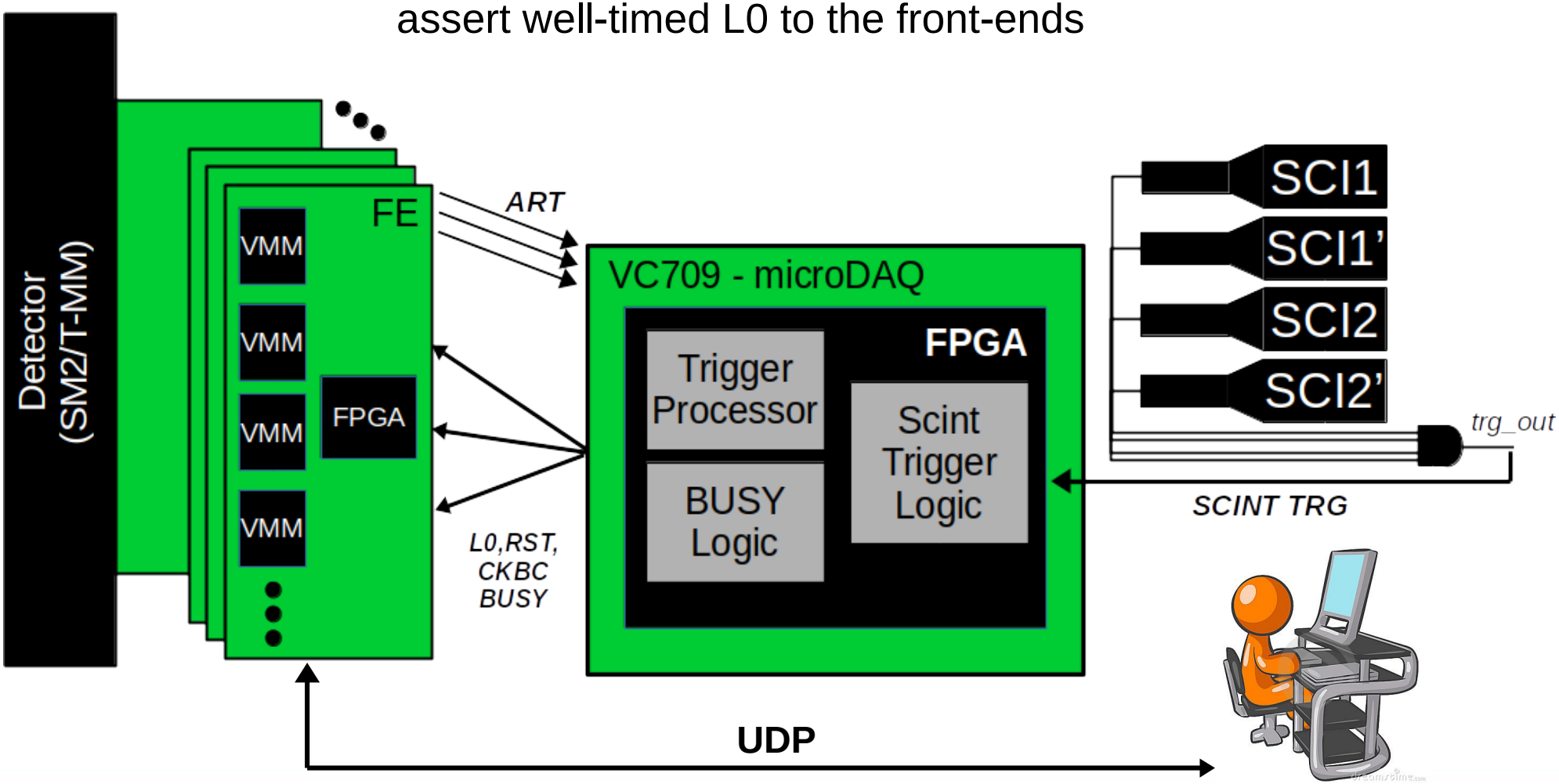
The microDAQ Trigger Processor Scheme

Implemented on a Xilinx VC709 Evaluation Board, the microDAQ trigger processor produces L0 triggers with a 650ns latency by driving the VMM ART address combinations into a LUT



DAQ Overview

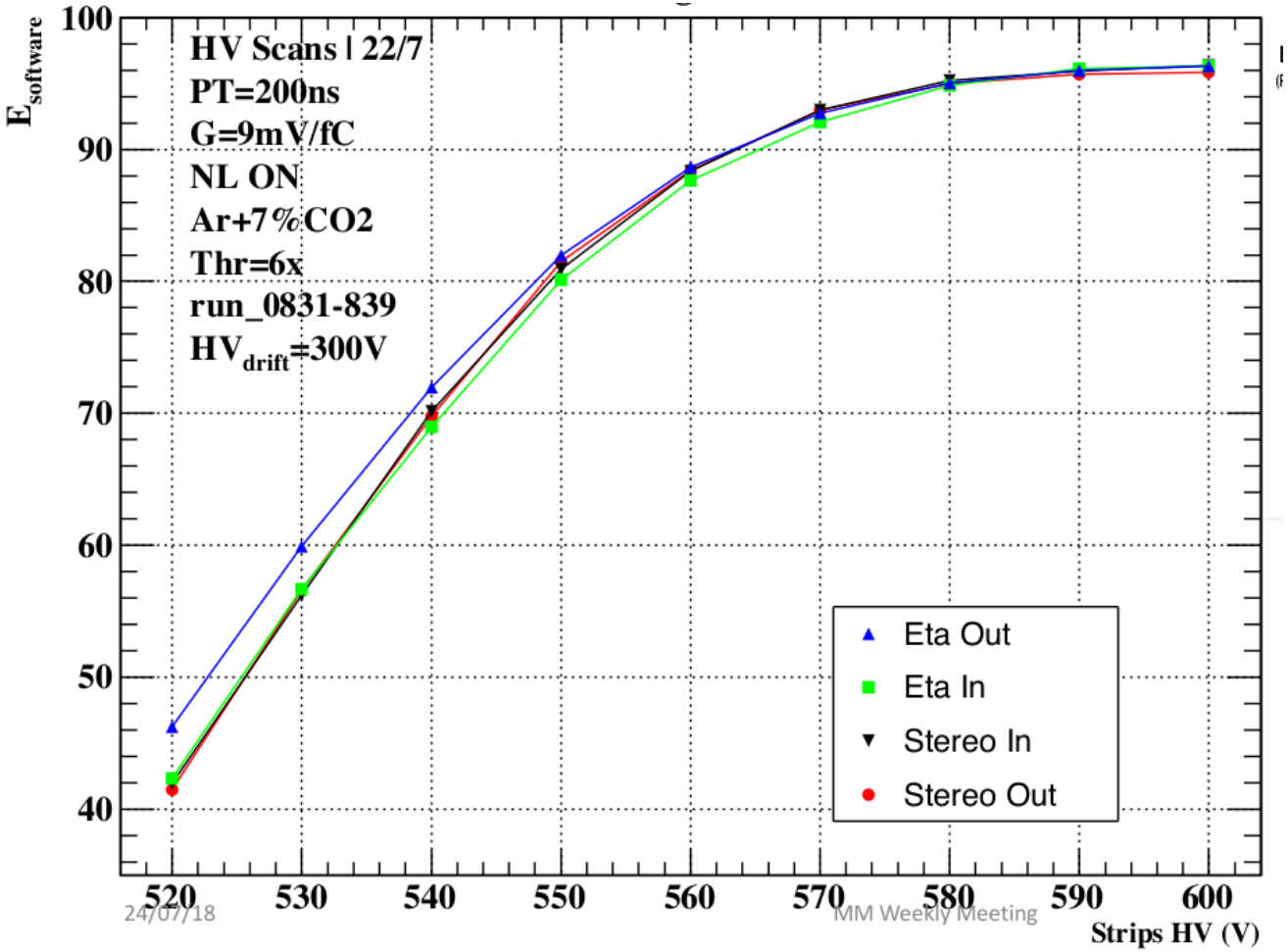
The microDAQ board connects with up to **eight** Front-Ends. Keeps them in **sync**, providing a common reference clock and a BUSY. It accepts scintillator coincidence triggers and sends well-timed L0 to the front-ends **or processes ART data** to assert well-timed L0 to the front-ends

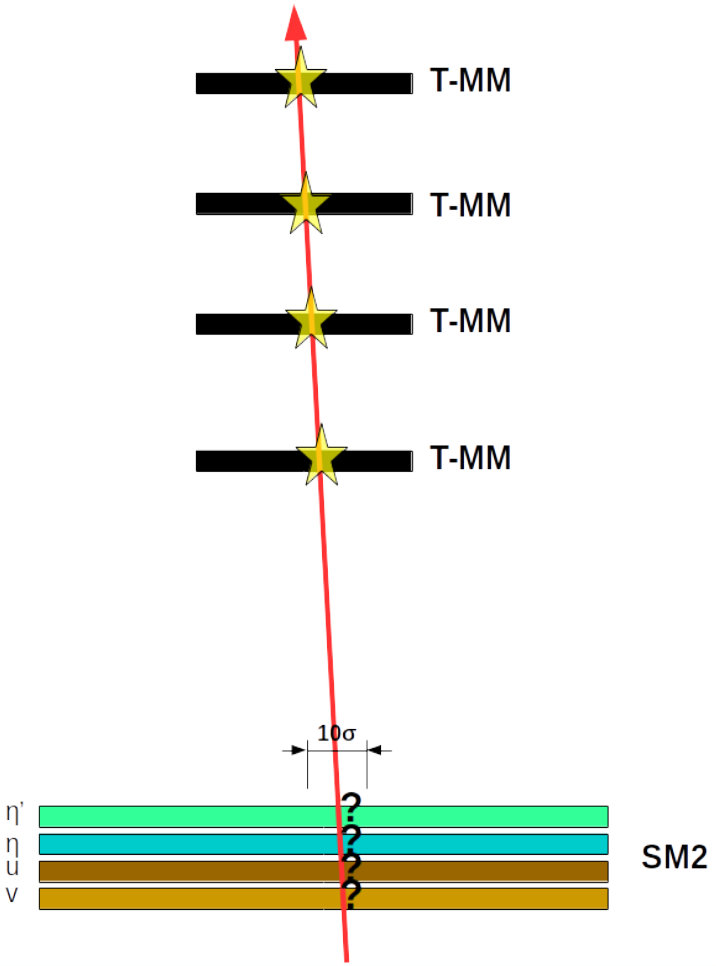


Results

HV Working Point and Gas Studies

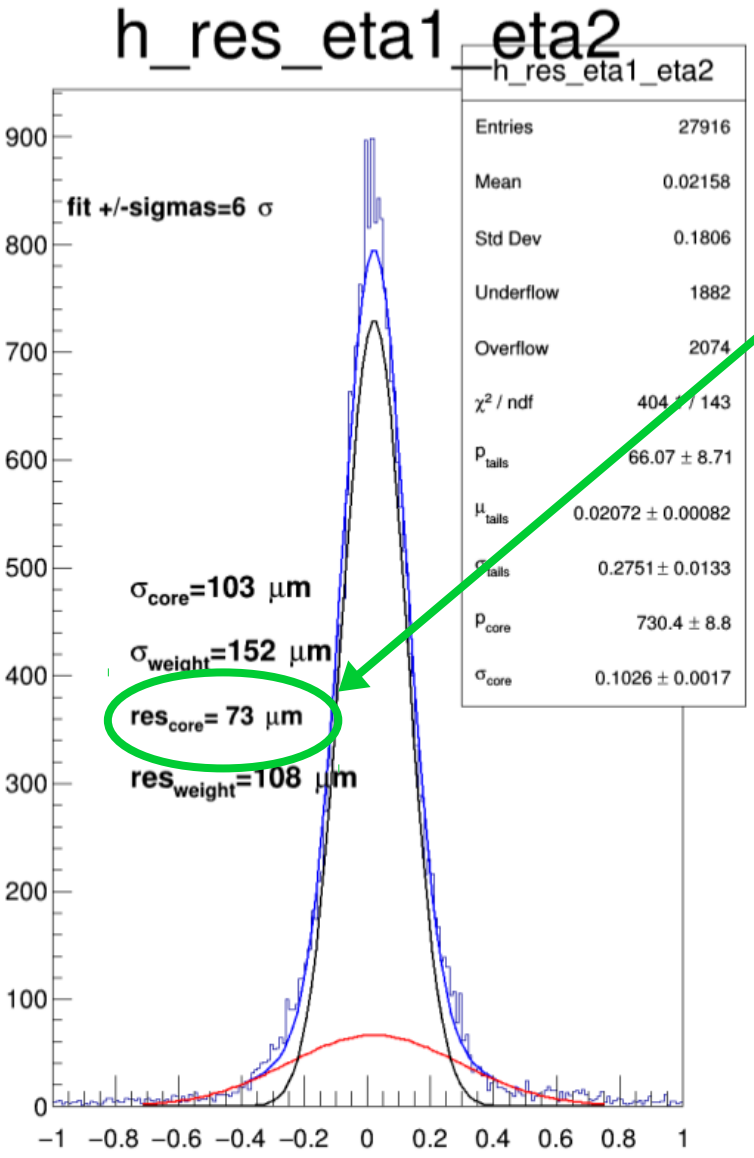
During the testbeam period, several studies with different gas mixtures and HV settings were performed. These studies were **imperative** to determine the full-size MM operation parameters





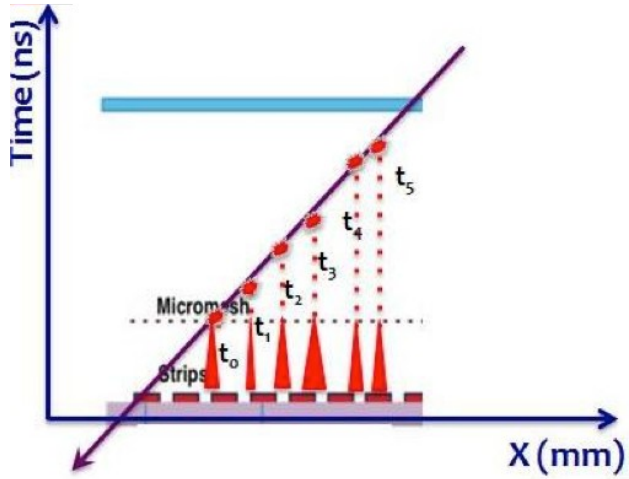
Results

Spatial Resolution – Within Specs



First testbeam results of large MM chamber prototype and final front-end ASIC (VMM), show that the chamber is performing within requirements resolution-wise

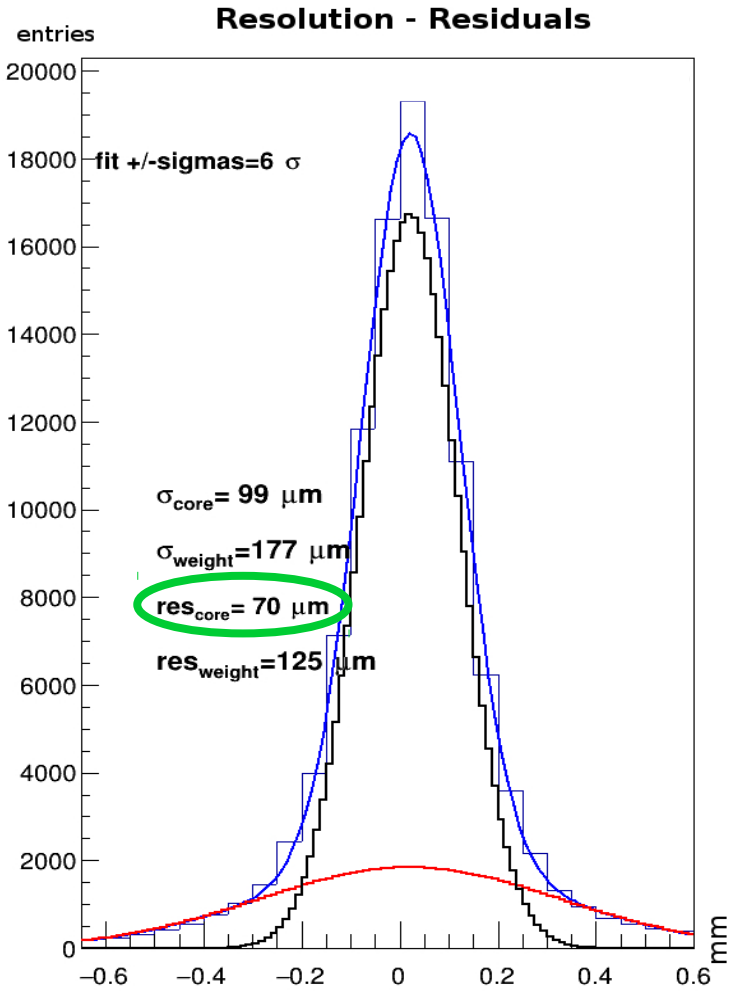
Angled track analysis is a work-in-progress (previous work with small chambers and VMM has shown a spatial resolution as low as 100μm)

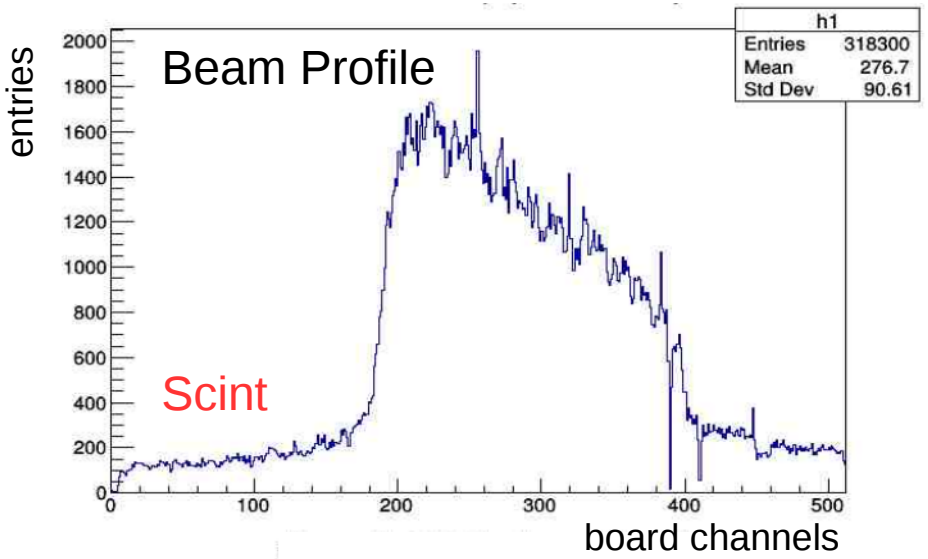


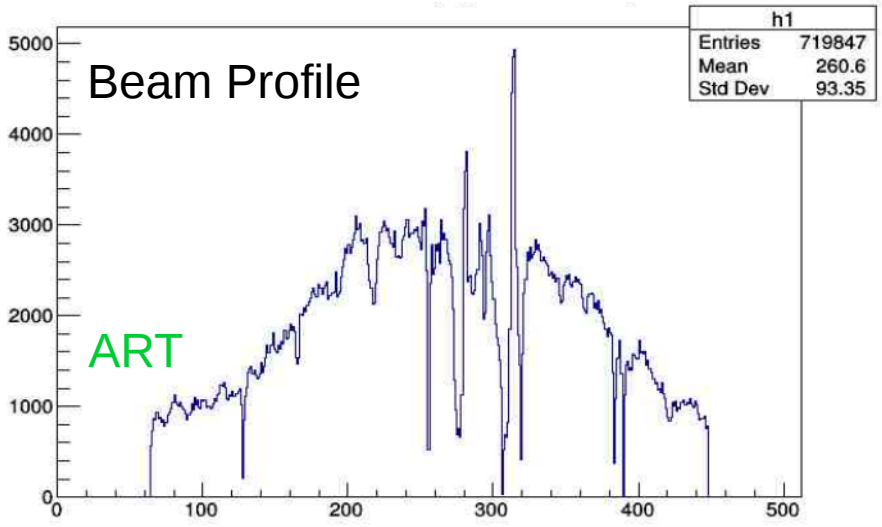
Results

MM Can Run Self-Triggered

The concept of using **only** the ART as a trigger gives a **good** resolution, more triggers per spill and a **wider** aperture with respect to scintillator triggering







Conclusions

- The 1-month-long testbeam was a huge collaborative effort, the **first with a full-size MM prototype and the final front-end chip**
- The DAQ system proved its **efficiency and reliability**. Within three days everything was setup for data taking. Rate >> 5 kHz/channel and 200k events per spill
- The MM working group of the NSW now has a **clearer picture** of what will the operating parameters of the chamber and the front-end electronics be. We can now move on the chamber construction with **more confidence**.
- The MM module's performance in terms of spatial resolution and efficiency was **validated**. Angled track resolution is a WIP
- The MM's and the VMM's **trigger** performance was **validated**, as we managed to collect data in a consistent manner, just by using the chip's trigger primitives

The Team

Testbeam Collaborators

Theo Alexopoulos, George Iakovidis, Christos Bakalis, Aimilios Koulouris, Stavros Maltezos, Dimitris Matakias, Paris Moschovakos, Christos Paraskevopoulos, Venetios Polychronakos, Polyneikis Tzanis
BNL/NTUA group

Melisa Franklin, Alex Tuna, Ann Wang, Sarah Flynn, G. Rabanal
Harvard

Patrick Scholer
Freiburg

Alan Peyaud
Saclay

Ralf Hertenberger, Bernhard Flierl , Christoph Jagfeld, Felix.Klitzner, Philipp Loesel, Maximilian Rinnagel
LMU

Kostas Ntekas
UC Irvine

Valerio D'Amico, Luca Martinelli
Roma Tre

A big Thank You to everyone who participated in the effort!

Backup

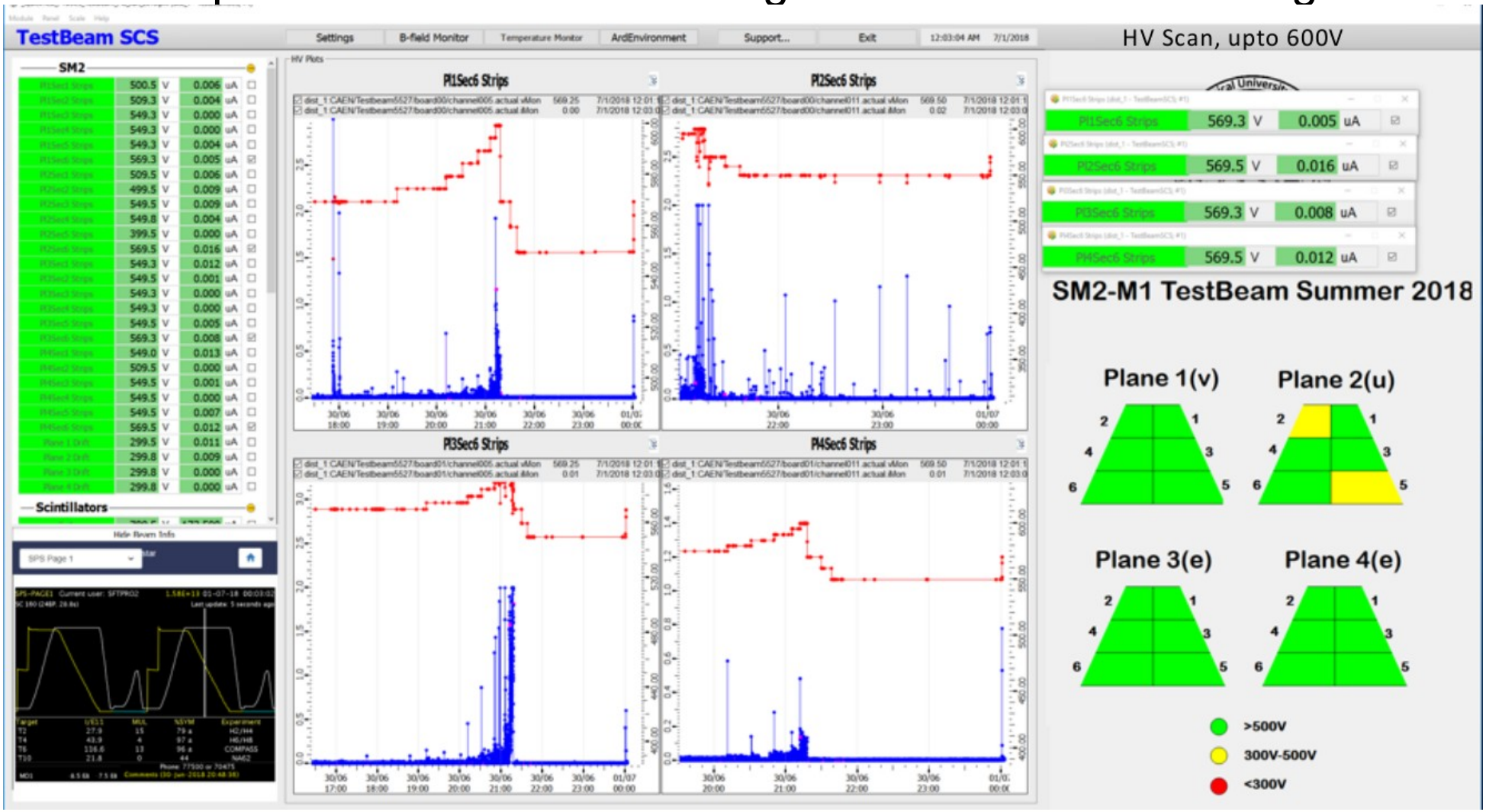
Useful GitLab Links

- VMM Readout Firmware (on Front-End FPGAs)
  - https://gitlab.cern.ch/NSWelectronics/vmm_boards_firmware
- microDAQ Firmware (VC709 supervisor and Trigger Processor)
  - https://gitlab.cern.ch/cbakalis/microDAQ_VMM
- VERSO (DAQ Software – thanks to D.J. Antrim)
  - https://gitlab.cern.ch/NSWelectronics/vmm_readout_software
- Monitoring Software
  - https://gitlab.cern.ch/aikoulou/vmm-mon
- Analysis Software
  - https://gitlab.cern.ch/aikoulou/koulVMM3

Testbeam Tools

Detector Control

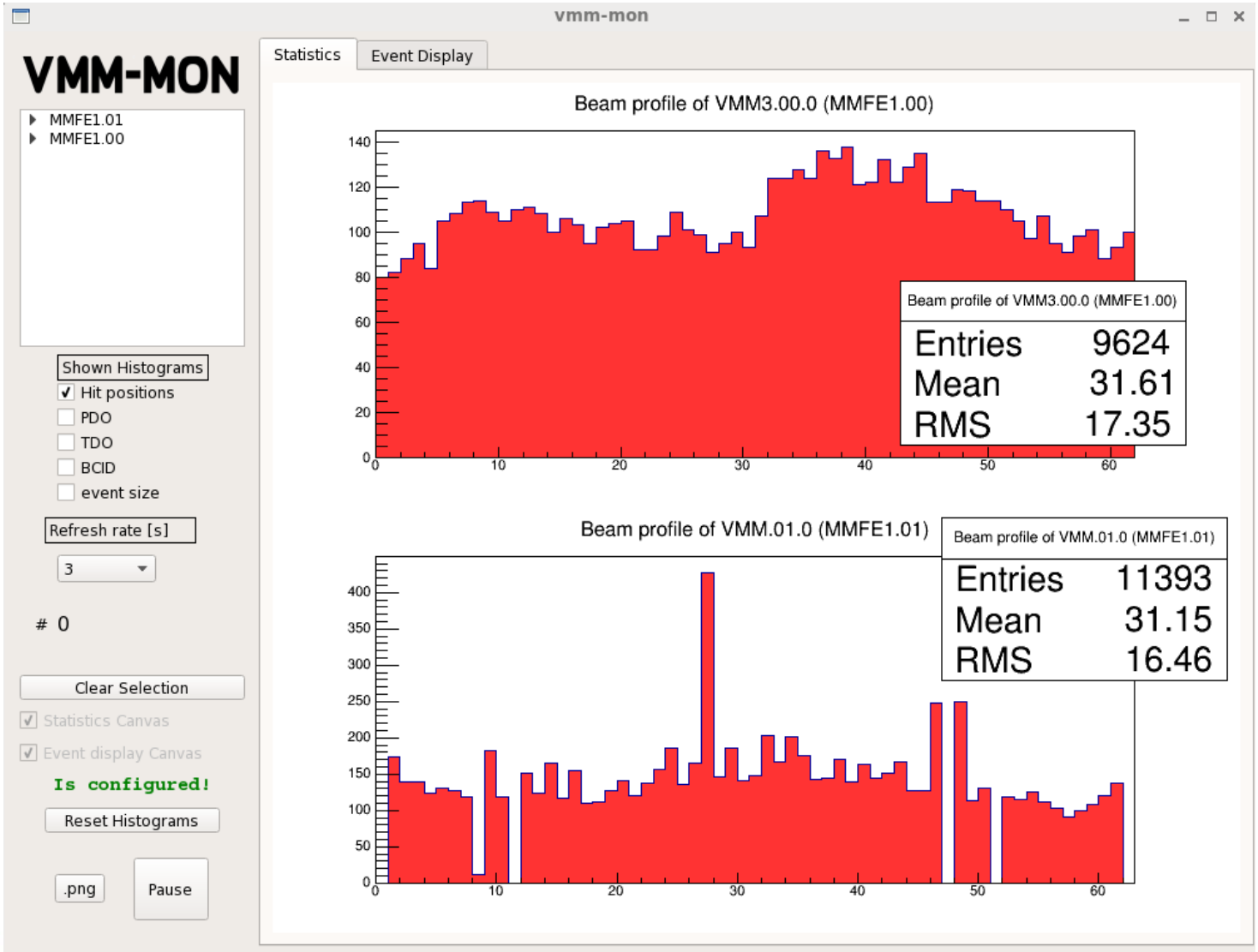
Based on WinCC-OA, the Detector Control System allows for remote operation of chamber voltage and current monitoring



Testbeam Tools

DAQ Monitoring

On-line plotting of chamber data



Can plot:

- Hit positions (beam profile)
- Charge distributions
- … and more

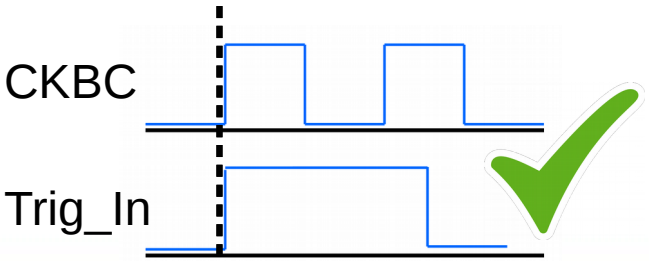
Synchronous Trigger

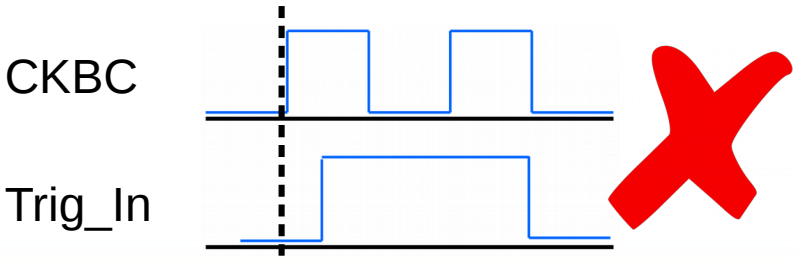
When running with angled tracks, it is **imperative** to have a well-defined t0. Abscence of a well-defined t0 will cause a 25ns-jitter in the measurements, which is a show-stopper for uTPC (angled track) analysis in the MM for testbeams

→ The t0 in the actual experiment is well-defined, as the collision at the IP occurs at the CKBC rising-edge, and we also know the TOF of a muon from the IP to the NSW

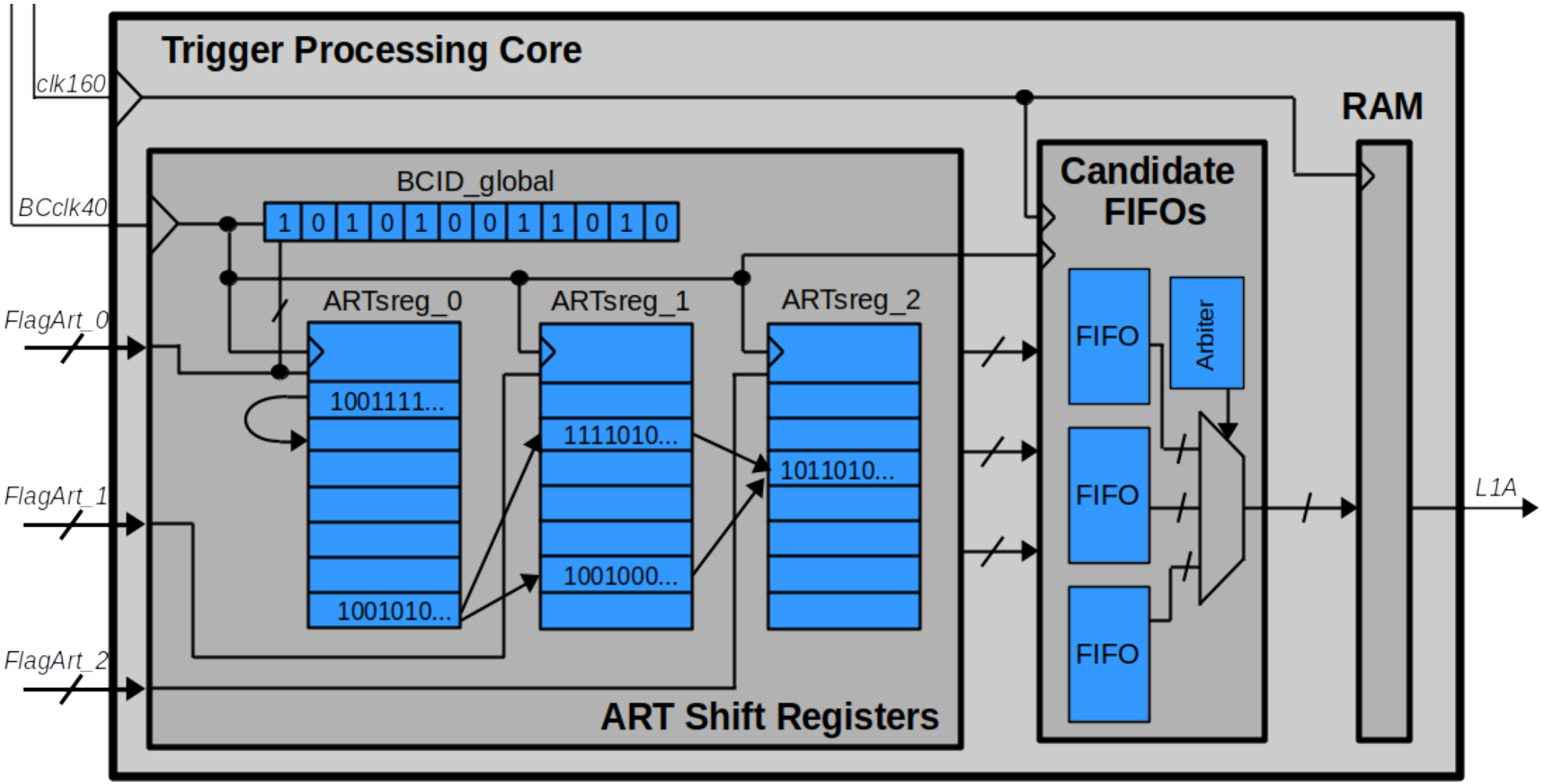
→ In the testbeam the particles arrive randomly with respect to the reference clock of the DAQ. No t0. How do we work with angled tracks?

The **solution** is to cherry-pick scintillator triggers in the microDAQ trigger logic. **Only** the scintillator coincidences whose rising-edges **coincide** with the rising-edge of the CKBC (with a ~500ps uncertainty) are accepted as triggers. Thus leading to a synchronous system

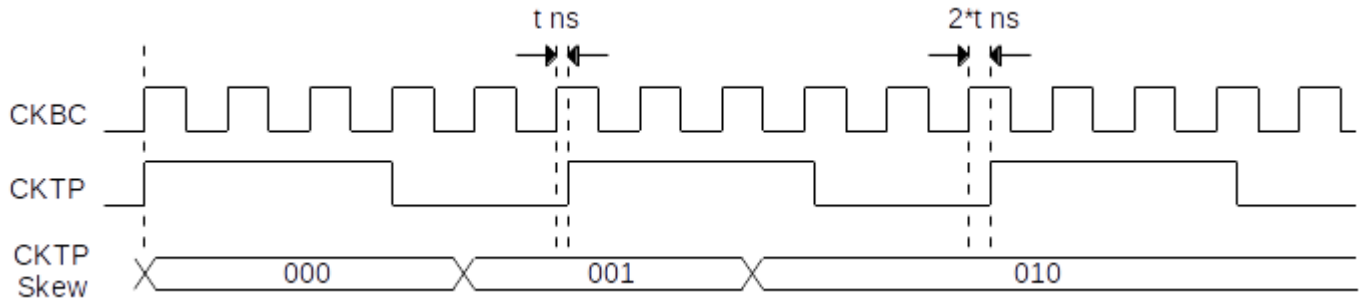




microDAQ TrigProc



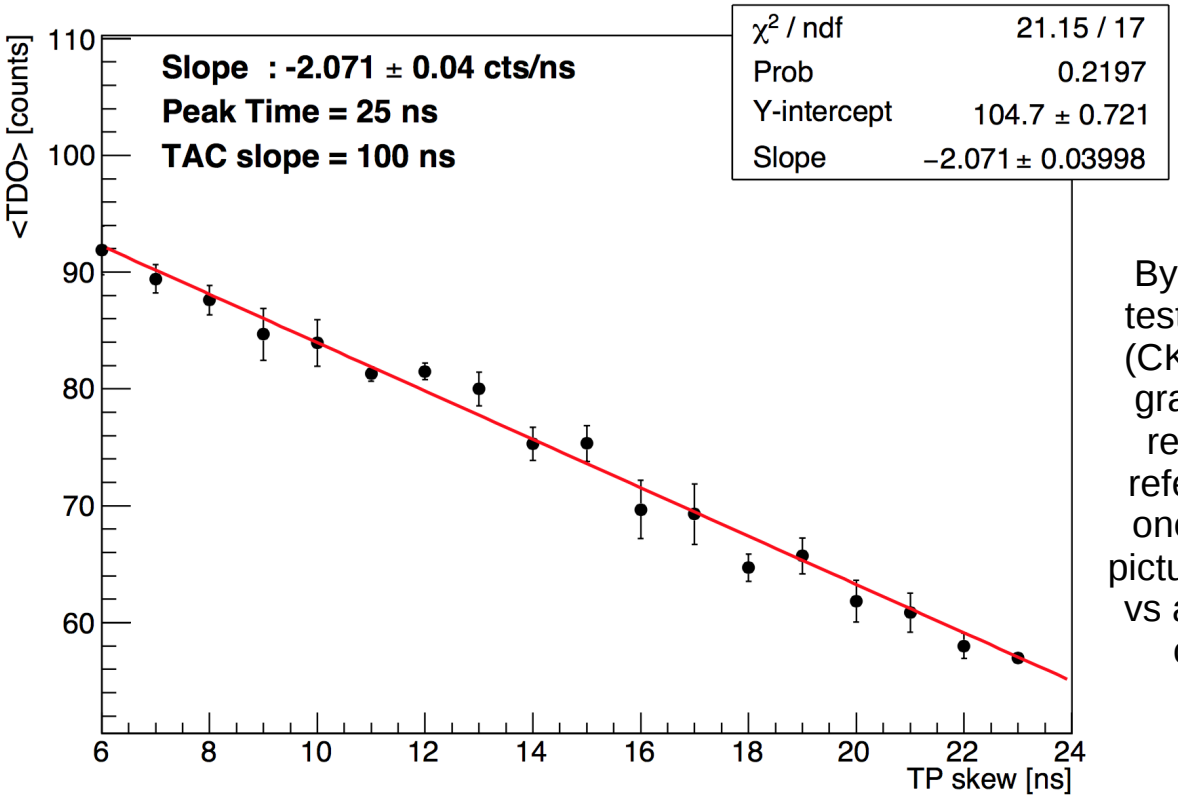
TDO Calibration



t = 1ns

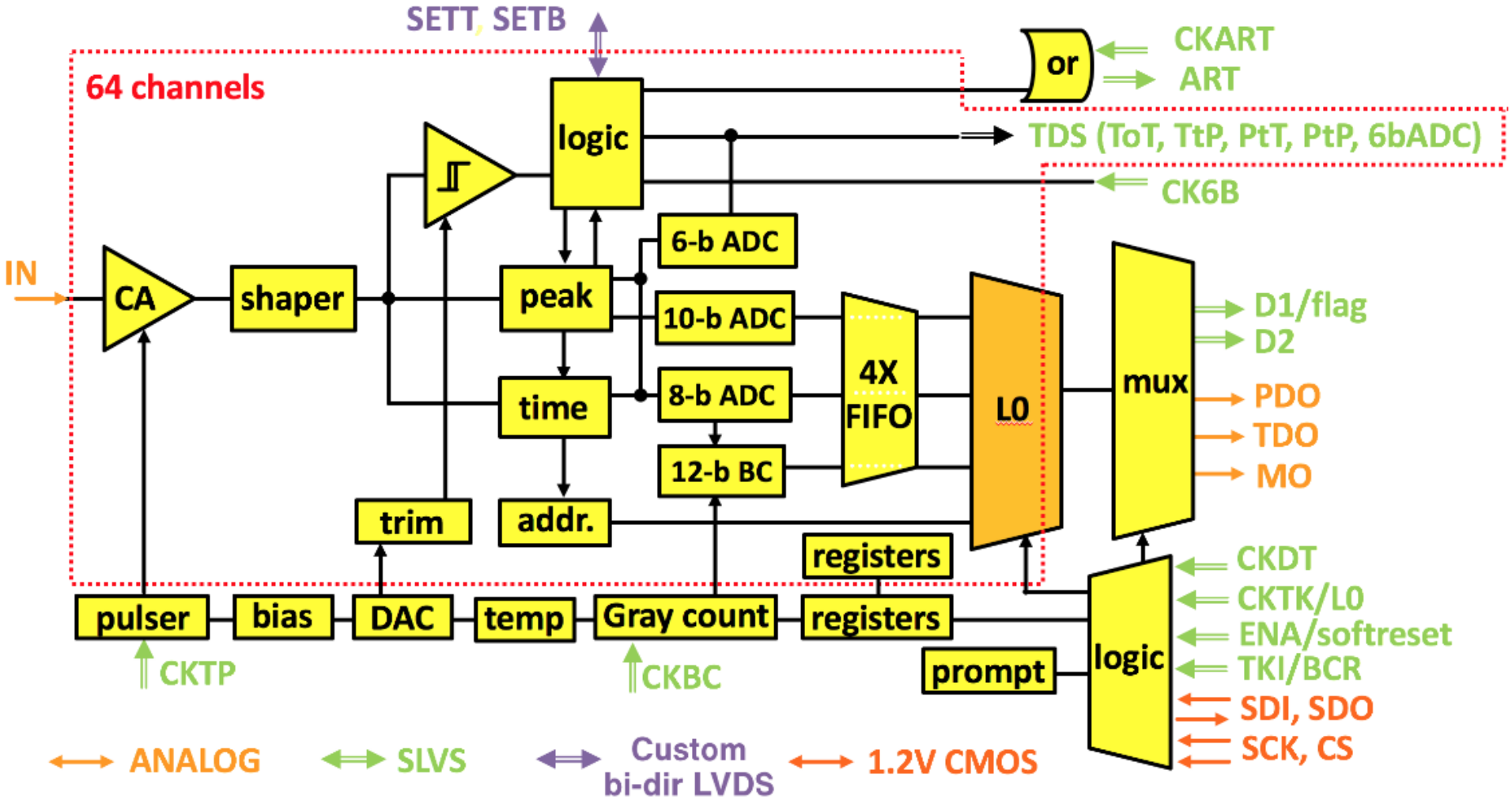
Calibration

- Embedded FPGA ADC (xADC) allows for calibration of VMM's DAC modules (e.g. threshold set)
- Test-Pulse (CKTP) issuer injects test pulses to the VMM. Calibrates the VMM's pulse height response ADC (PDO) and its timing response ADC (TDO)
  - Can skew CKTP wrt CKBC with **1ns granularity**



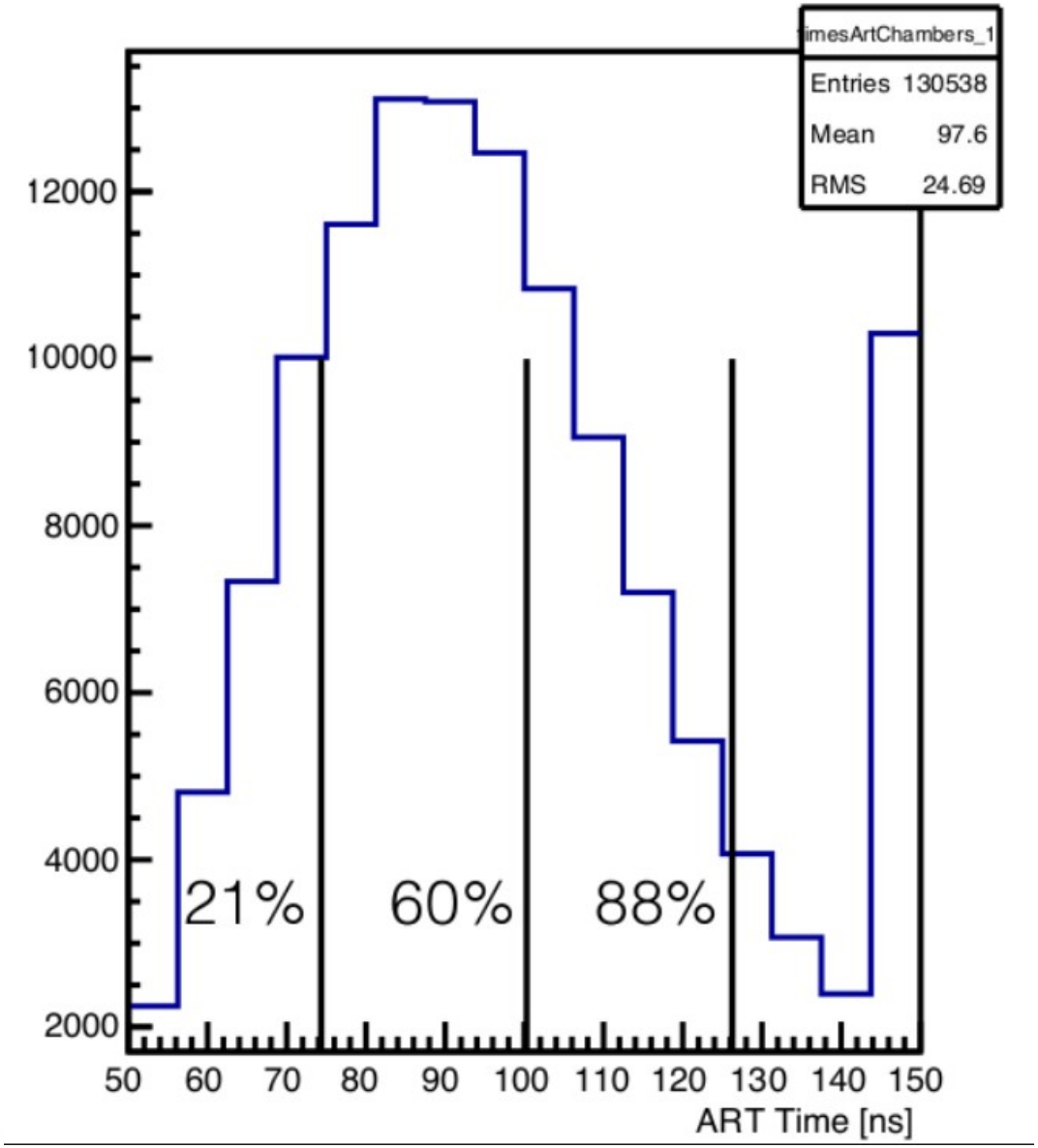
By skewing the test-pulse signal (CKTP) with 1ns granularity with respect to the reference clock, one has a clear picture of the TDO vs absolute-time correlation

VMM Block Diagram



ART Time Distribution

MM and VMM ASIC



Most of the ART data arrive within 4-5 BCs → hence the 5xBC time cut in the microDAQ TP

L0 Readout Window (x8 BCs) > ART time span in MM