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ATLAS NSW Micromegas Test-Beam System

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The LHC at CERN plans to have a series of upgrades to increase its instantaneous luminosity to 7.5×10^{34} cm^{-2}s^{-1}. The ATLAS experiment will upgrade its inner end-cap muon chambers to cope with the increased collision rate expected from the High-Luminosity-LHC. This project, called New Small Wheel, includes resistive Micromegas chambers together with small-strip Thin Gap Chambers (sTGC), conforming a system of ~2.4 million readout channels in total. This is the first time that large Micromegas are built in such a scale. In total, 128 Micromegas modules up to 3 m2 in size, and from different production sites spread in Europe, will be produced, with target installation at the end of Long Shutdown 2 (LS2) of the LHC. A series of test-beam runs have been conducted to test and validate large scale micromegas modules. One of the first series modules in muon/pion beam at the H8 line of SPS.

The experimental setup includes a DAQ system, DCS system based on WinCC-OA for the monitoring and control of HV and monitoring the environmental parameters. A set of Scintillators are used as a trigger system and a series of small size micromegas served as an external reference tracker.

The Micromegas DAQ system (in short: microDAQ) is comprised of one Xilinx VC709 evaluation board that supervises the front-end boards and up to eight VMM/FPGA-bearing front-end boards that can connect to a large Micromegas chamber, or small Micromegas chambers used for tracking. The system is easily scalable and easy to deploy. It is fully compatible with VERSO software process on the back-end, and its main usage is for testbeam and cosmic data-taking applications. Monitoring panels that are integrated with VERSO and on-the-fly analysis tools can be used, in order to verify the quality of the setup. Using the CTF module, one can input an external trigger (i.e. scintillator coincidence) to the DAQ system, which can support rigger rates of up to several hundred kHz without loss of events. For a chamber that has no inclination with respect to the beam, all triggers are accepted. For an inclined setup, where the exact timing of the incident particle must be constrained somehow in order to facilitate track reconstruction, a synchronous-to-BC clock mode is used, which vetoes triggers that are not within ~1.6ns of the rising-edge of the BC clock. This simulates the behavior of the LHC machine, where the timing of an incident particle is well-defined with respect to the BC clock. Finally, the system supports a stand-alone, self-triggered mode, that does not use an external trigger to initiate the readout. In this mode, the VMM's Address in Real Time (ART) stream is analyzed by the VC709, in which a trigger processor has been implemented and upon the detection of a coincidence, injects a trigger to the front-end boards to read the VMMs out.

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