INFN - Padova
michele.michelotto at pd.infn.it

From Westmere to Magny-cours: Hep-Spec06
Lisboa, Hepix Spring ‘10

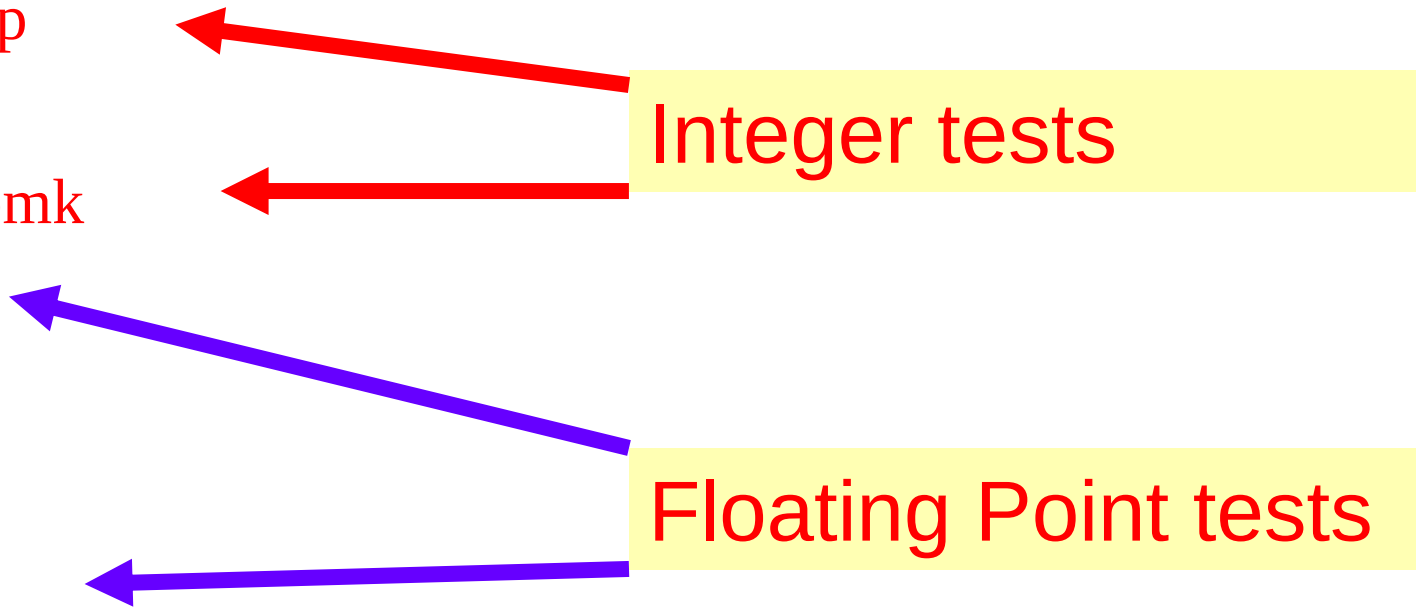
Processor Available

- Magny Cours and Westmere now available
- I'll show some preliminary result

CPU	Westmere Gulftown	Nehalem Beckton	Magny Cours	Lisbon
process	32 nm	45 nm	45 nm	45 nm
est GHz at launch	3.33++	2.26++	2.2	2.8
Cores & caches	6 cores 12 MB L3	8 cores 24 MB L3	12 cores 12 MB L3	6 cores 6 MB L3
Net DDR3 ch / socket	3	8	4	2
market	Mid-to-high end	Ultra high end	High end	Mid-to-high end
Perf per core est avg	1 x	0.7 x	0.55 x	0.75x

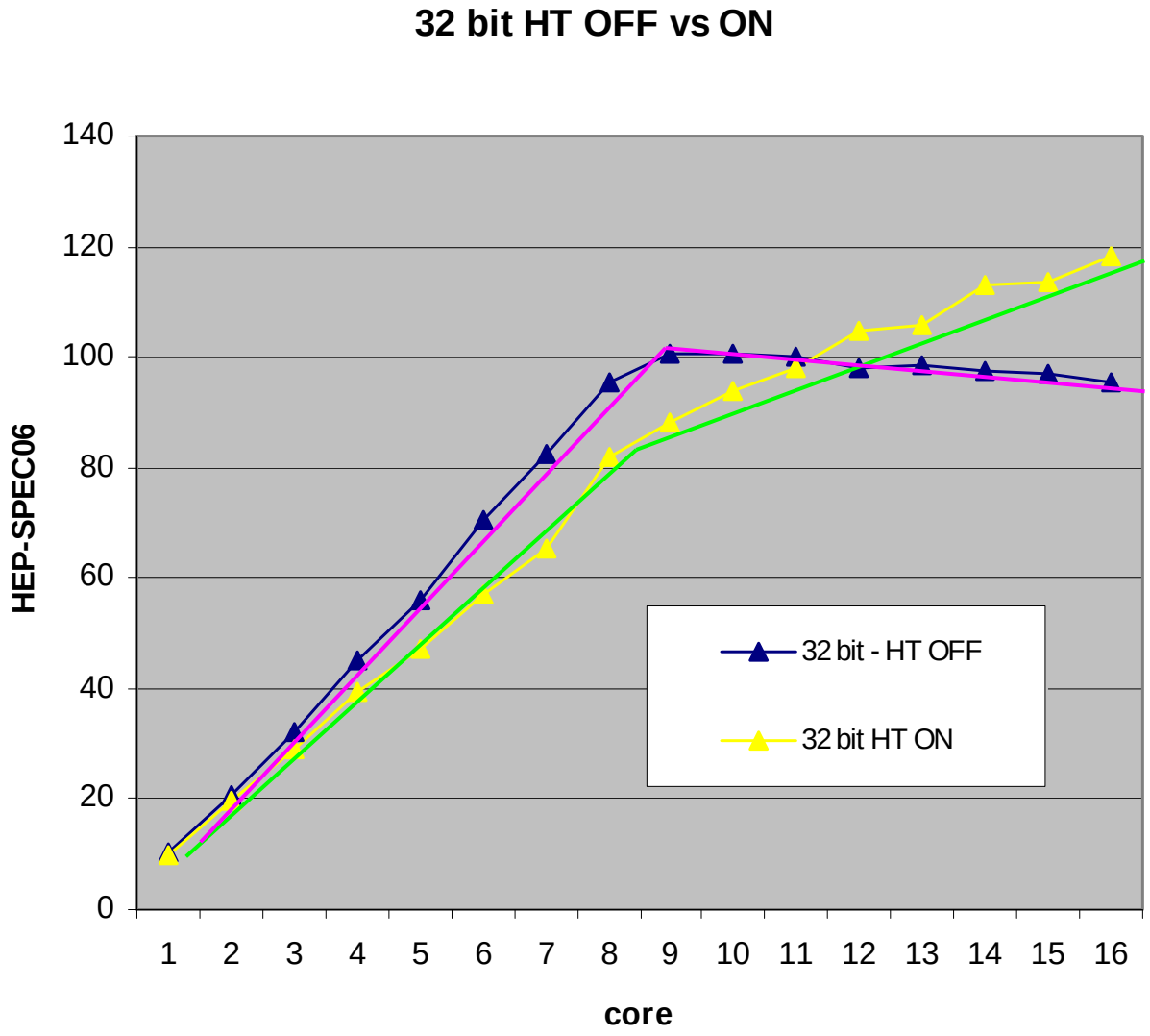
HEP-SPEC06

- 471.omnetpp
- 473.astar
- 483.xalancbmk
- 444.amd
- 447.dealII
- 450.soplex
- 453.povray



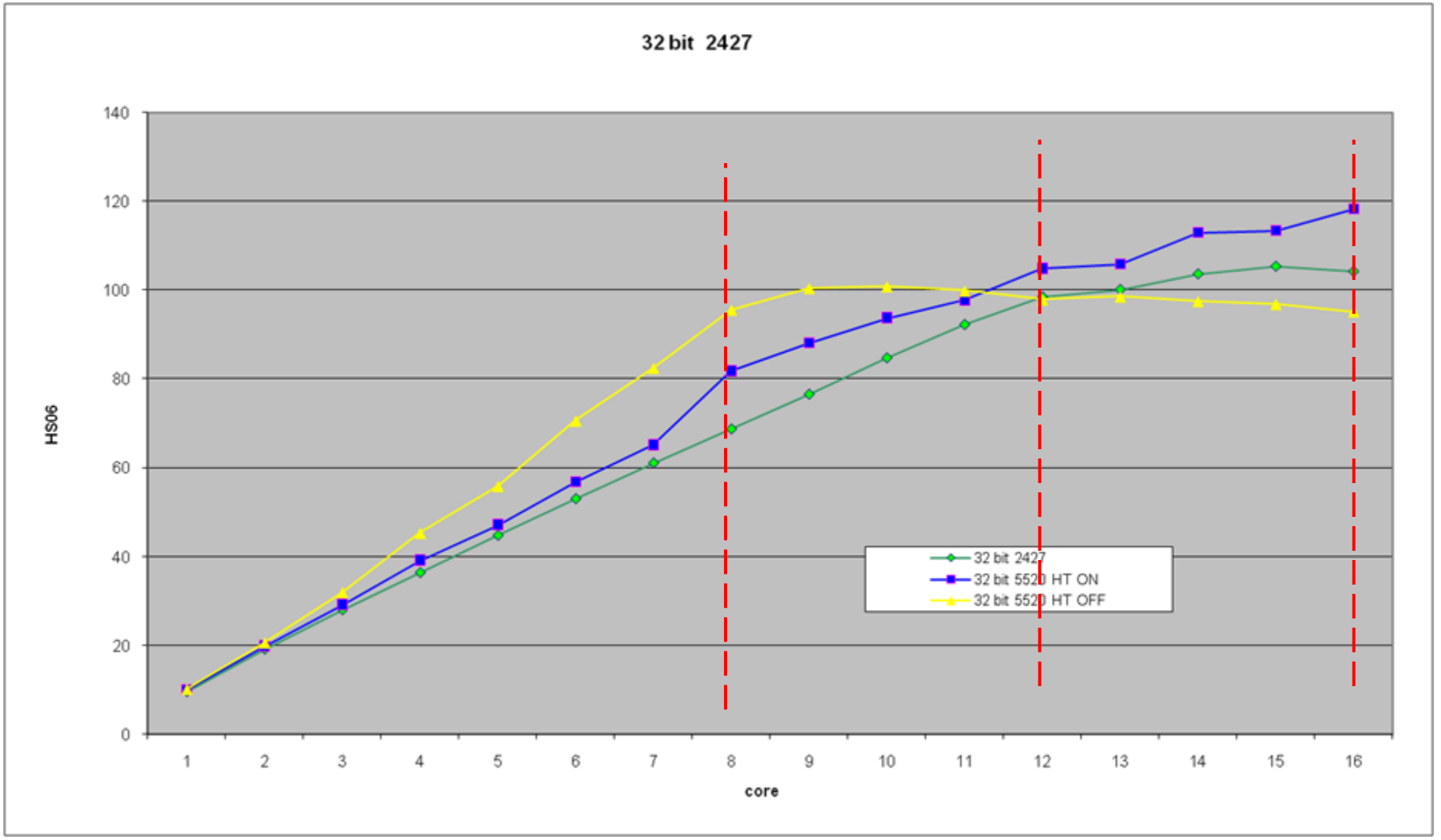
- Geometric average on 7 tests. Sum on all cores
- Sum on all Worker nodes

5520 32 bit - HT ON/OFF

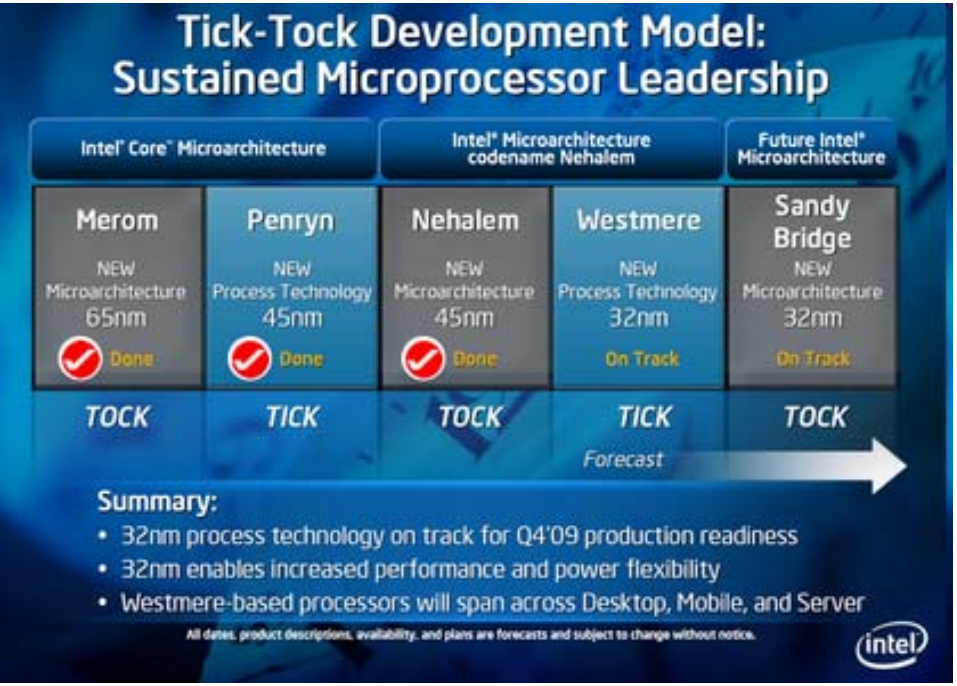


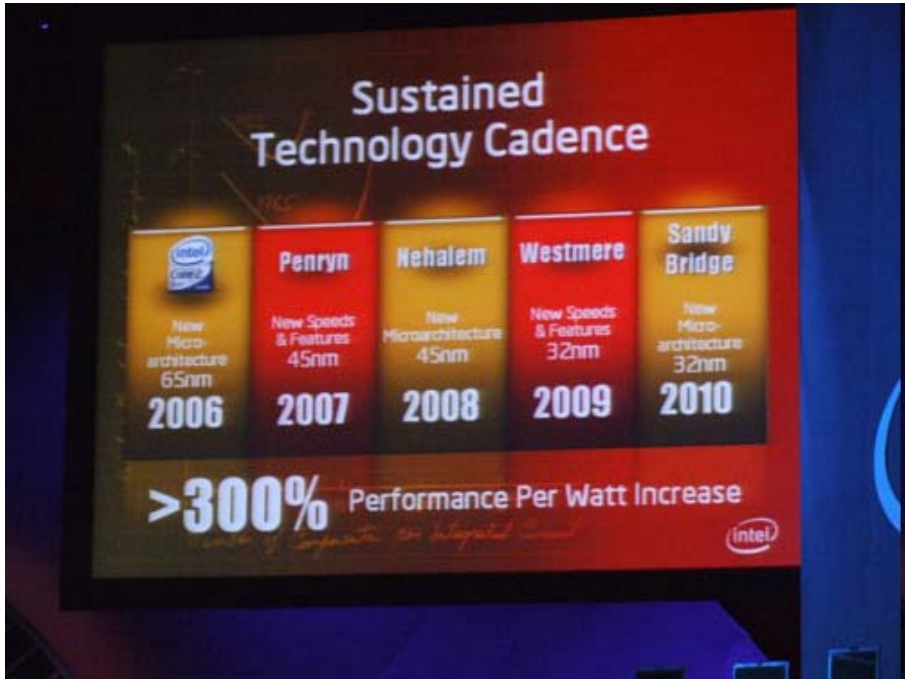
HT ON:81.81
HT OFF: 95.96
HT OFF is better up to 11concurrent run

5520(2266) vs 2427(2200)



Tick Tock


Tick-Tock Development Model:
Sustained Microprocessor Leadership
Intel® Core™ Microarchitecture
Intel® Microarchitecture codename Nehalem
Future Intel® Microarchitecture
Merom
NEW Microarchitecture
65nm
Done
Penryn
NEW Process Technology
45nm
Done
Nehalem
NEW Microarchitecture
45nm
Done
Westmere
NEW Process Technology
32nm
On Track
Sandy Bridge
NEW Microarchitecture
32nm
On Track
TOCK
TICK
TOCK
TICK
TOCK
Forecast
Summary:
• 32nm process technology on track for Q4'09 production readiness
• 32nm enables increased performance and power flexibility
• Westmere-based processors will span across Desktop, Mobile, and Server
All dates, product descriptions, availability, and plans are forecasts and subject to change without notice.
intel

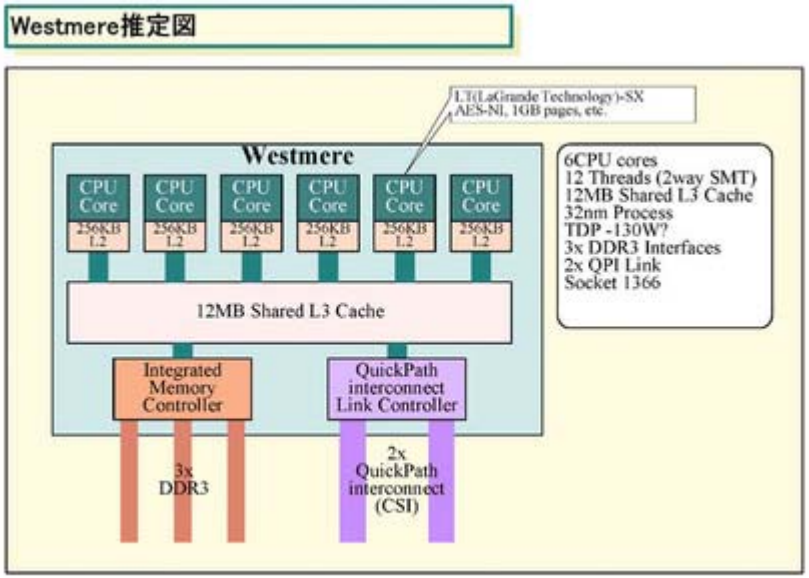

Sustained
Technology Cadence
New Micro-architecture
65nm
2006
Penryn
New Speeds & Features
45nm
2007
Nehalem
New Microarchitecture
45nm
2008
Westmere
New Speeds & Features
32nm
2009
Sandy Bridge
New Micro-architecture
32nm
2010
>300% Performance Per Watt Increase
intel

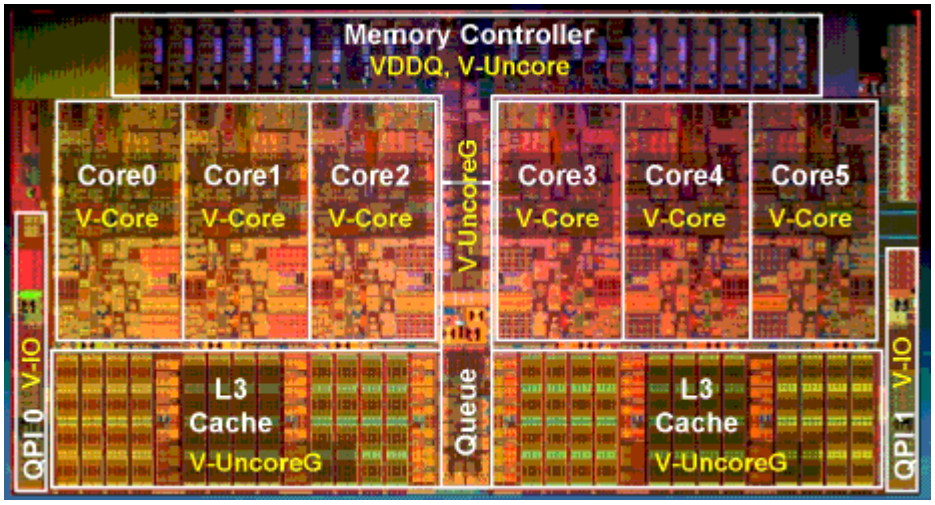
Westmere DP

- 16 March 2010 first release of Xeon DP on Westmere 32nm

model	Cores/threads	L3 cache	Clock with Turbo Mode Off	TDP
X5680	6/12	12 MB	3.33 GHz	130 W
X5670	6/12	12 MB	2.93 GHz	95 W
X5660	6/12	12 MB	2.80 GHz	95 W
X5650	6/12	12 MB	2.66 GHz	95 W
L5640	6/12	12 MB	2.26 GHz	60 W
X5677	4/8	12 MB	3.46 GHz	130 W
X5667	4/8	12 MB	3.06 GHz	95 W
E5640	4/8	12 MB	2.66 GHz	80 W
E5630	4/8	12 MB	2.53 GHz	80 W
E5620	4/8	12 MB	2.40 GHz	80 W
L5630	4/8	12 MB	2.26 GHz	40 W

Westmere 56xx

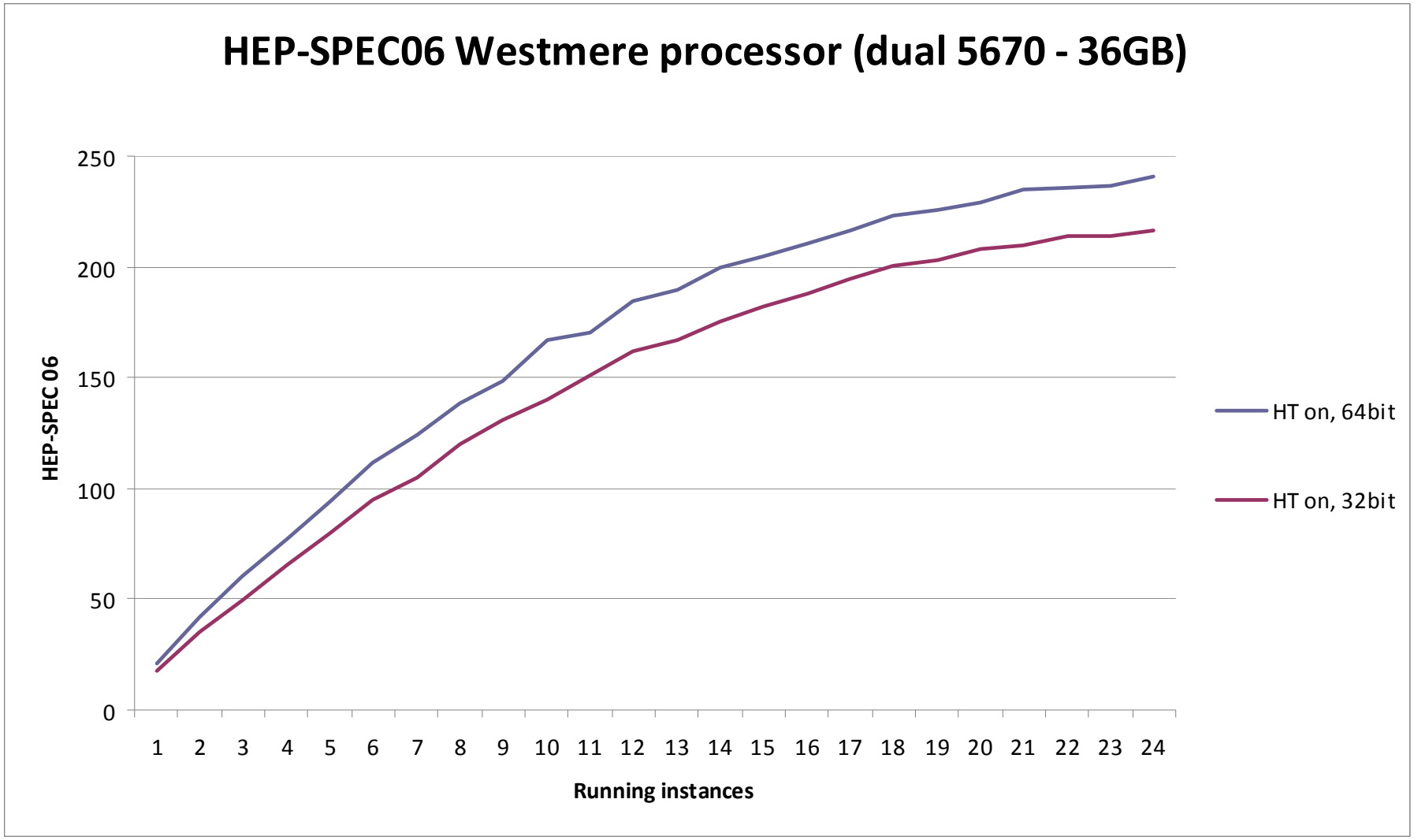




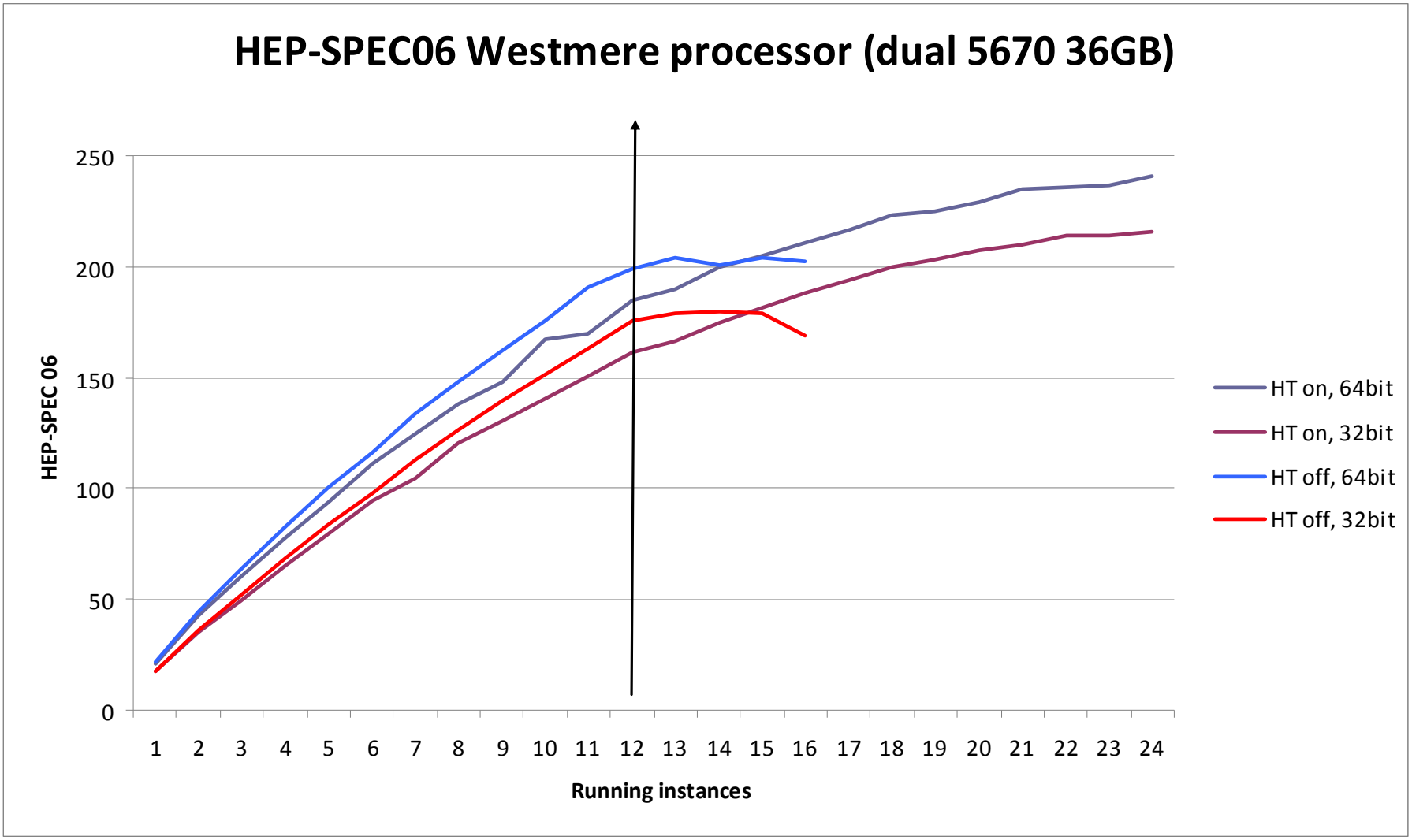
Thanks

- Thanks to Andrea Chierici from the Farming Group at CNAF – INFN Tier1 in Bologna for measurements on Intel Westmere
- Thanks to AMD for the access to a 2x6174 in Munich

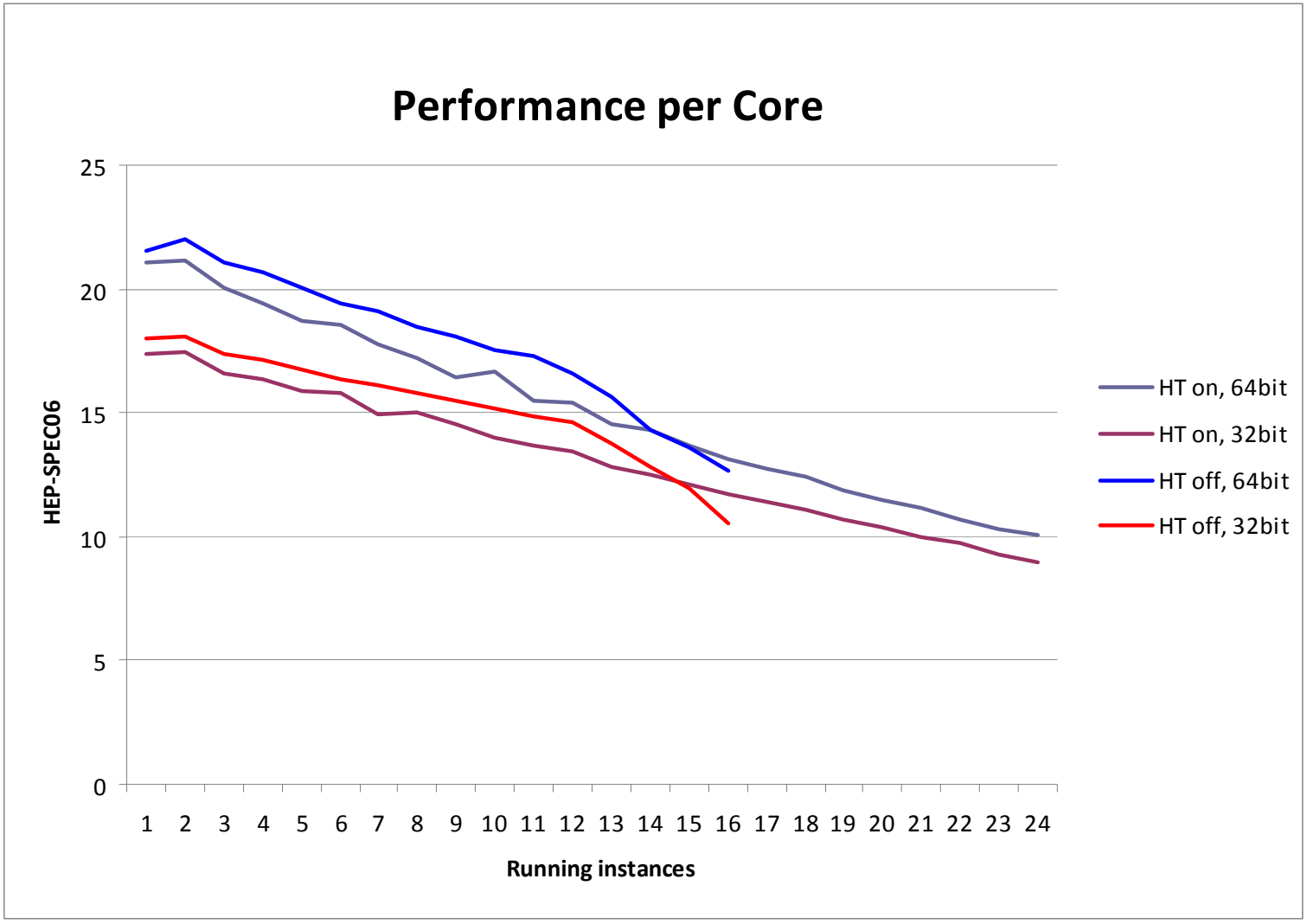
5670 64 bit vs 32 bit



5670 HT-ON or OFF



HS06 per core



AMD Magny-Cours 61xx

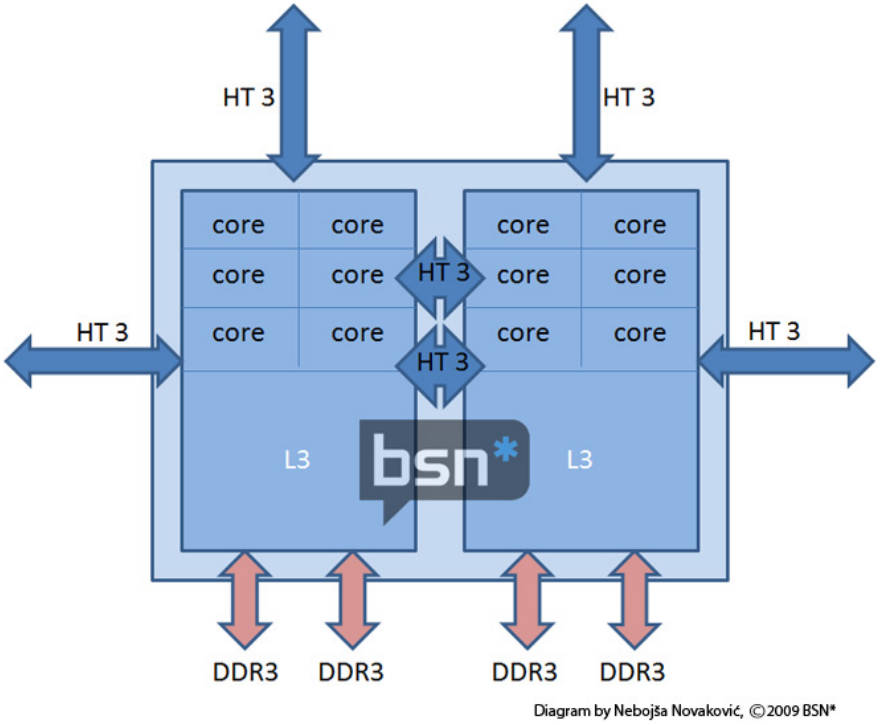
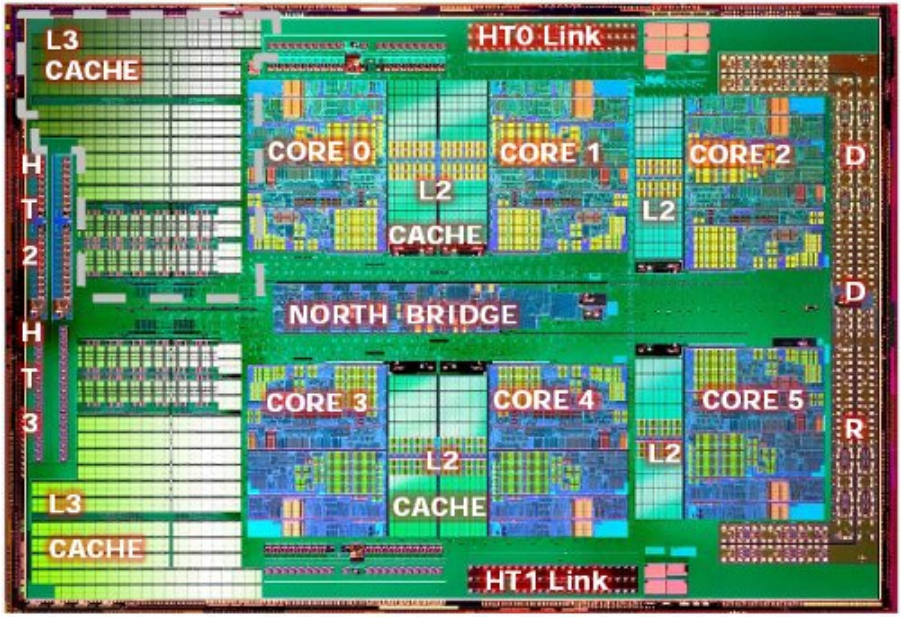
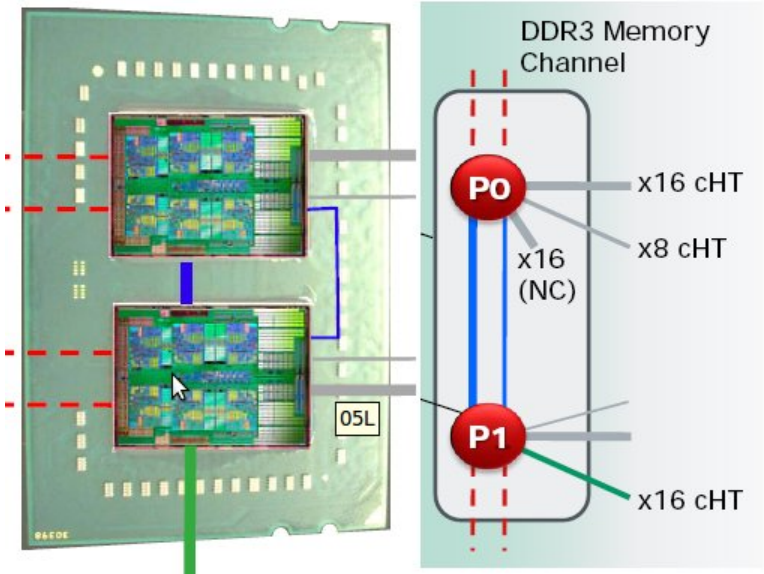


Diagram by Nebojša Novaković, ©2009 BSN*

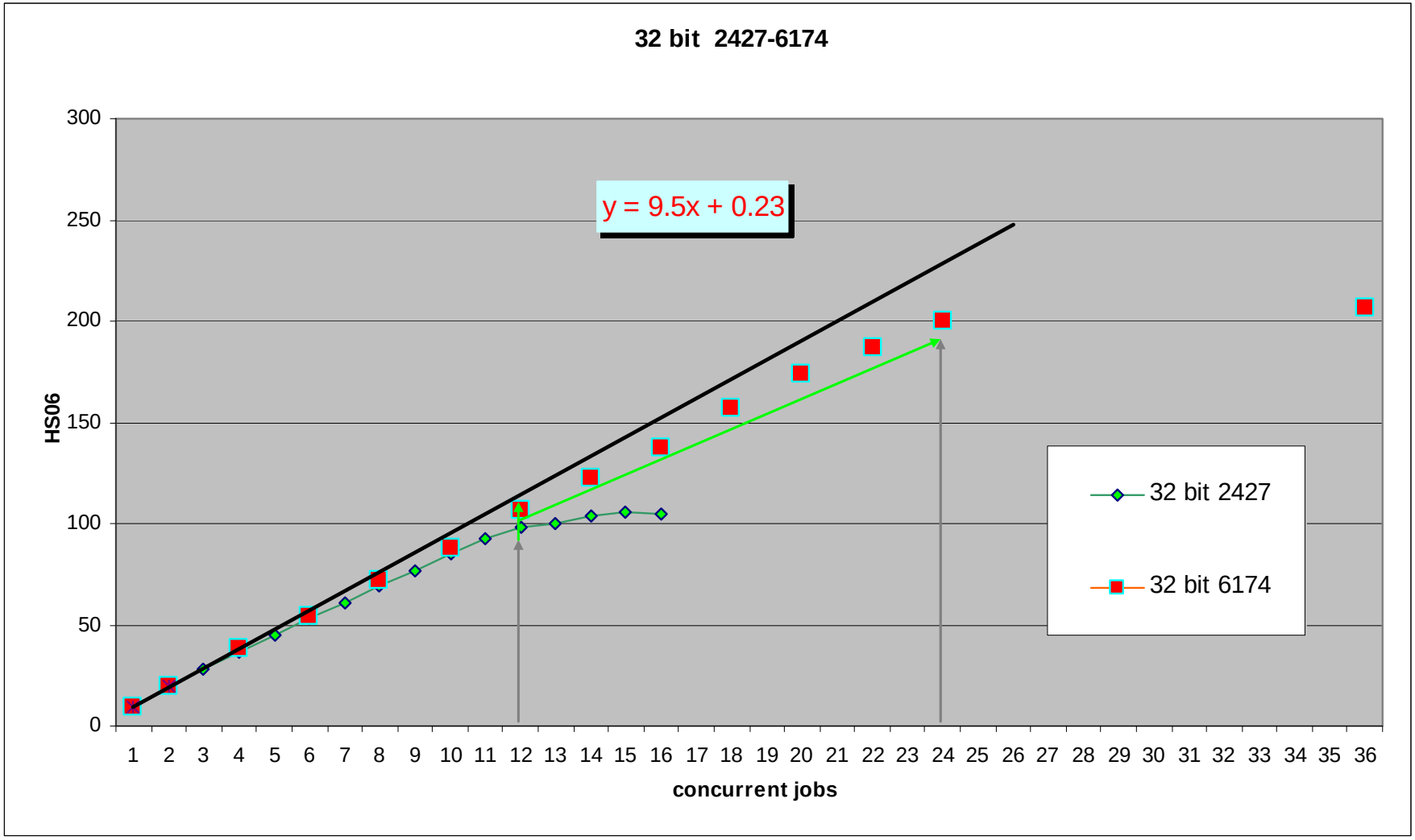




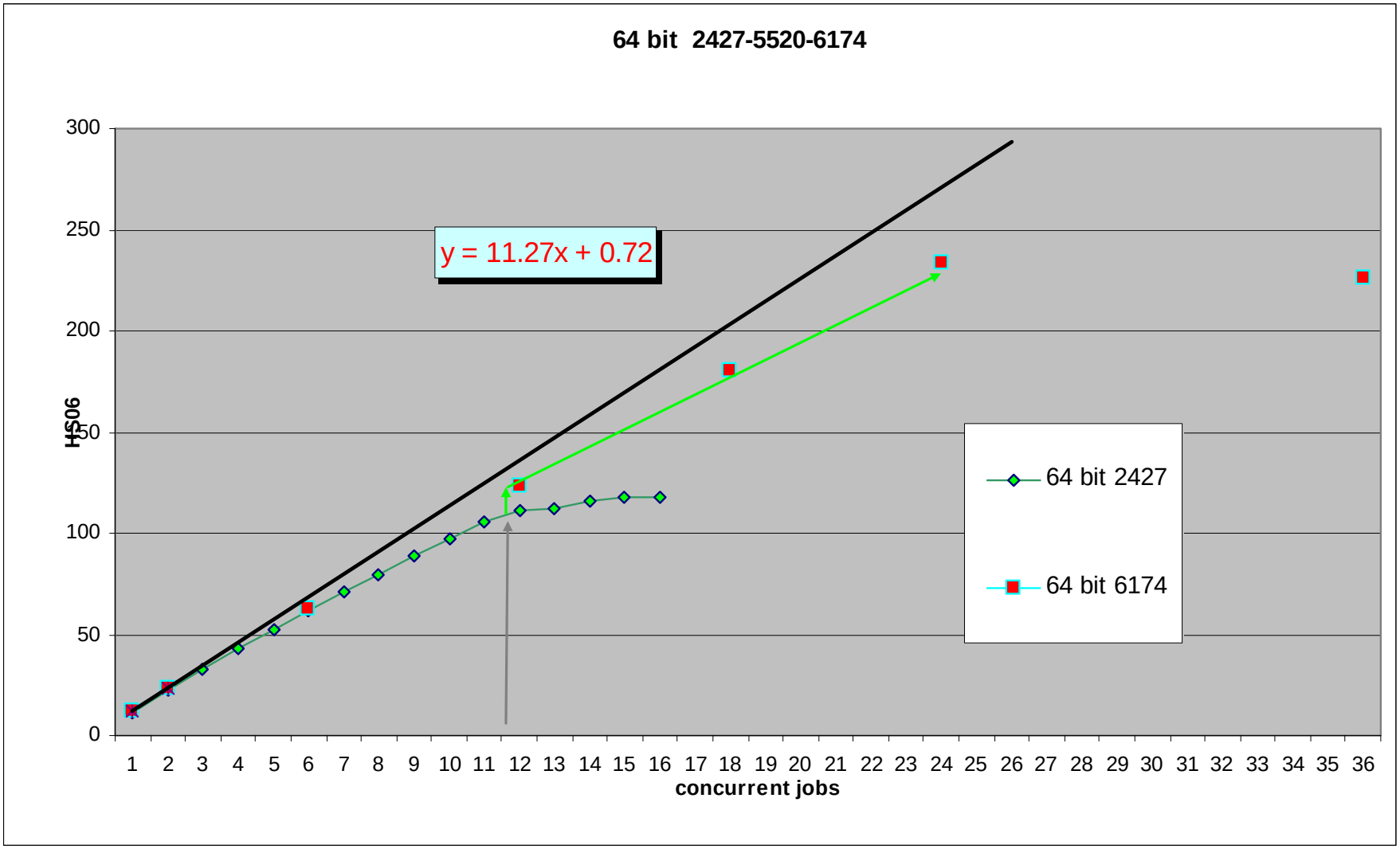
Magny-Cours

model	Cores/threads	L3 cache	Clock	ACP
Xeon 5670	6/12	12 MB	2.93 GHz	95 W
6124 HE	8/8	12 MB	1.8 GHz	65 W
6128	8/8	12 MB	1.8 GHz	80 W
6128 HE	8/8	12 MB	2.0 GHz	65 W
6134	8/8	12 MB	2.3 GHz	80 W
6136	12/12	12 MB	2.4 GHz	80 W
6164 HE	12/12	12 MB	1.7 GHz	65 W
6168	12/12	12 MB	1.9 GHz	80 W
6172	12/12	12 MB	2.1 GHz	80 W
6174	12/12	12 MB	2.2 GHz	80 W
6176 SE	12/12	12 MB	2.3 GHz	105 W

6174 (2.2 GHz) 64 GB 32bit



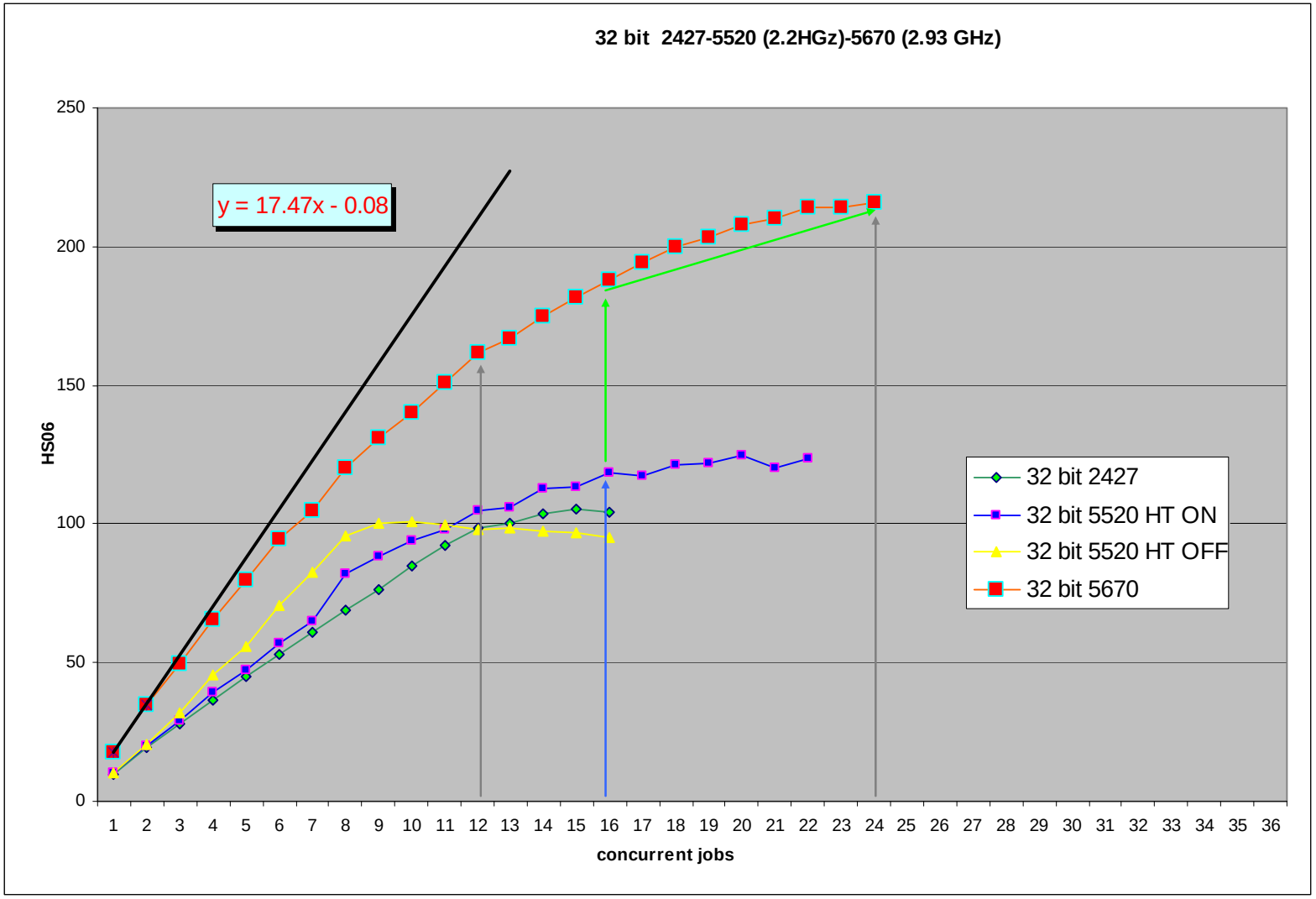
6174 64 bit


64 bit 2427-5520-6174
y = 11.27x + 0.72
HS06
concurrent jobs
64 bit 2427
64 bit 6174
0
50
100
150
200
250
300
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36

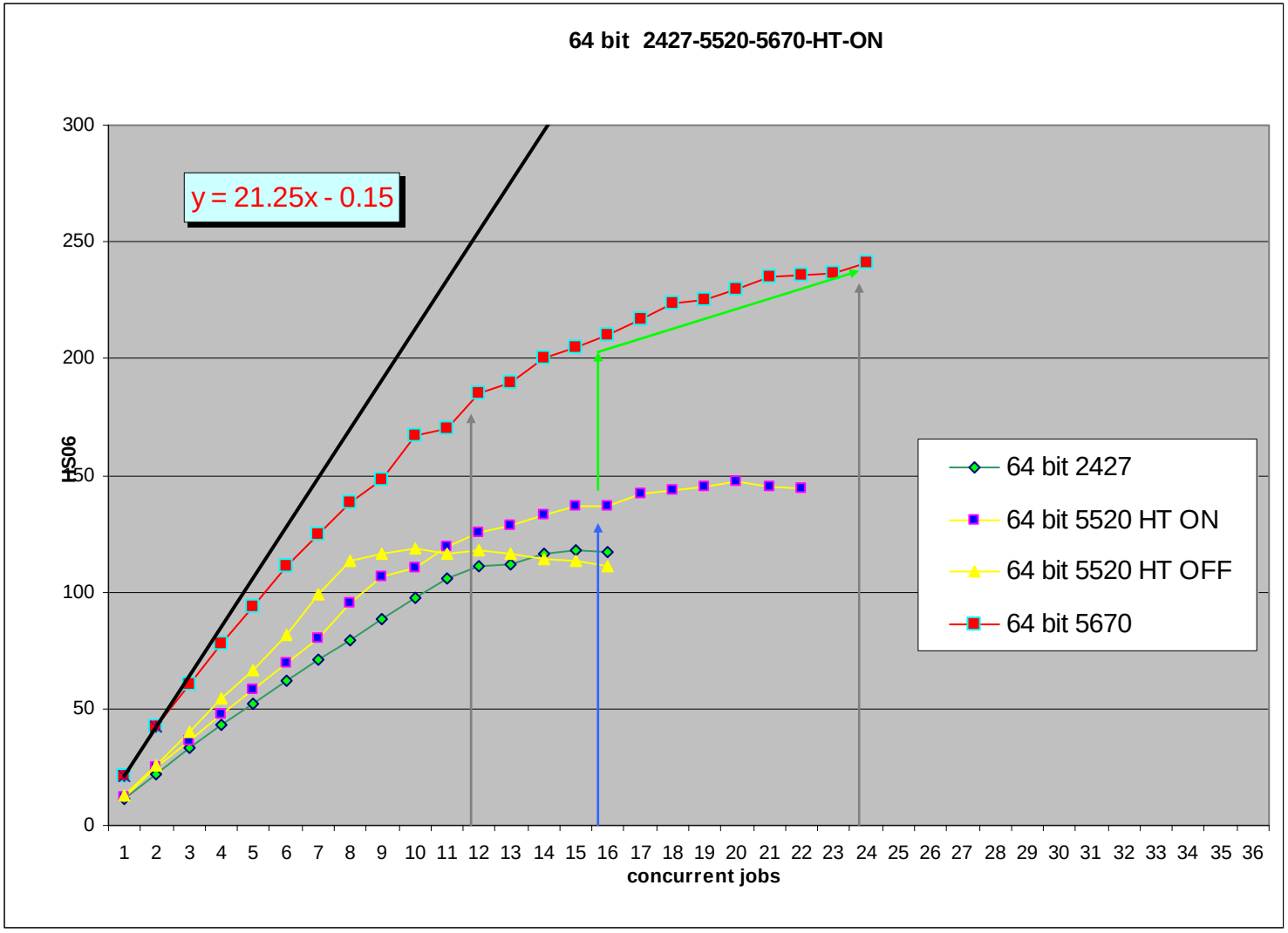
From 2009 to 2010

- Intel moved Nehalem to Westmere
  - From 45 nm to 32 nm
  - From 4-core/8 logical cpu to 6core/12cpu
- Amd moved from Instambul to Magny-Cours
  - From 6 cores to 12 cores

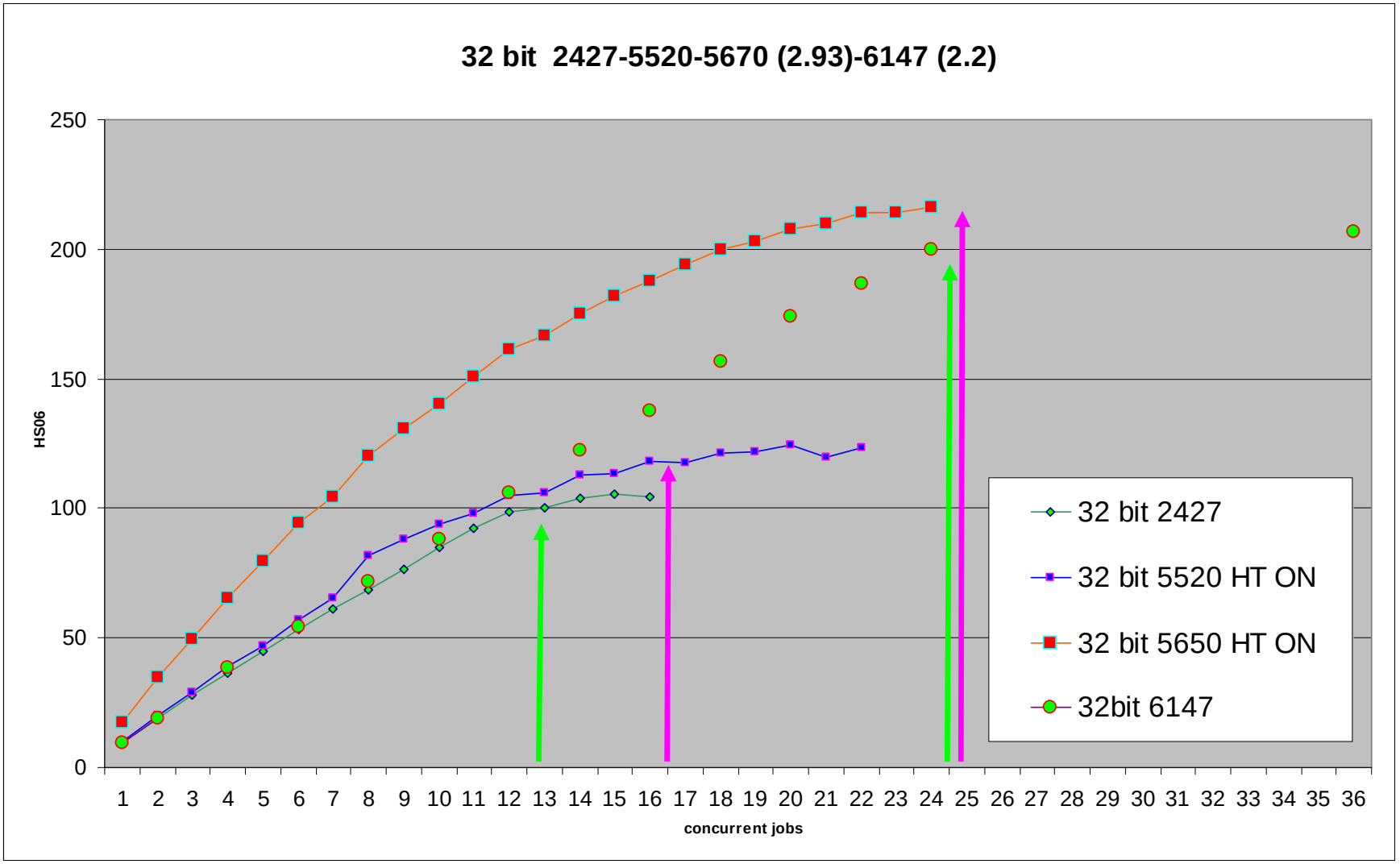
32 bit - 5520 (2.2) - 5650 (2.93)



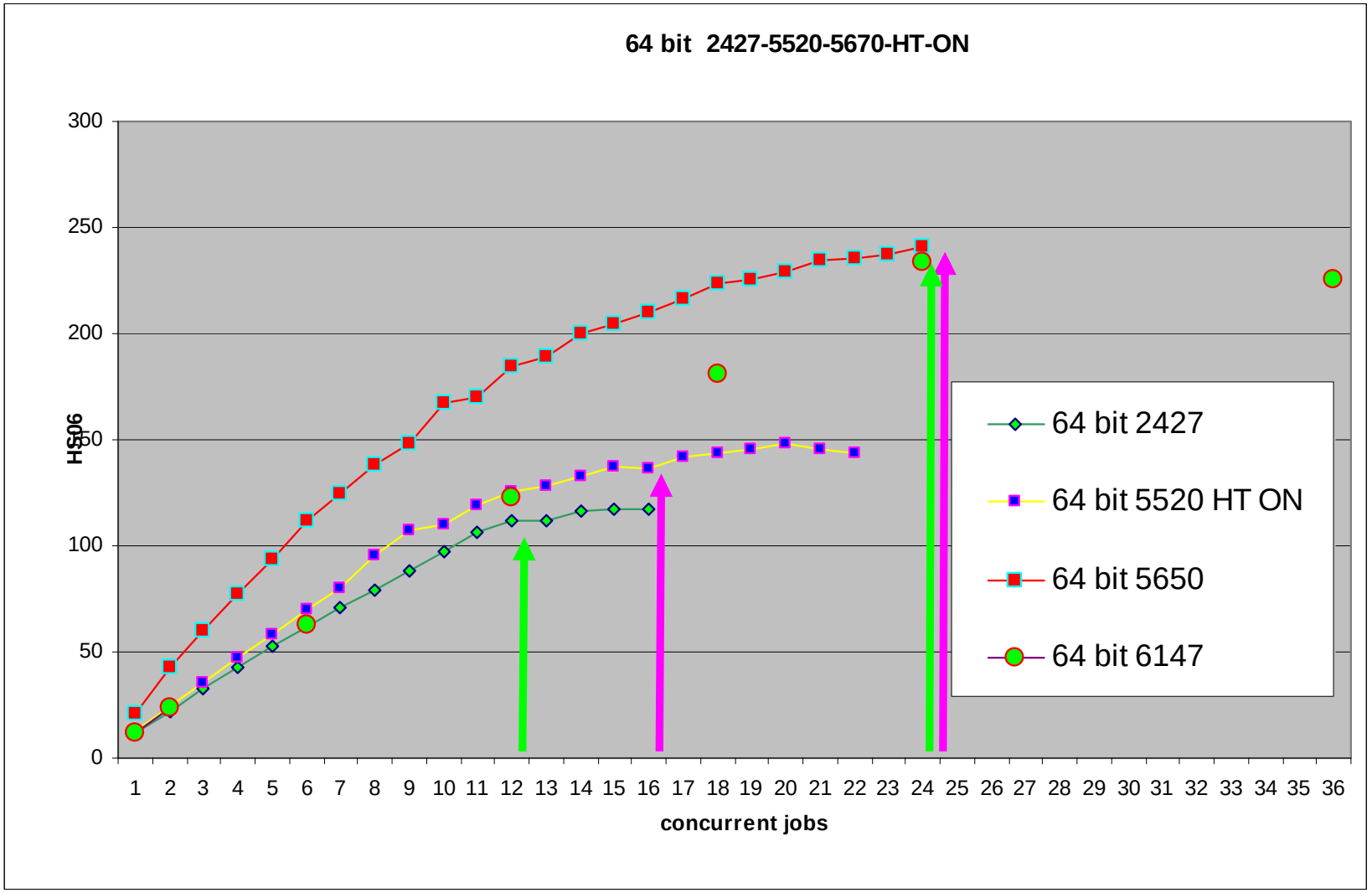
64bit - 5520 (2.2) - 5650 (2.93)



From 12-16 cpu to 24 cpu



From 12-16 cpu to 24 cpu



Questions?