Lessons learned from CMS Phase-1

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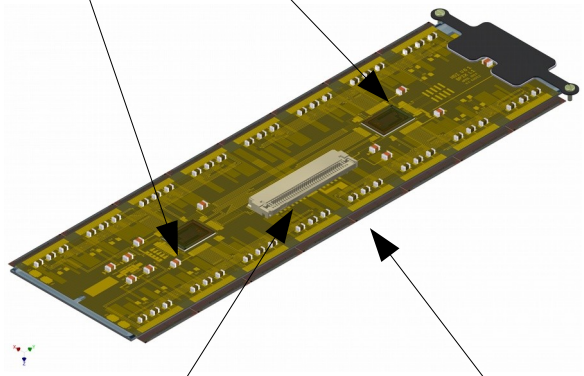
Condensed version of a presentation shown at the module workshop CERN 14 December 2017

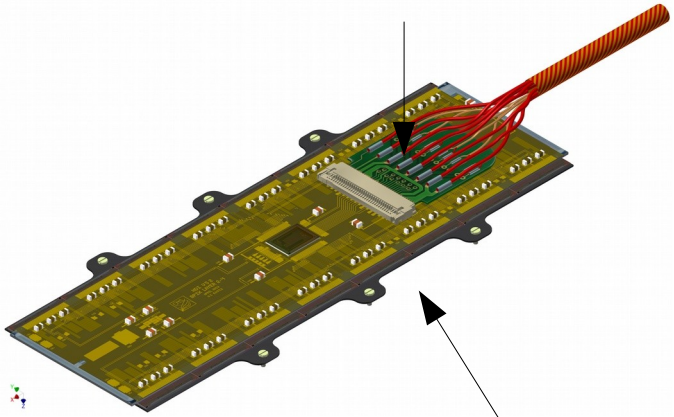
https://indico.cern.ch/event/681678/

Phase 1 Modules

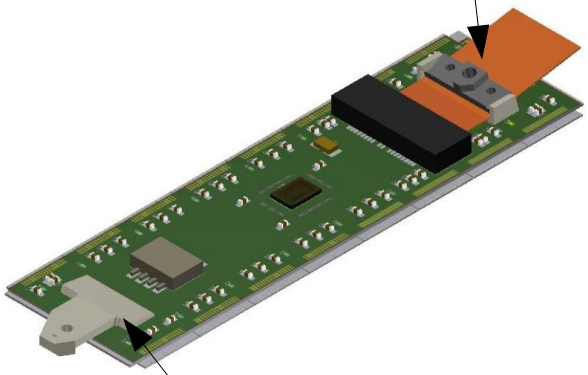
2 TBMs
(output rate)



33 pin connector
1 m long cable
flexible in all direction



Al flat cable
radial routing



39 pin connector
(# links, power)
different cable routing
(space)

no base-strip
(space)

base-strips
(mounting
/safe handling)
1088 modules

clamp
(no neighbour
in this direction)

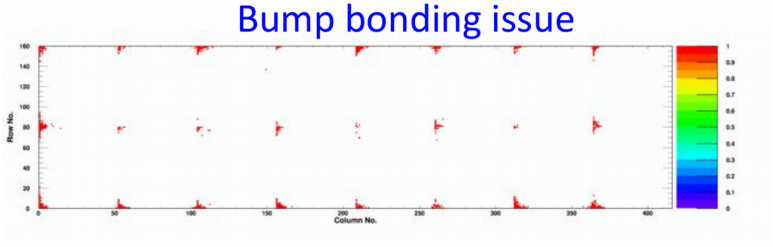
more delicate, but only ~96 modules

Production experience

- ROCs tested on wafer (common for FPIX/BPIX)
  - High yield 93 %
  - Some re-tested after dicing, negligible losses
  - Some of the losses during full module qualification may possibly have been avoidable with more extensive on-wafer testing
- TBMs tested on wafer (common for FPIX/BPIX)
  - retested (brief) after mounting on HDI (BPIX)
- BPIX Sensors tested on wafer (vendor + x-checks),
  - re-tested after dicing / picking 93 % yield
  - Identical vendor / design as in phase 0, no surprises
  - Same sensor for all bpix centers except for metallization material / size and UBM
- FPIX, >95%, one problematic batch (processing mistake), needed higher HV for first 10 fb^{-1}

BPIX Bump-Bonding

- Bare module (ROC+sensors) tested after bump-bonding (probestation)
  - tests sensor IV, ROC functionality, bump-bond yield before full assembly
  - module yield varied between 84 % and 96 %
  - re-work (not done in all centers)
    - 10 - 20% reworked with good yield
    - 4 % not reworkable (sensor IV)



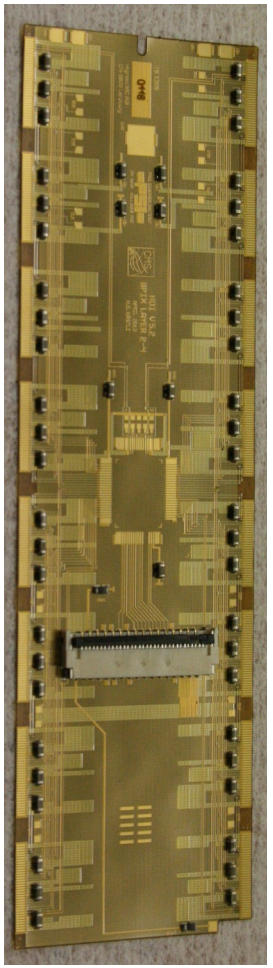
- 5 vendors → > 5 sets of problems
  - Process instability (metallization, surface quality, the unknown)
  - ROC damage (→ rework)
  - IV characteristic changes (few %, not reworkable)
  - Bump yield usually bi-modal (ok or catastrophic, very process dependent)
  - Throughput, availability of material and vendor delayed us more than once

FPIX bump bonding

- Another vendor, another set of problems
- Dicing debris sticking to ROCs
  - Causing shorts, etc, if pushed into ROCs when bump-bonding to sensor
  - initially 70 % of the modules had at least one damaged ROC
  - no bare module test, only detected after full assembly
  - later improved to ~ 20 % by visual inspection before bumping
- A small number of modules had ROCs with large regions of unconnected pixels (1 %)
- A bare module was only used for the very last round of modules with rework presumably would have resulted in much better than 80 % yield

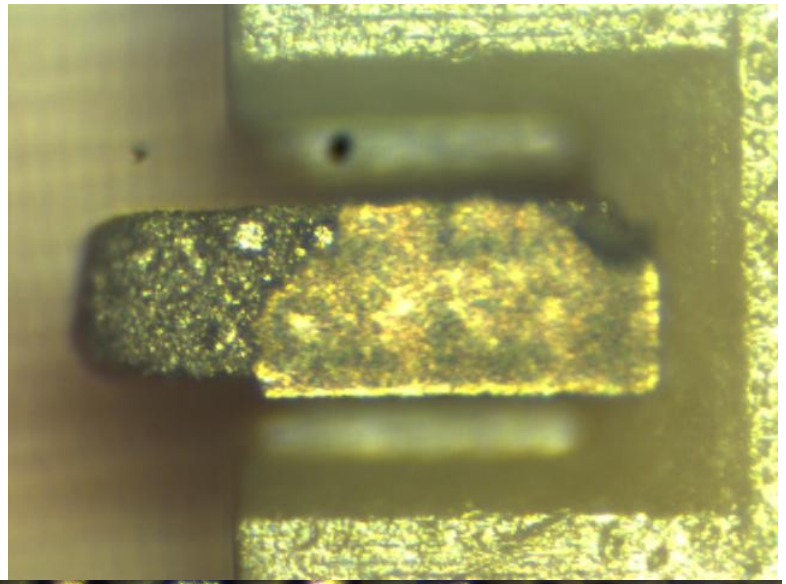
BPIX HDI (“ a recurring nightmare”)

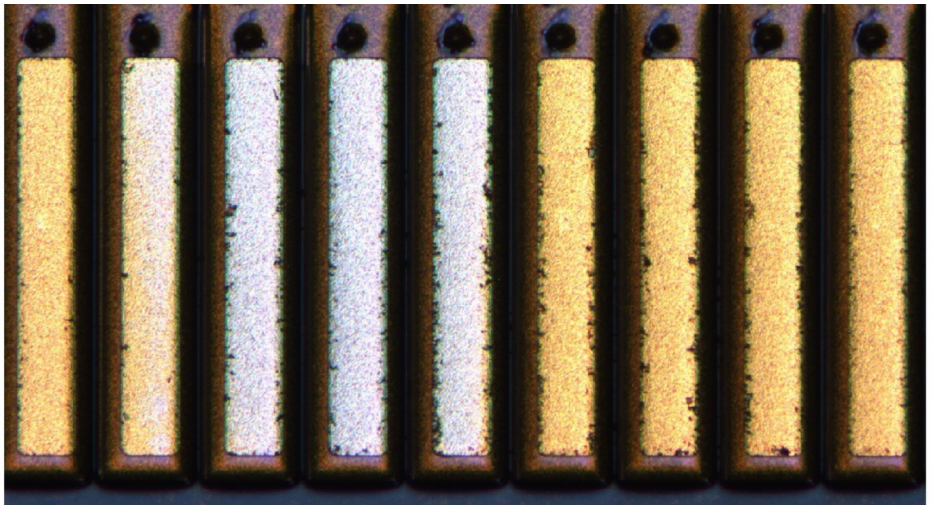
- 3 layer Cu/Kapton, same vendor/ technology as in Phase 0 (several iterations), similar design
- Electrical test by vendor, no electrical faults found in delivered HDIs, some had high resistance
- Optical inspection in production centers
  - surface discoloration
    - Not a problem according to vendor, took back one batch anyway (ended up buying some of it later when we ran out of material)
    - similar problems at a lower rate in other batches accepted
    - impact on bondability varied from center-to-center
      So far, no known losses due to detaching wire-bonds
  - Poor soldering quality
    - some joints not sufficiently heated during reflow (covered by connector)
    - changed procedure (vapor phase), resoldered one batch
    - Subsequent batches with good quality
- Should have been easy, turned into a nightmare, lost a lot of material to tests

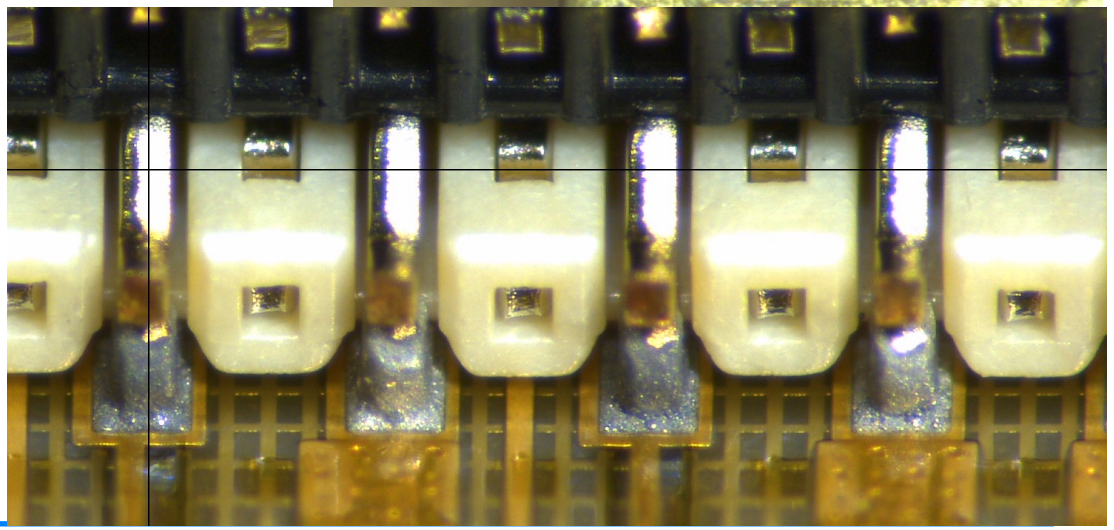


HDIs

- No Problems reported by ATLAS
- nightmares for FPIX and BPIX
  - Tolerances, shorts, surface/wire-bonding, soldering
  - ended up spending a lot of time with visual inspection
  - Lost a lot of material (tests, rejects)

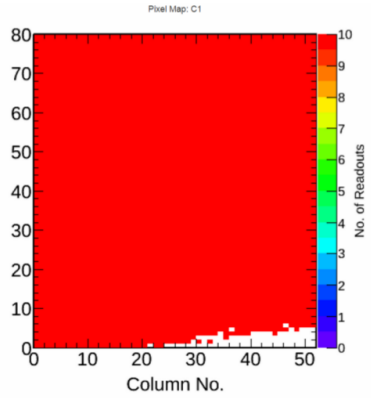


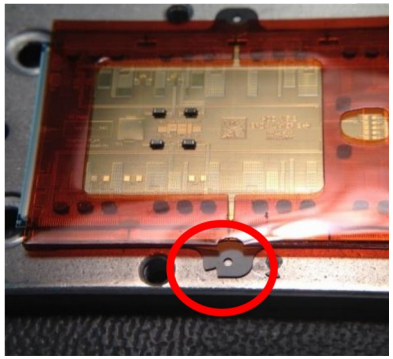




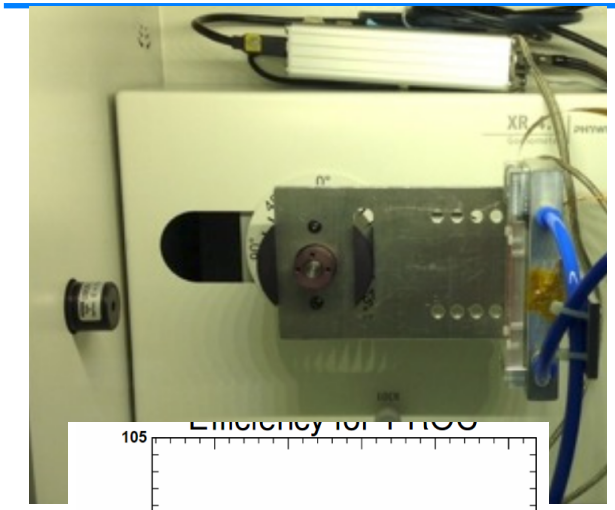
BPIX Module Assembly

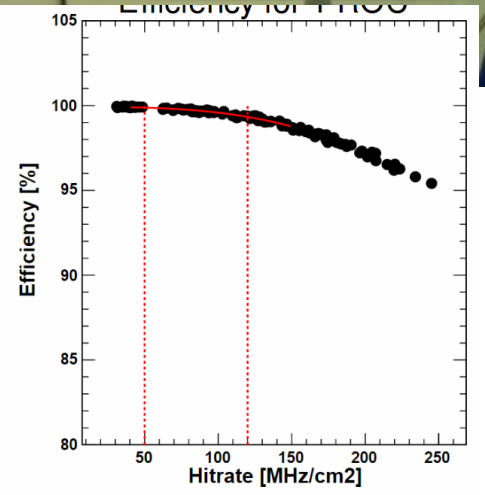
- Semi-manual procedure
- good bare module → installable full module : 76 % yield
  - 65 % .. 85 % (including startup production)
  - > 50 % of the loss due to ROC failures in high rate x-ray test
  - Importance of other loss types varied by center
    - leakage current increase (few % – 40 %)
    - various failures of ROCs with unknown reason
    - localized pixel damage during assembly (one center initially, fixed later)
    - Many others O(1 %):
      Gluing, handling, accidents, HDI soldering failure / connector failure/ /not wire-bondable, broken base-strips
- Overall yield quite a bit lower than expected
- ATLAS IBL experience: expect more handling losses with thinner modules

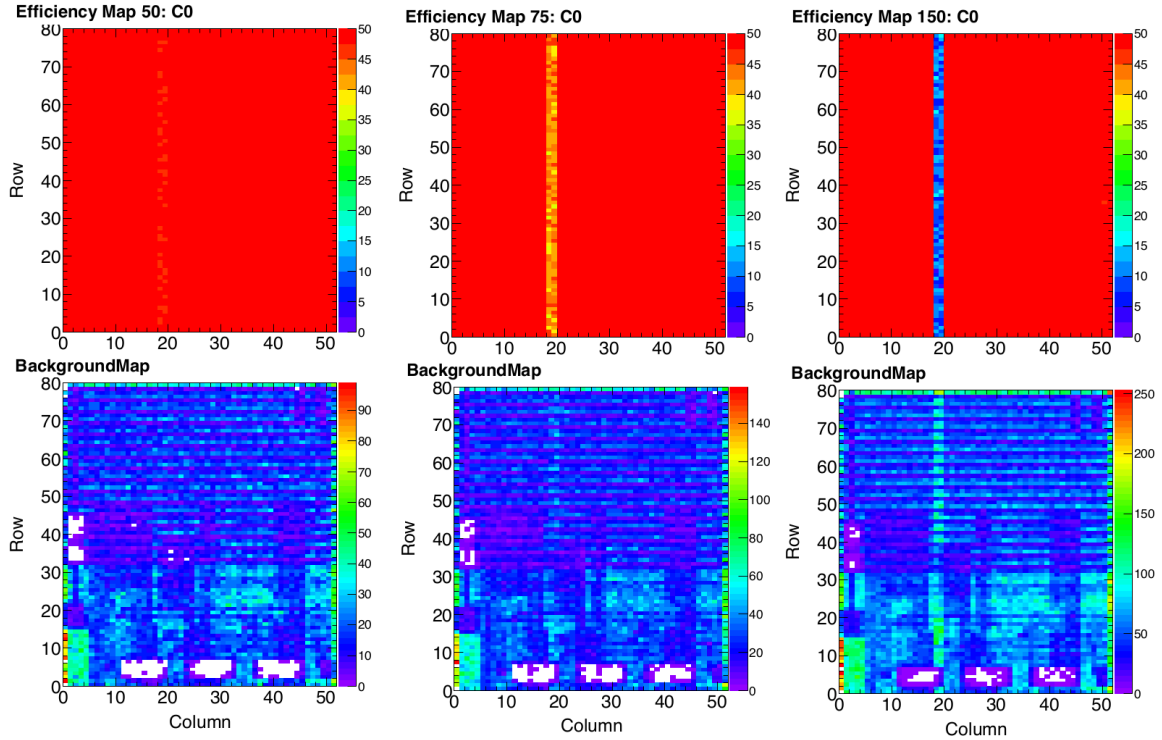




High rate x-ray test





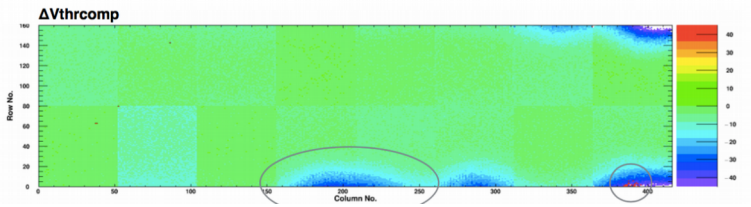


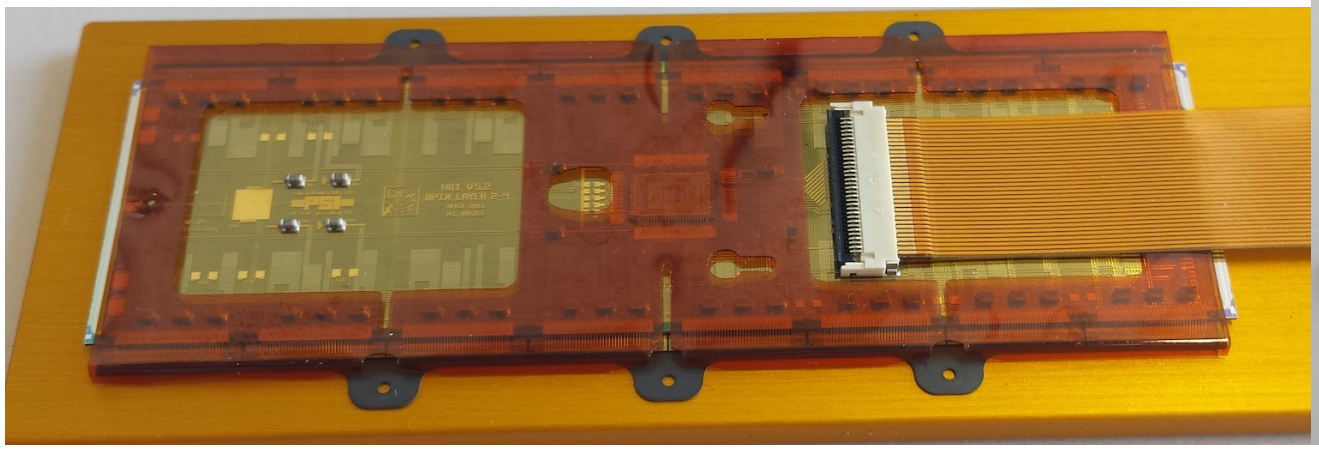
efficiency(cal) hitmap(x-rays)

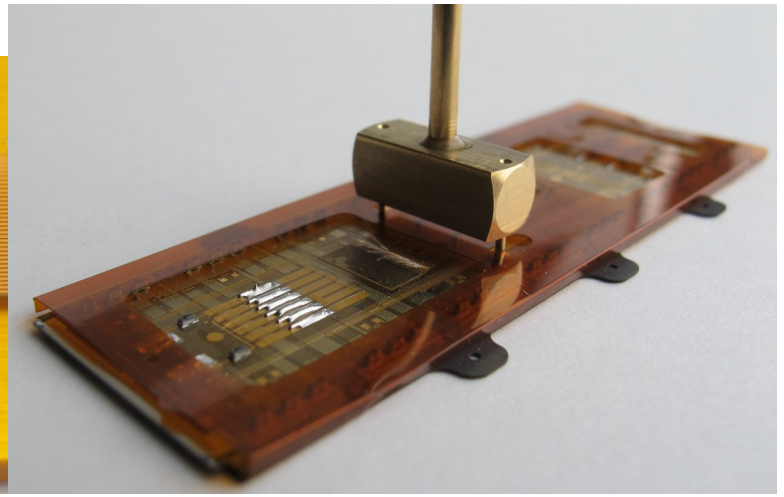
- High rate tests may reveal defects that do not show up otherwise
- affects < 1 % of the ROCs, maybe a more elaborate wafer test could have caught it if the issue had been known at that time

BPIX assembly : Module protection caps

- After mounting, cables run on top of other modules
- Phase 1 cables are more flexible than for phase 0
  - Protect all wire-bonds (phase 0 pixel: only TBM)
  - 75 um Kapton foil, cut-outs, bent at edges
- Lost a few modules in this step
(handling, procedure optimization)
- Worked nicely during integration (handling tool)

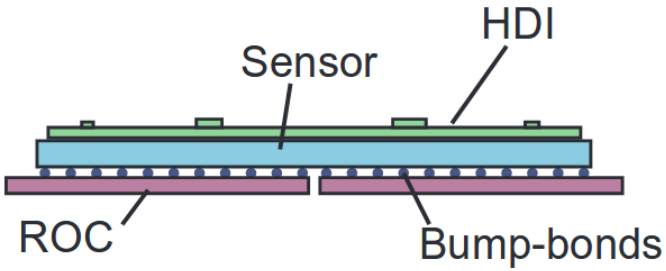


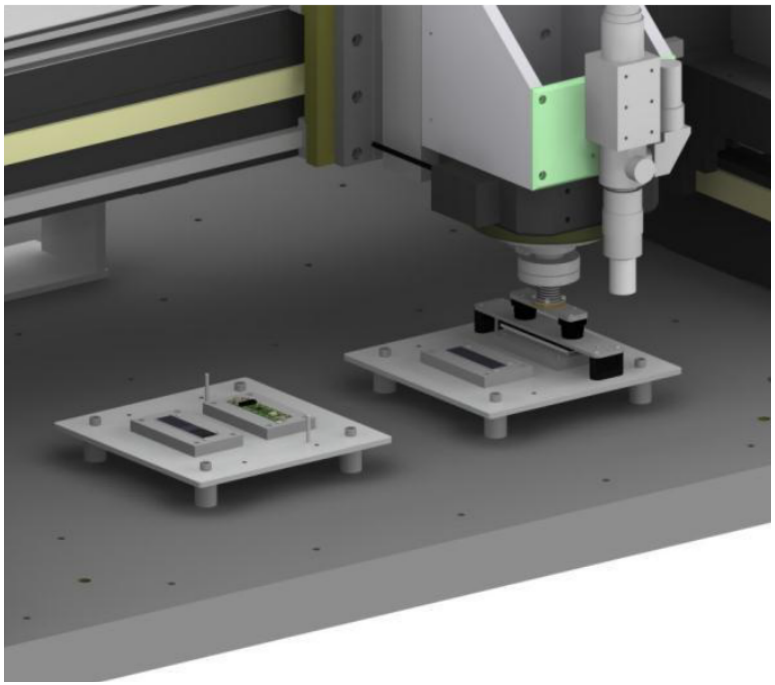




FPIX assembly

- Wire-bond encapsulation instead of module caps
- High throughput achieved (2x higher than a BPIX center)
- Sometimes slowed down
  - availability of parts (happened in BPIX, too)
  - limited testing capabilities
- Overall yield (including bare-module yield): 69 %
  - Could have been significantly higher with bare module test
  - ~20 % spares





Lessons : production

- Sustained production throughput needs all ingredients
  - components, assembly stages + personnel , test equipment
- bump bonding can be difficult, even if it worked at some point or for someone else
  - Multiple vendors / processes can be a good thing
    (caveat : may not be able to use material prepared for others)
- Similar lesson from Atlas (including, but not restricted to bump-bonding)
  - fast Q/A , short reaction times are important
  - Good /direct contact to vendors
- bare module tests can be useful,
  - If yield is an issue and rework is possible
  - Otherwise avoid time-lags between bump-bonding and final assembly(see above)

Lessons: production

- wafer tests of ASICs should catch as much as possible (BPIX high rate test yield)
  - have your ASICs early and prepare testing carefully
- Fine pitch HDIs can be tricky, BPIX and FPIX had problems, Not mentioned by Atlas
  - limits of technology + soldering + wire-bonding
  - assess vendors ability (and willingness) early,don't take constant quality for granted (good to have a second source)
- Visual inspection can be crucial, but
  - cumbersome / expensive on high volumes (automatization?)
  - sometimes difficult do draw hard / objective conclusions
- To pot or not to pot ?
  - Both approaches seem to work fine for CMS
  - Atlas : avoid full encapsulation (CTE mismatch issues)

Unexpected problems, how to avoid them

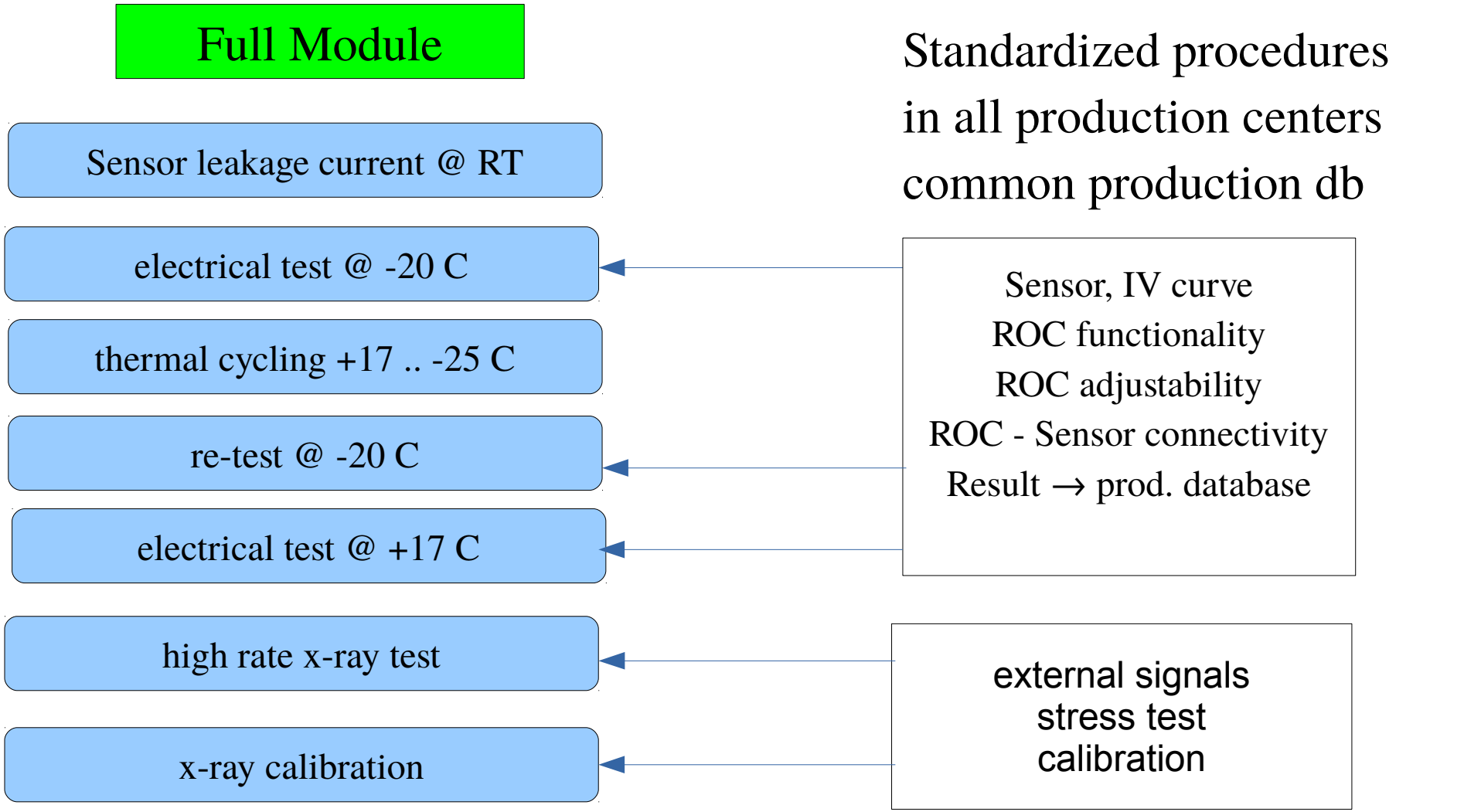
- L1 ROC timing offset
  - Trivial oversight, how to avoid?
    - Direct communication between designers of interacting parts
    - don't assume everybody is aware of the obvious
  - Follow up on unexpected results (here: different caldel values)
  - Higher granularity of delay adjustments would provided a workaround
- TBM locking up (presumably SEU)
  - Hard to catch in tests (unless you know exactly what to look for)
  - Make sure you can reset as much as possible without power-cycling
- HV problems
  - Exact failure to be seen
  - Full module / in-situ HV was not possible with BPIX sensors, would be nice to have

Recommendations

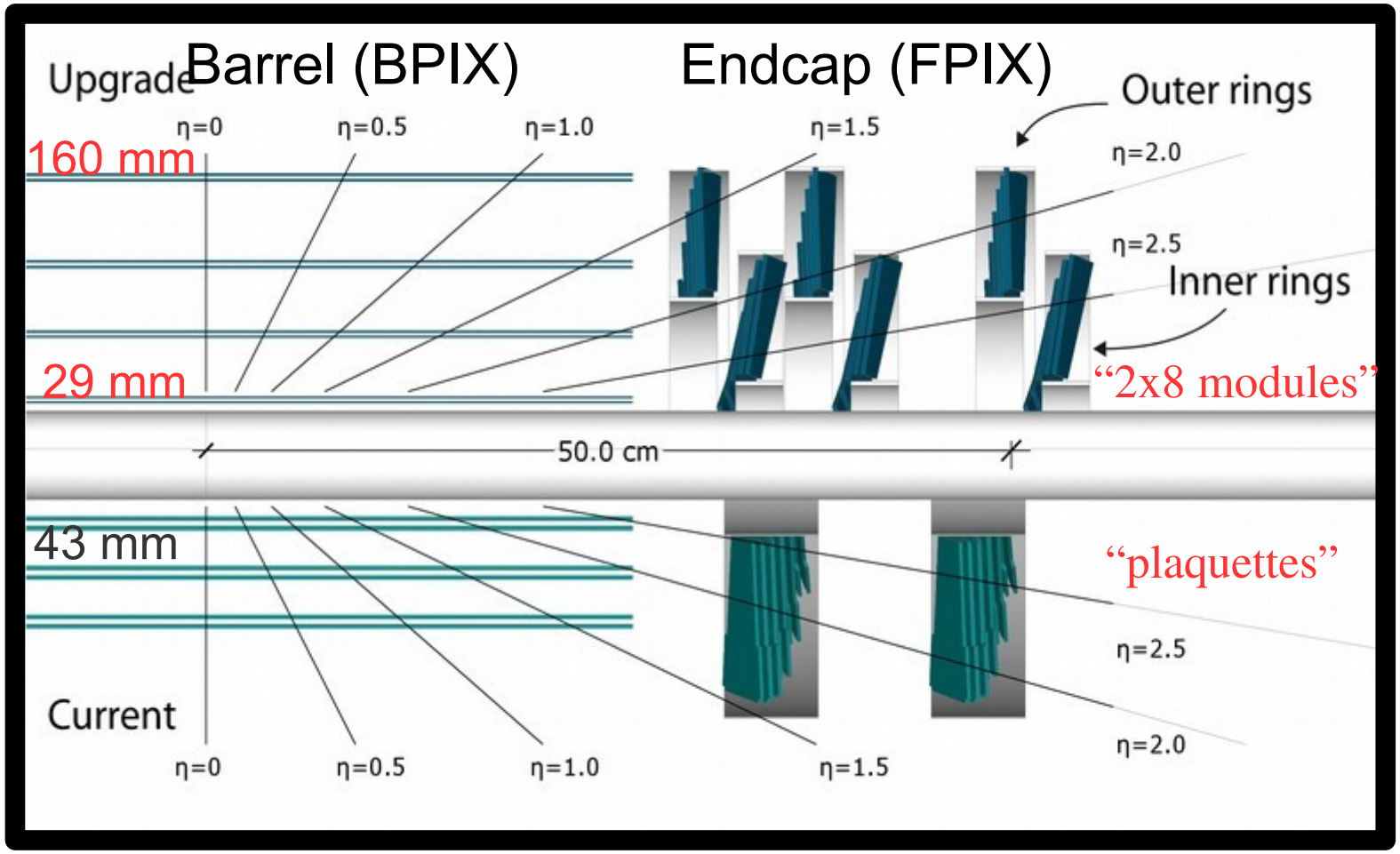
- Production (Atlas speaker recommendations, similar to our conclusions)
  - "Don't go too early into production, take enough time for pre-production"
  - "Push for fast turnaround, immediate feedback"
  - "Be prepared for suprises"
  - "Testing can be a bottleneck, ensure sufficient testing capabilities"
- Design/ Development (mostly trivial and in contradiction with reality)
  - A large system in which every part needs fine-tuning is hard to operate, high granularity and adjustability may allow workarounds for the unexpected
  - Avoid having to finish things in a rush
    - Possible issues get overlooked
    - Things get damaged
    - Tests are more useful if there is still time to address problems


CMS
Compact Muon Solenoid

Module qualification



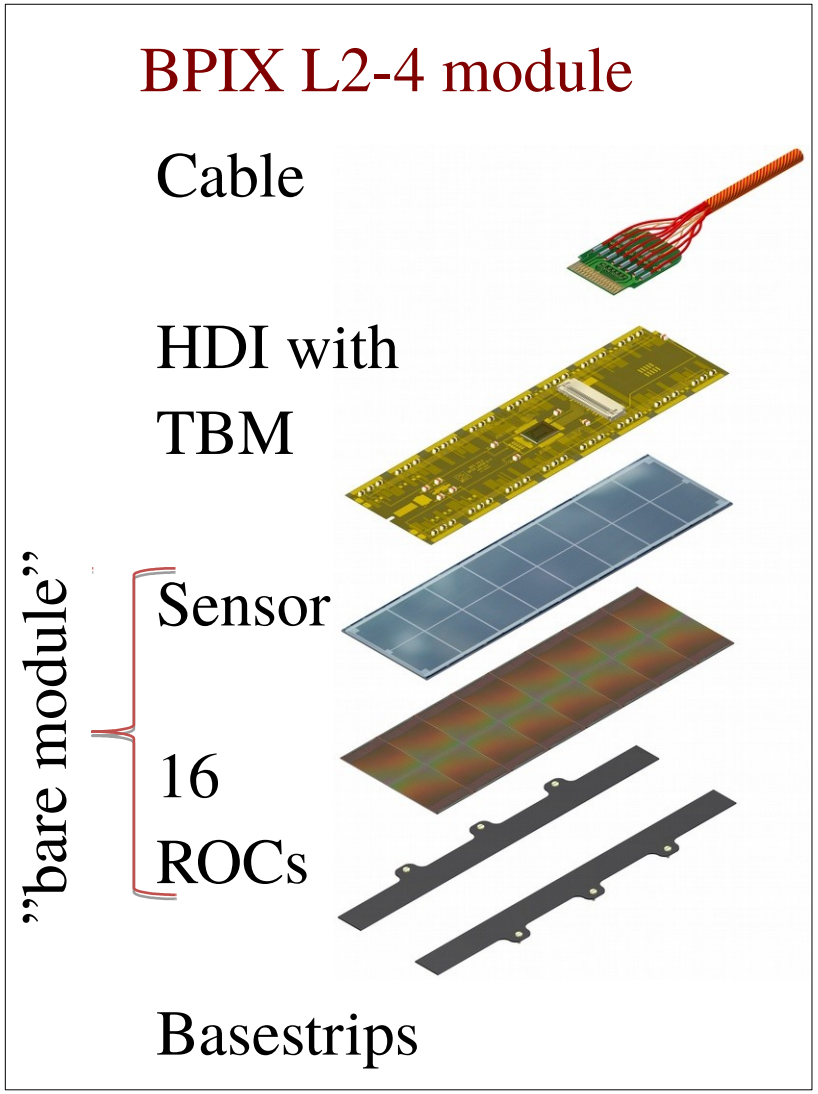
Phase 1 pixel upgrade



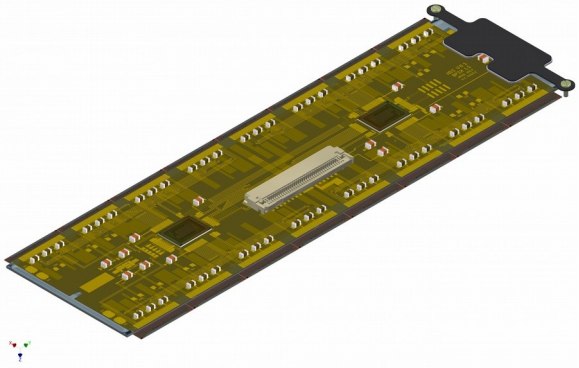
- Front-end and readout with higher rate capability
- Additional tracking layer in central and forward for improved pattern recognition in high PU

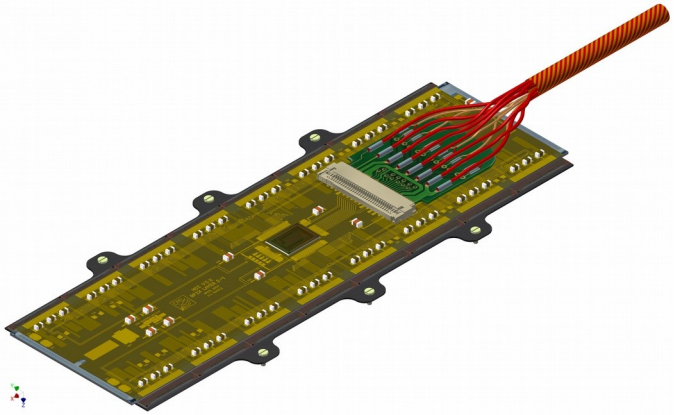
Modules

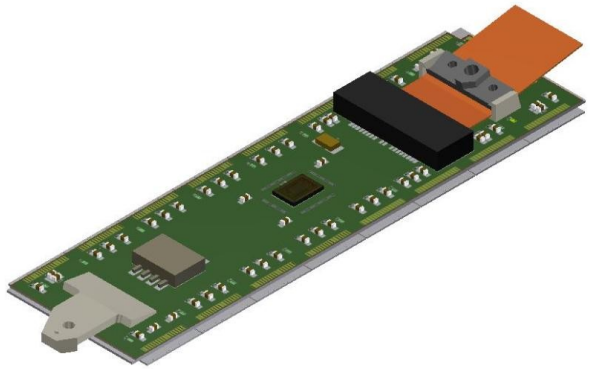
- Simplified module concep wrt “phase 0” :
  2x8 Readout chip modules in FPIX and BPIX
  - “Phase 0” :
    - BPIX 2x8 + 1x8
    - FPIX blades with “plaquettes” :
- However
  - Non-uniform requirements in different parts of the detector (rates, geometry)
  - Contributing groups have differing expertise / experience / equipment / preferences
- ended up with 4 different module types



Modules Flavors







layer	Radius [cm]	modules	Hit rate [MHz/cm^2]	Links / module	Rate/link [Mbits/s]
1	3.0	96	580	4	140
2	6.8	224	120	2	80
3	10.2	352	60	1	80
4	16.0	512	40	1	60
D1-3 inner	4.5-11.0	264	100	1	130
D1-3 outer	9.6-16.1	408	40	1	70

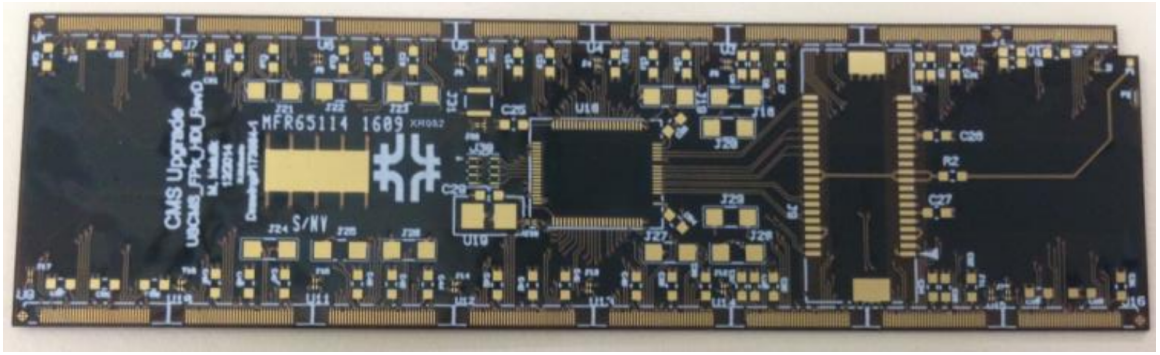
Module production

- BPIX
  - 5 production consortia
    - PSI / ETHZ (L1, L2)
    - CERN / TW / FIN (½ L3)
    - INFN (½ L3)
    - KIT/ Aachen (½ L4)
    - Desy / UHH (½ L4)
  - 5 different bump-bonding vendors
  - standardized assembly and testing
  - Integration center ETHZ / PSI
- FPIX
  - 2 assembly sites (assembly, electrical test)
    - Nebraska (½ FPIX)
    - Purdue (½ FPIX)
  - Common Bump bonding vendor
  - 2 testing / qualification sites
    - UIC
    - KU
  - Integration center FNAL

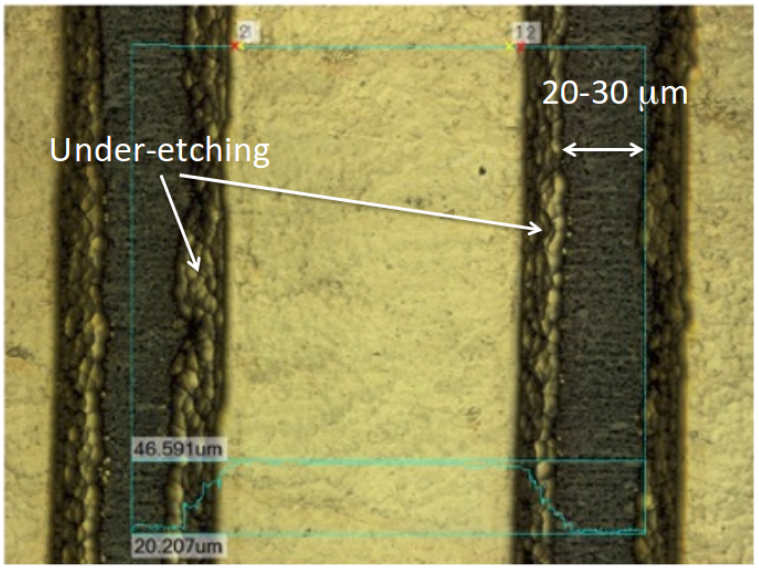
- Common FPIX / BPIX : ROC, TBM, testboard, software
- Different : sensors, BB, HDI, assembly procedure, module protection, cable, some tests procedures, db,

FPIX HDI ("a constant source of pain")

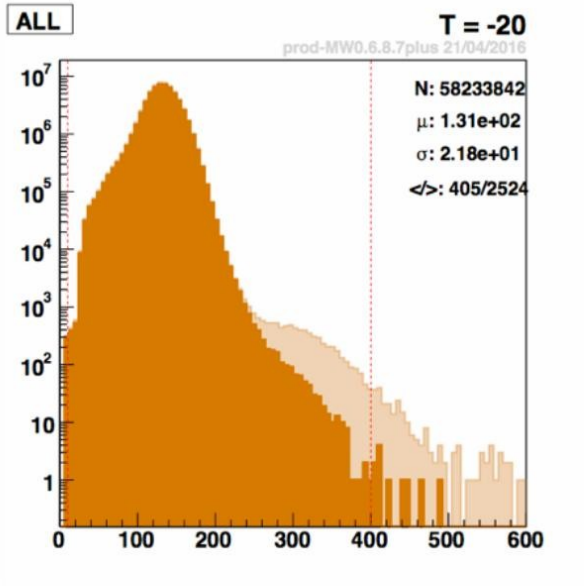
- Four layer flex, more standard PCB than BPIX
- First vendor failed to stay within specifications (tolerances, alignment of masks)
  - Most of the delivered HDIs were rejected after visual inspection
  - Some improvements but also batch-to-batch variations
- 2nd vendor with better results, but needed iteration, too
  - rather late addition
    (prototypes just a year before installation)

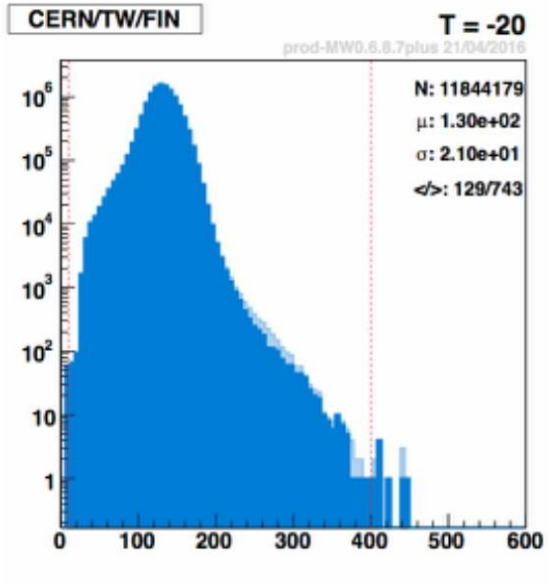


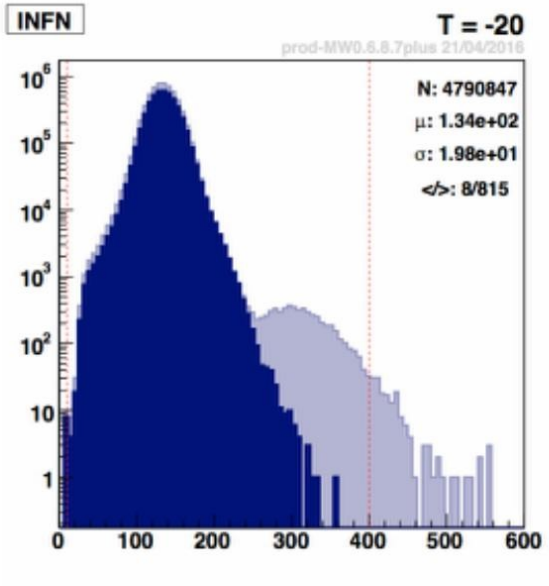
HDI Visual Inspection

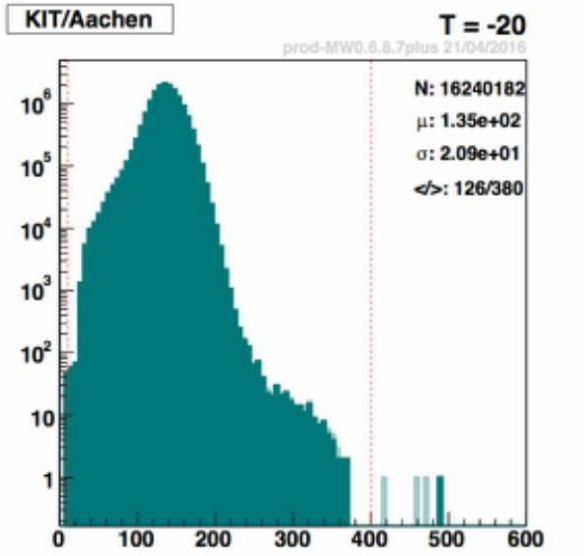


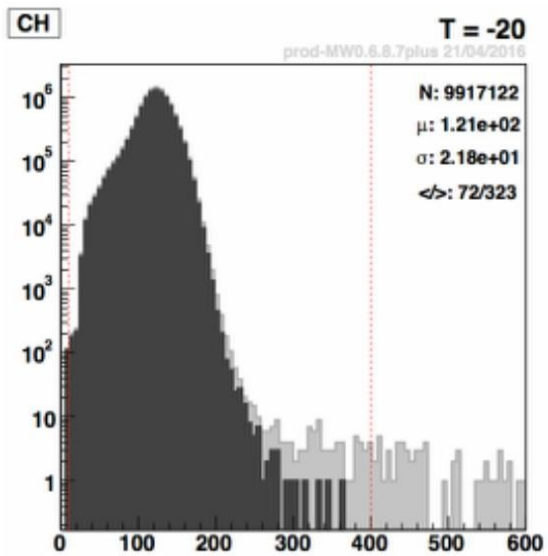
Pixel noise [e-]

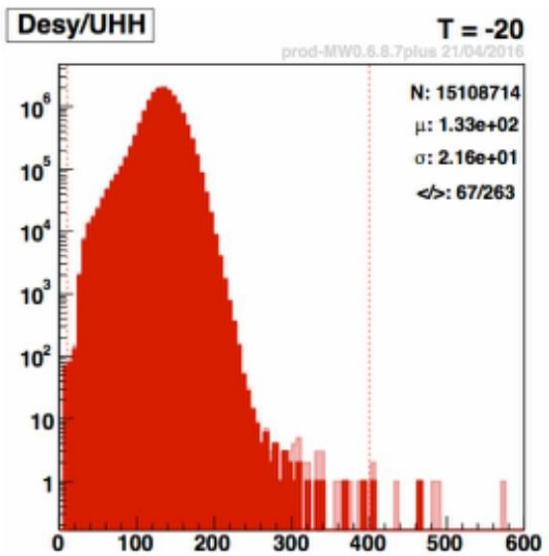






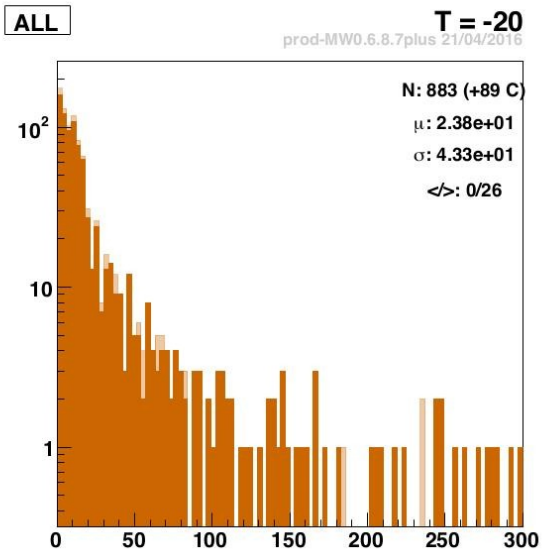


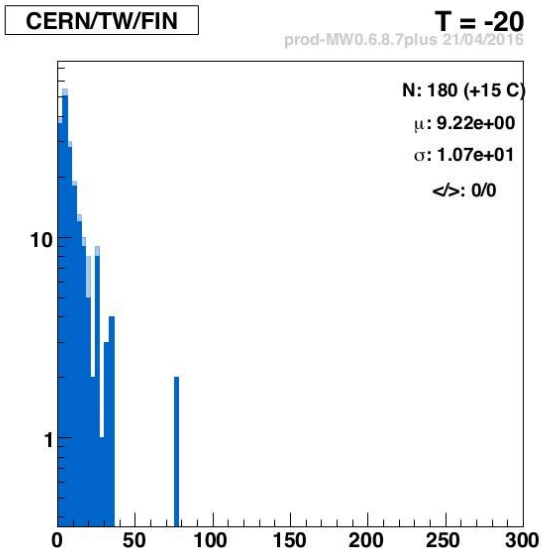


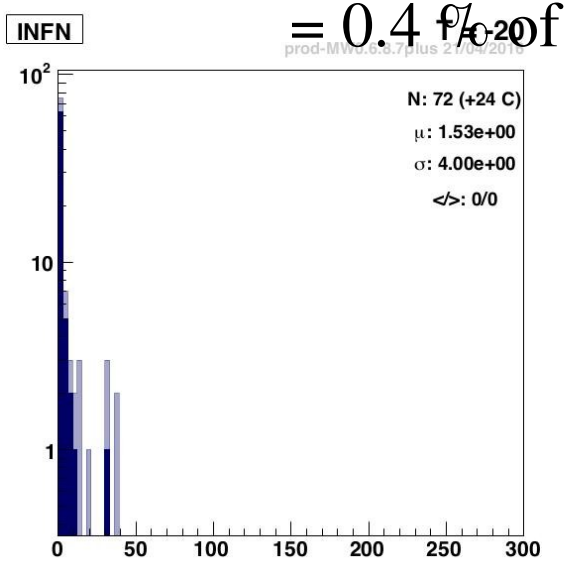


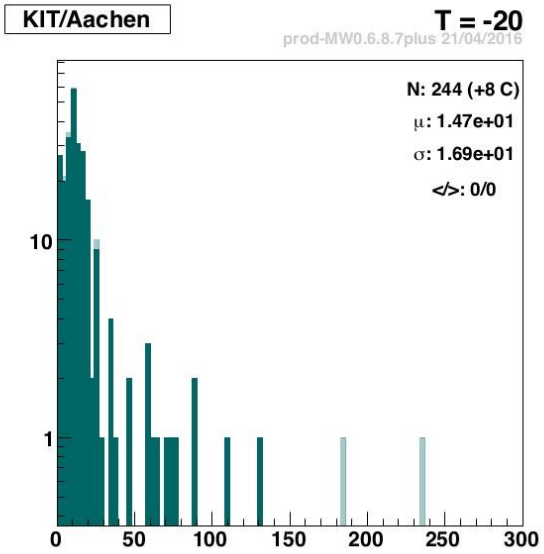
BB defects /module

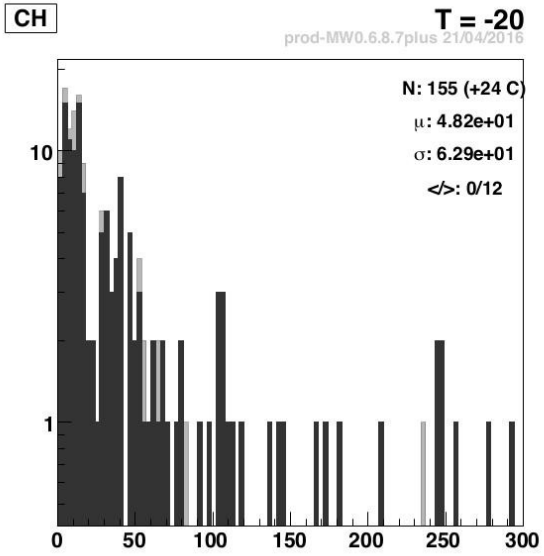
Note: 300 defects = 0.4 ‰ of 66k

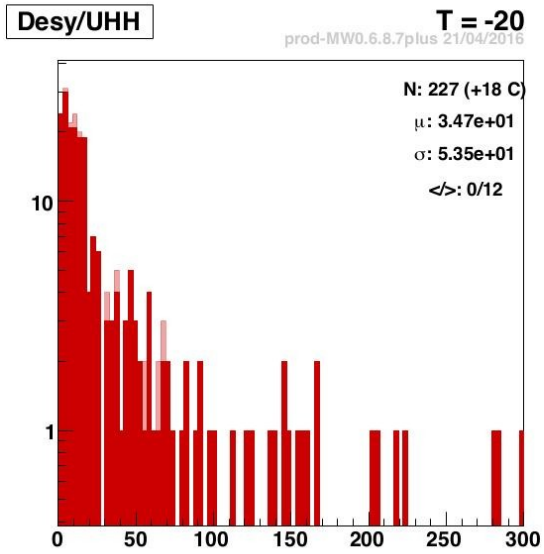




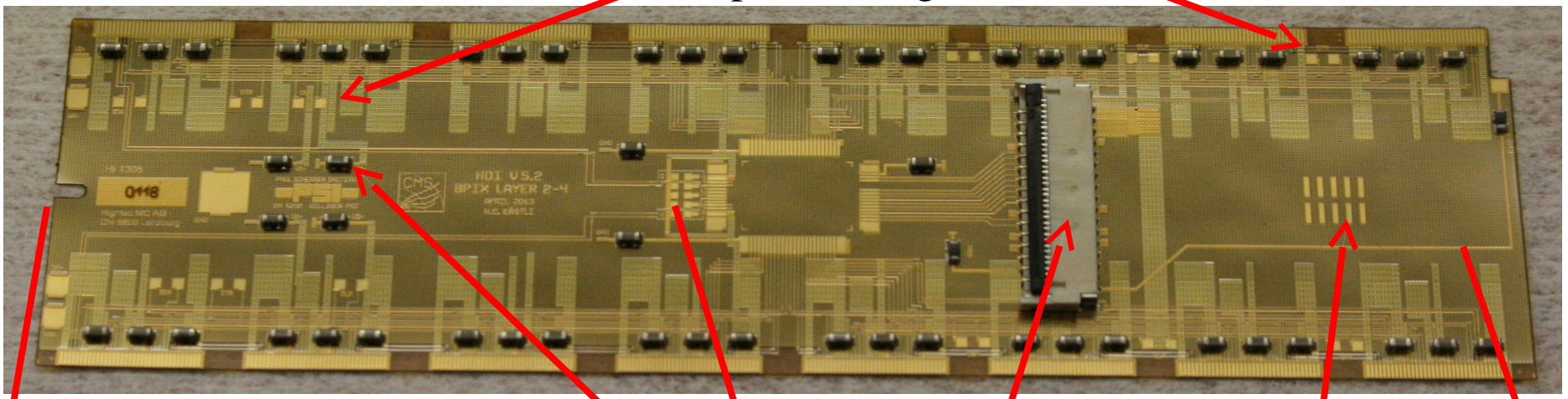


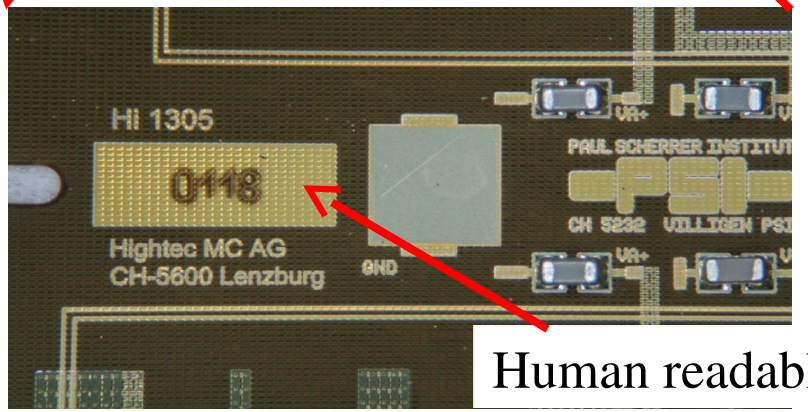






Outer Layers HDI





Human readable unique ID