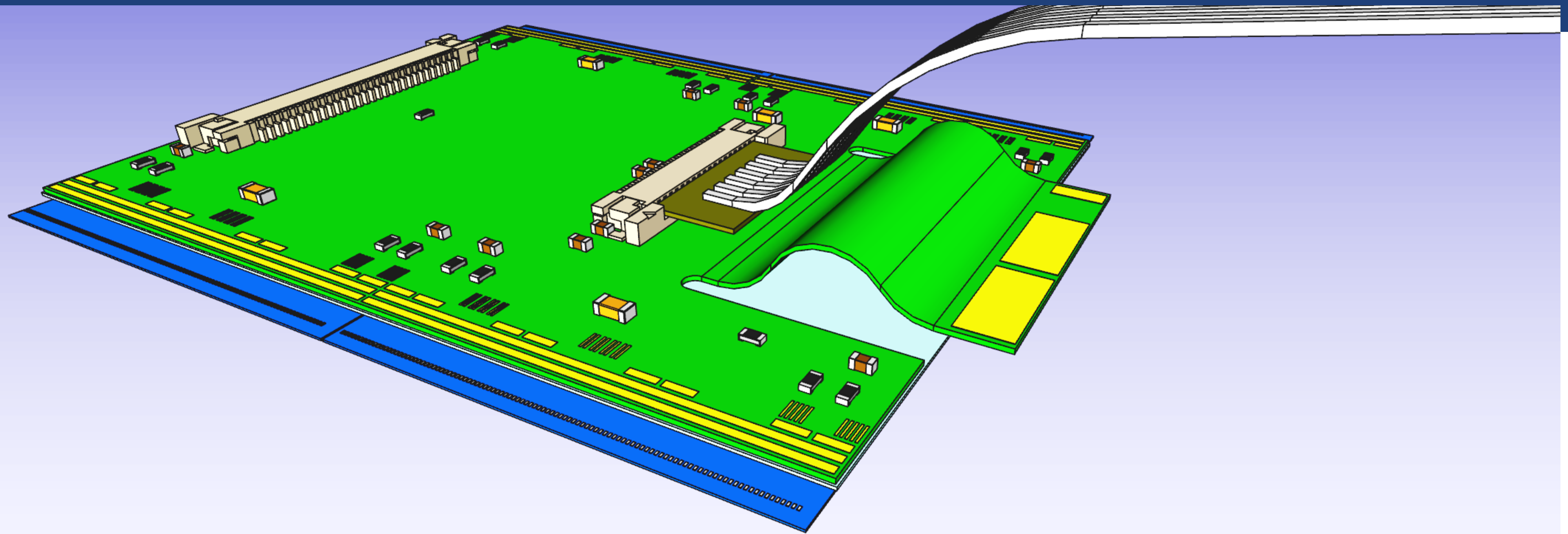
ETH zürich



Modules

Malte Backhaus

IPA

Outline

- Introduction to current activities in IT module WG
- Project schedule
- Barrel vs. disc modules
- Considerations on HDI design for serial powering
- Update of TBPX 2x2 RD53A HDI design

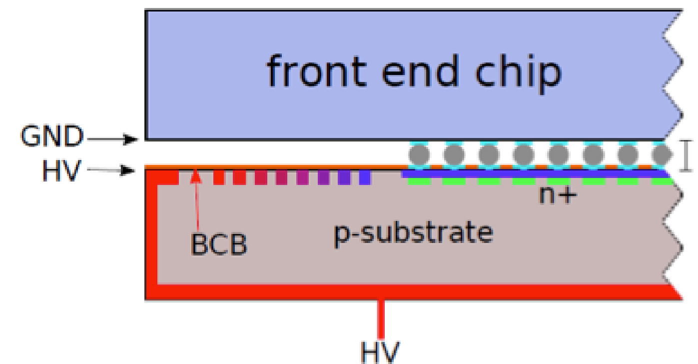
IT module WG activities

- Focus on RD53A modules this year.
- Plan to build ~100 RD53A modules, number in good agreement with “orders”.
  - 2x2 modules and 1x2 modules
- Sensor production by two vendors: FBK and HLL. Agreed to share the area with ATLAS.
- Purpose is **not** sensor or chip or BB validation, but
  - Module construction and testing procedure
  - Module component R&D (HDI, encapsulation, module rails, …)
  - Validation of thermal simulations on prototype mechanics
  - Serial powering validation (realistic SP chains)
- „Pseudo-2x2“ modules consisting of two 1x2 chip sensors (diced to single piece)
  → Larger gap between ROCs,
  900μm inactive distance in y-direction
  300μm active distance in x-direction
- Larger thickness of ROCs to increase mechanical stability

IT module WG activities

- Additional topics of the year:
  - Passive material irradiation
  - Power connector
  - eLink connector
  - AC-coupling scheme of eLinks
  - Adapter PCBs
  - Module test system

- Additional topics next year:
  - Spark mitigation on modules (in sensor WG)
  - Wire bond protection
  - Assembly procedures
  - Start development of production test program



RD53A module count

- Result of poll in good agreement with previously estimated number of modules.
- Price per module between 1.5kCHF and 1.9kCHF, to be reimbursed by institutes.

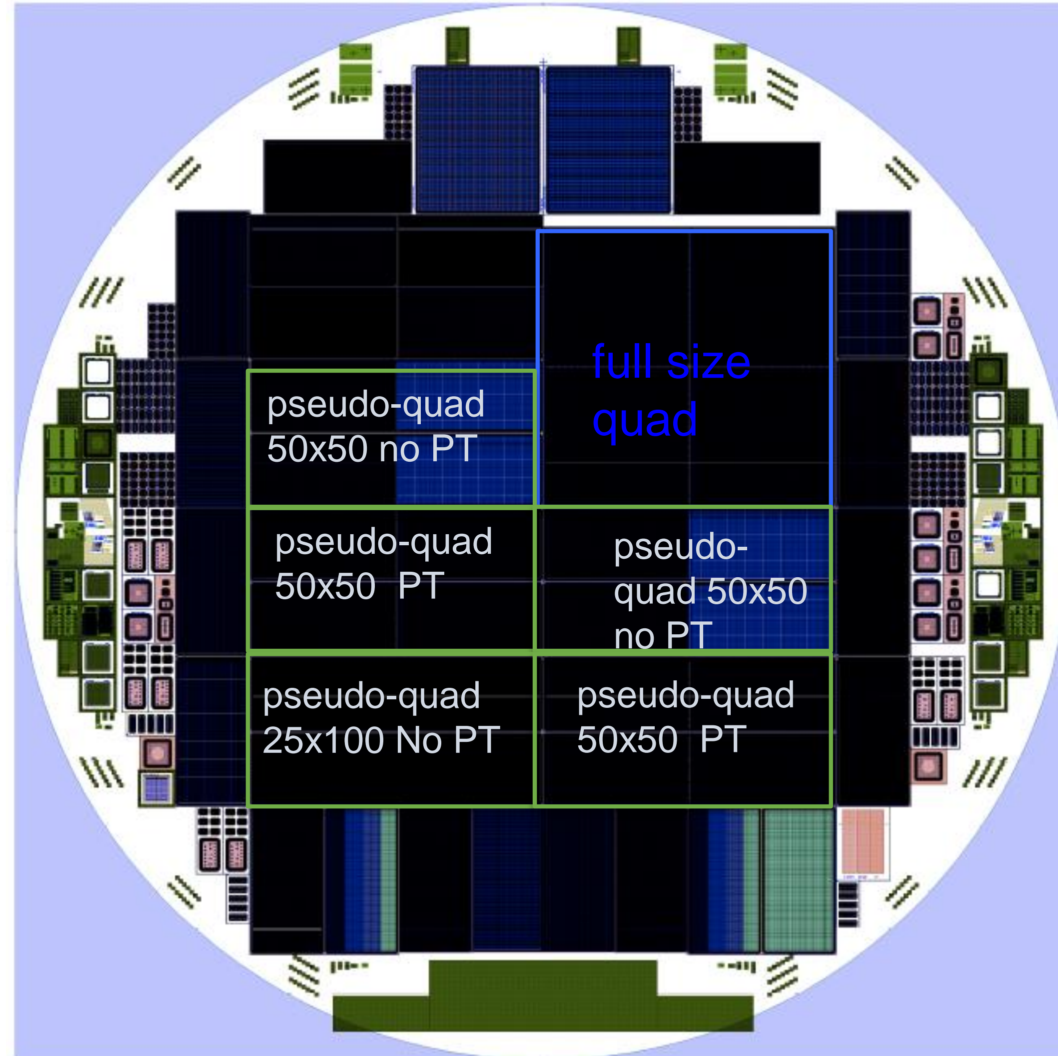
Institute	Contact	1x2 dressed	2x2 dressed	1x2 bare	2x2 bare	Comment
INFN Milano Bicocca	Mauro Dinardo	1	1	0	0	
Instituto de Fisica de Cantabria (CSIC-UC) - Santander	Ivan Vila	0	0	10	0	
ITAINNOVA	Alvaro Pradas	2	0	0	0	to be received from Santander
PSI	Wolfram Erdmann	0	0	0	4	
ETH Zurich	Malte Backhaus	0	0	0	20	includes modules for SP demonstrator
University Hamburg	Georg Steinbrück	0	2	0	4	
US	Karl Ecklund	3	3	0	4	4 to be decided later
Zagreb	Andrei Starodumov	0	0	3	0	
Florence	Giacomo Sguazzoni	2	15	0	0	
CERN	Jorgen Christiansen	12	12	0	0	
Sum of type		**18**	**33**	**13**	**32**	
Total					**96**	

→ TEPX: ~7 modules
→ TFPX: ~10 modules
→ TBPX: ~79 modules

ETH zürich

RD53A module sensor production: HLL

- Design by A. Macchiolo, MPI Munich.
- Productio ongoing
  → Ready in September
- UBM, BCB, and thinning at HLL.
- Agreed with ATLAS to share the wafer area
- Several large structures:
  - One ATLAS “full size” quad
  - Five RD53A 2x2 sensors (1x2 sensors, dicing to 2x2)
- 20 Wafers in production:
  - 12 wafers of 100µm thickness
  - 8 wafers of 150 µm thickness



IPA

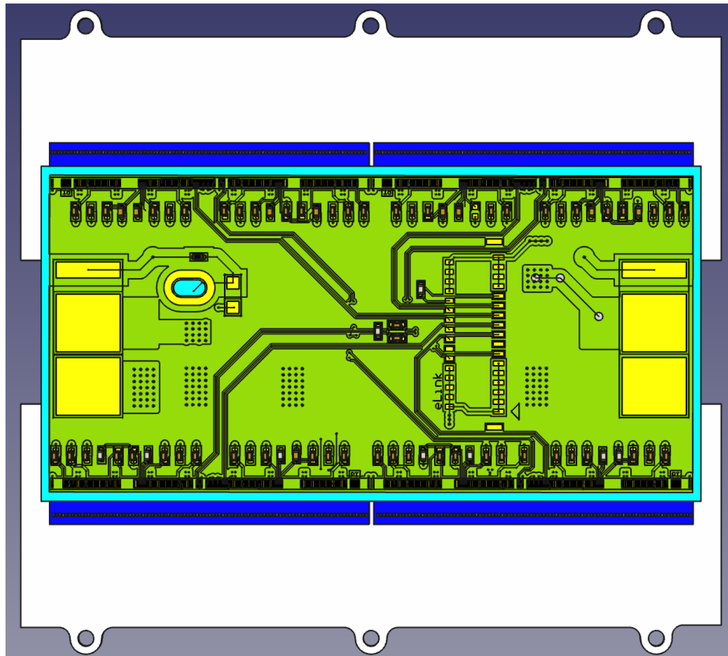
RD53A module sensor production: FBK

- Silicon wafers ordered from ICEMOS
  → Delivery expected (as of yesterday): July 2018
- 20 wafers, 150 µm SiSi direct bonded
- Processing at FBK should start in June to avoid significant delay
  → Need to order masks by mid-June
  → Sensors available by end of 2018
- Design started based on existing structures (guard rings, pixel cells, ...)
- ATLAS interest in shared FBK produktion vanished
  → This is our production now. Agree next week for structures to place on wafer layout

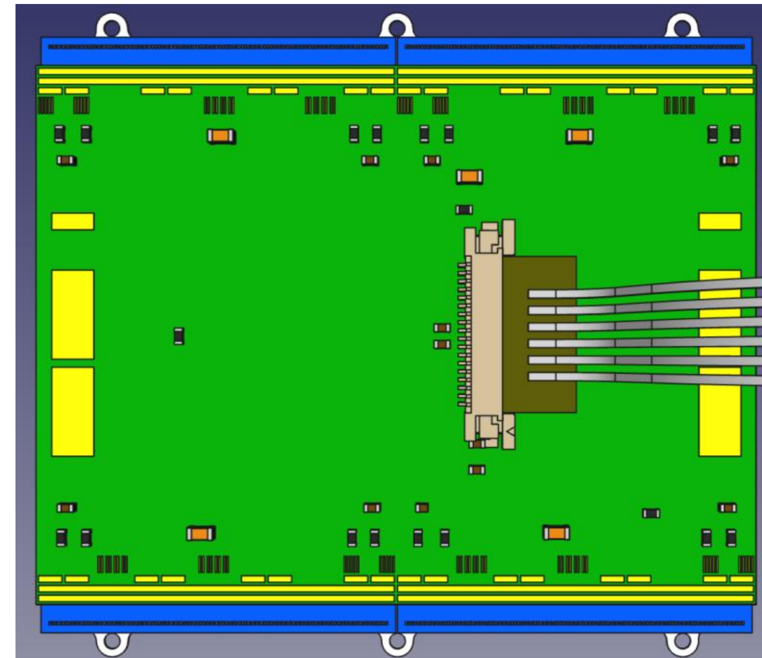
RD53A module dimensions

- Drawing of RD53A 2x2 module with realistic dimensions
  - Larger gap between ROCs
  - Module Rail dimensions (fixation) compatible with final module, stretched in y-direction
    → used dimensions of TBPX mechanics drawings. Need revision.

RD53A 2x2 Module

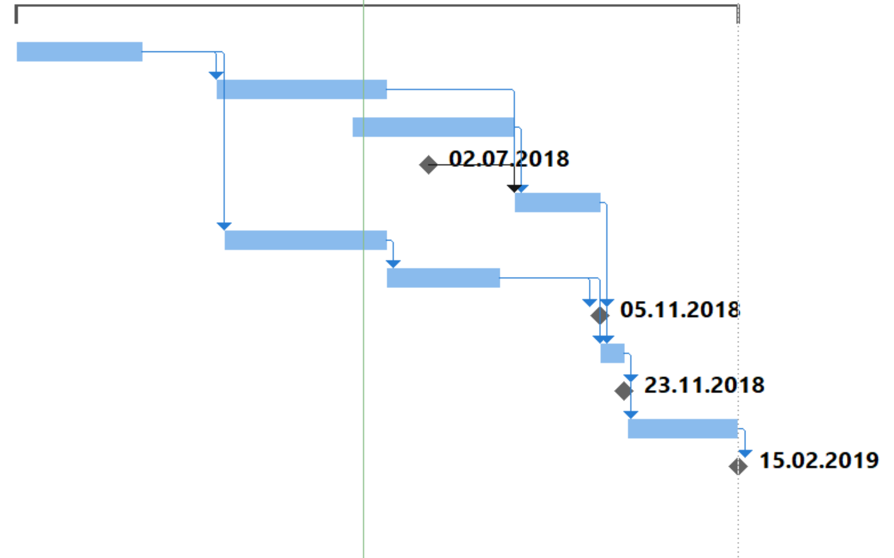


Final PROC 2x2 Module



Updated schedule for first few modules

Task Name	Duration	Start	Finish
RD53A Prototype	**382 days**	**Thu 31.08.17**	**Fri 15.02.19**
RD53A Production	67 days	Thu 31.08.17	Fri 01.12.17
RD53A Testing	90 days	Fri 26.01.18	Thu 31.05.18
RD53A Sensor Production at HLL	86 days	Mon 07.05.18	Mon 03.09.18
Probed RD53A wafers available	0 days	Mon 02.07.18	Mon 02.07.18
Flip Chip	45 days	Tue 04.09.18	Mon 05.11.18
RD53A HDI design	86 days	Thu 01.02.18	Thu 31.05.18
RD53A HDI production	60 days	Fri 01.06.18	Thu 23.08.18
RD53A prototype material ready	0 days	Mon 05.11.18	Mon 05.11.18
RD53A Module Assembly	14 days	Tue 06.11.18	Fri 23.11.18
RD53A Prototype ready	0 days	Fri 23.11.18	Fri 23.11.18
RD53A Module Tests	60 days	Mon 26.11.18	Fri 15.02.19
First RD53A Multichip modules constructed and tested	0 days	Fri 15.02.19	Fri 15.02.19

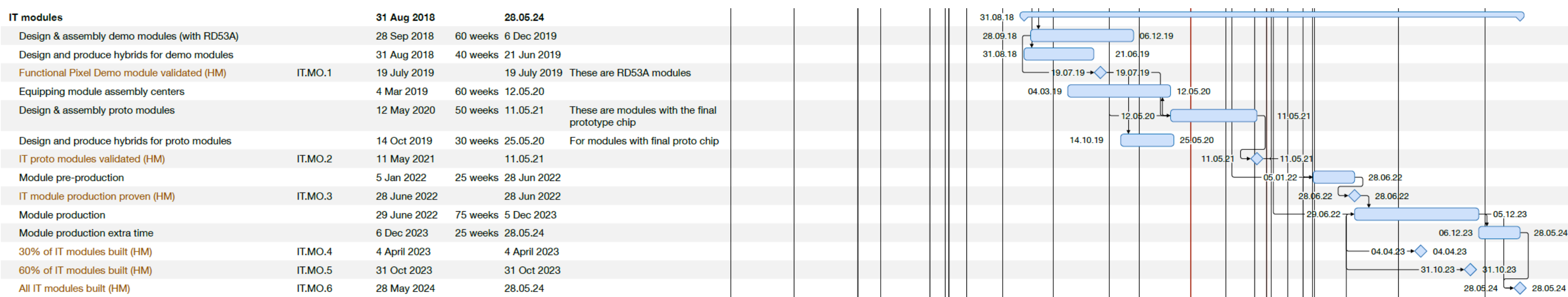


- Schedule updated.
- With started HLL production we are well on schedule to meet milestone 6 month earlier (see next slide).
- Next uncertainty: availability of probed RD53A wafers. Probing independent of Bonn by ~August would be beneficial.
- FBK sensors available later, ~November 2018. Wafers ordered, expected May/June.
- Will build modules without sensors as soon as HDI and chips available.

ETH zürich

Overall Tracker Schedule

Screenshot of latest Tracker Upgrade Schedule



Task	ID	Start	Duration	Finish	Notes
IT modules		**31 Aug 2018**		**28.05.24**	
Design & assembly demo modules (with RD53A)		28 Sep 2018	60 weeks	6 Dec 2019	
Design and produce hybrids for demo modules		31 Aug 2018	40 weeks	21 Jun 2019	
Functional Pixel Demo module validated (HM)	IT.MO.1	19 July 2019		19 July 2019	These are RD53A modules
Equipping module assembly centers		4 Mar 2019	60 weeks	12.05.20	
Design & assembly proto modules		12 May 2020	50 weeks	11.05.21	These are modules with the final prototype chip
Design and produce hybrids for proto modules		14 Oct 2019	30 weeks	25.05.20	For modules with final proto chip
IT proto modules validated (HM)	IT.MO.2	11 May 2021		11.05.21	
Module pre-production		5 Jan 2022	25 weeks	28 Jun 2022	
IT module production proven (HM)	IT.MO.3	28 June 2022		28 Jun 2022	
Module production		29 June 2022	75 weeks	5 Dec 2023	
Module production extra time		6 Dec 2023	25 weeks	28.05.24	
30% of IT modules built (HM)	IT.MO.4	4 April 2023		4 April 2023	
60% of IT modules built (HM)	IT.MO.5	31 Oct 2023		31 Oct 2023	
All IT modules built (HM)	IT.MO.6	28 May 2024		28.05.24	

- RD53A prototype modules: 19/07/2019 → 6 months ahead
- Prototype modules (final ROC): 11/05/2021
- Production capability proven: 28/06/2022
- Module production: 06/2022 – 01/2024 (+ 6 months safety margin)

→ Six months ahead with RD53A modules, but not incredibly large time for R&D left.

→ Keep progress high and streamlined. But look also sideways from baseline:
Al in HDI for supply current, other SP options, novel sensor techn., …

Module differences between barrel and discs

- Geometrically very different constraints:
  - Connector positioning (esp. power connector) should be different:
    → barrel modules: current-in on one end, current-out on opposite ends
    → disc modules: current-in and current-out on both wire bond sides or on same end
  - Module fixation
    → barrel modules on the wire-bond side
    → disc modules on the ends
- In TFPX inner ring: factor ~5 difference in TID within one ROC
  (factor 7 per sensor)
  → if along columns (current design), independent bias setting per DC easily possible, current/voltage mirrors per DC present in RD53A

→ Electrical and mechanical constraints of HDI are very demanding
(see later slides)

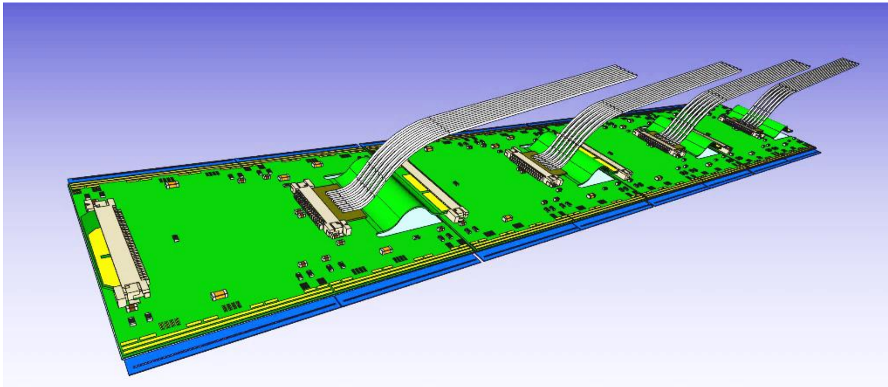
→ Same HDI for barrel and disc structures leads to additional complications
→ Plan with dedicated designs

Module Connections

TBPX

Module connection design converging:

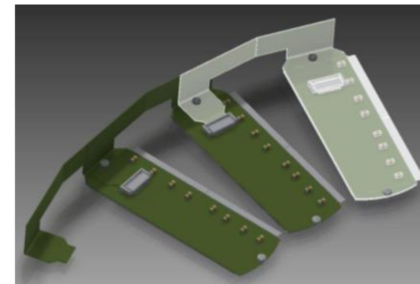
- Pigtail + ZIF power connector
- Independent eLink connector
- Return current on module
(change of mechanical support would be needed to route the return current on the "ladder" or "stave" backside)

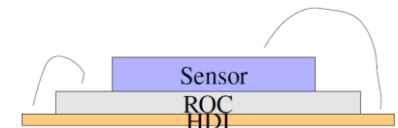


TEPX/TFPX

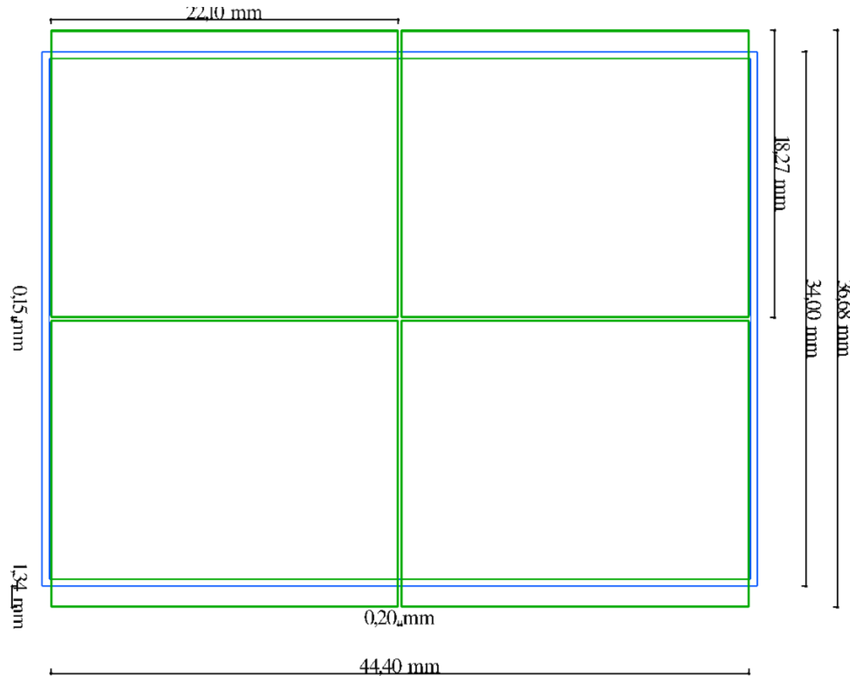
Connection designs under investigation:

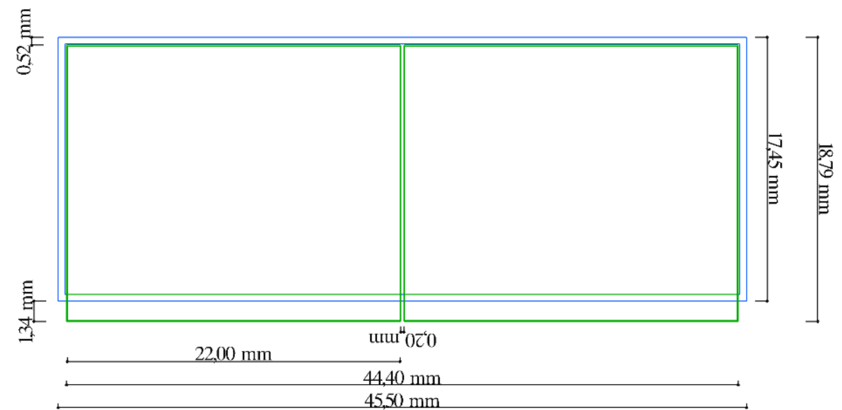
- Pigtail HDI extension from module to module
- Laminate HDI on disc and wire-bond down
  - "best" for current routing sideways
(ATLAS investigates flex cable over wire-bonds)
  - Module replacement?





Final module dimensions





- Module dimensions for the bump bonding market survey
  - ROC sealing ring and dicing line included
  - 200um spacing between ROCs in *x*, ≥150 um in *y*
    → all ROC edge pixels are 50 um x 200 um
    → all ROC corner pixels are 200 um x 200 um
  - 450 um inactive edge in sensor

HDI design

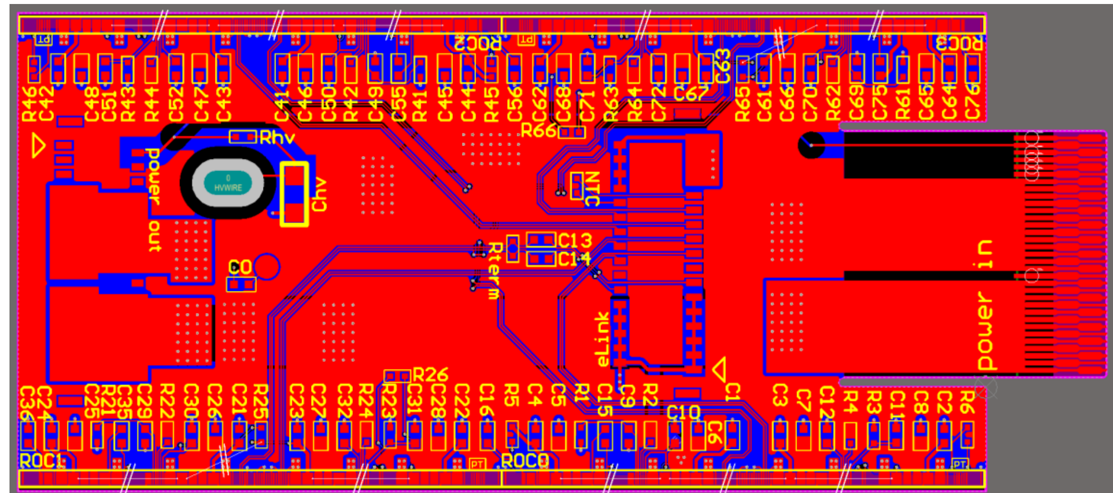
- Many guidelines for HDI design in:
  - Module design workshop (https://indico.cern.ch/event/681506/)
  - Alvaro's presentation in IT modules meeting (https://indico.cern.ch/event/668468/contributions/2866651/attachments/1588089/2511705/PCB_design_recommendations_VF3.pptx)
  - Discussions with Alan Honma
- Started design for RD53A 2x2 TBPX prototype modules.
- Design files in CERN Gitlab repository during development, in sharepoint once submitted. Inform me if you like to get access.
- Created libraries with the footprints etc. for easy sharing.
- Currently in contact with one possible vendor, also used for OT hybrids.
- Design started to have a good base for discussion with vendors.
  → submission planned next week

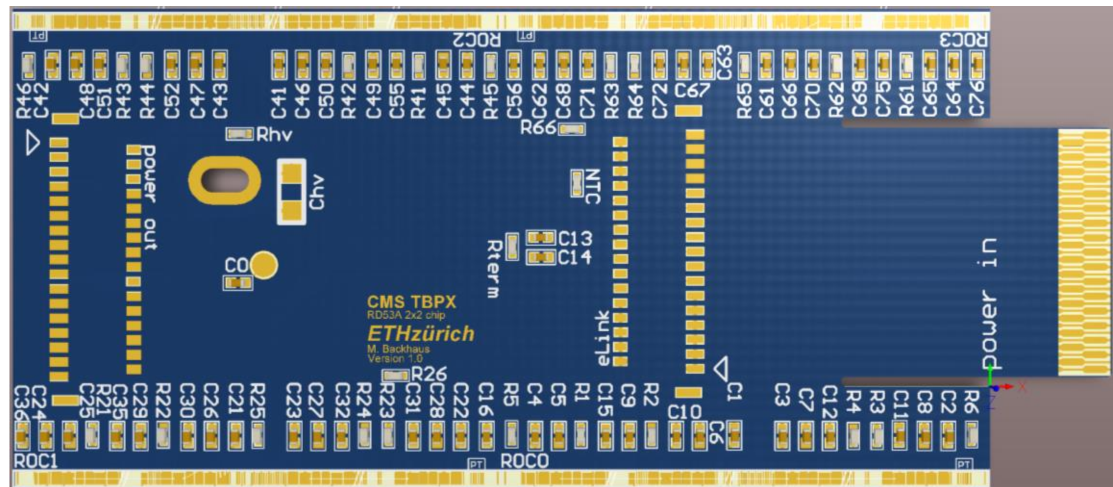
HDI Requirements

- Clearance driven by wire-bond pad frame
  - If possible on HDI: single row, no fanout, >50um wide pads
  - ROC: 100um pitch
  - → Chose 60um wide pads, 40um clearance (updated last week)
    → 10um copper thickness and ENIG/ENEPIG gold-plating possible with larger clearance
- High voltage design
  - More challenging due to distribution from module to module
  - Clearances, design constraints, etc. to be discussed with vendor next week
- Supply current distribution
  - Up to 8A in I_{in} and also I_{ret} on final modules, ~1/2 on RD53 modules
  - Low as possible resistance difference between parallel chips
  - Need a plane on stable potential for shielding + return current routing on the module (TBPX)
  - → Use Bottom Layer as “local module GND” plane
  - → Use Top Layer as I_{in} plane
  - → Use middle plane for return current routing
- Radiation tolerance
  - Activation
  - Glue delamination
  - → To be validated

Overview

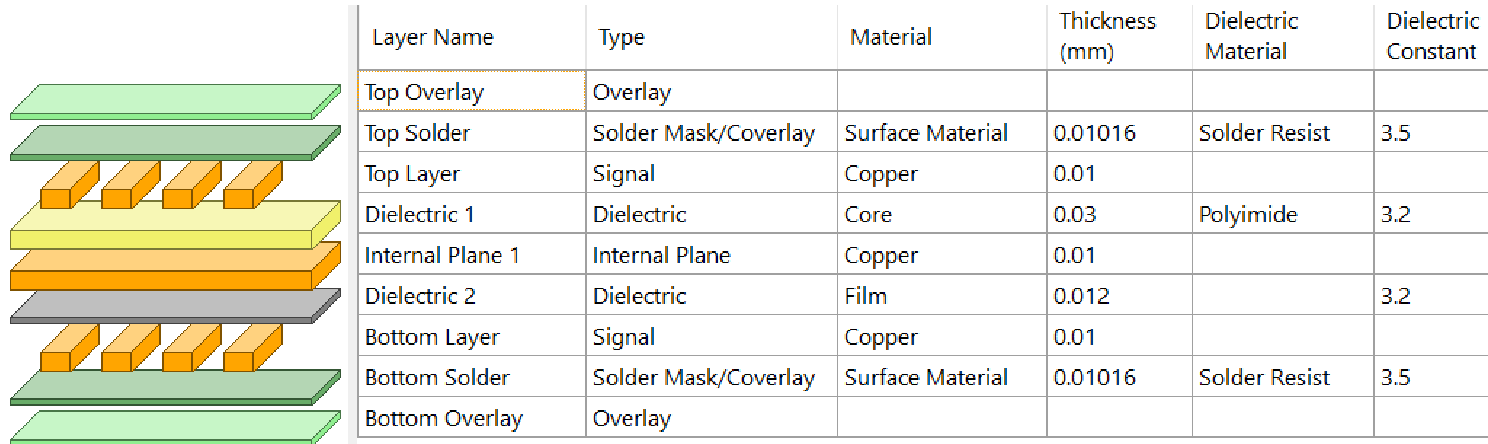
- For now: Phase 1 BPix ZIF connector for eLink (lack of existing alternative…)
- Phase 1 Bpix ZIF connector for power
- 0402 SMD components
  → possibility for manual replacement
  → later 0201 possible where voltage rating allows





TBPX HDI layer stack

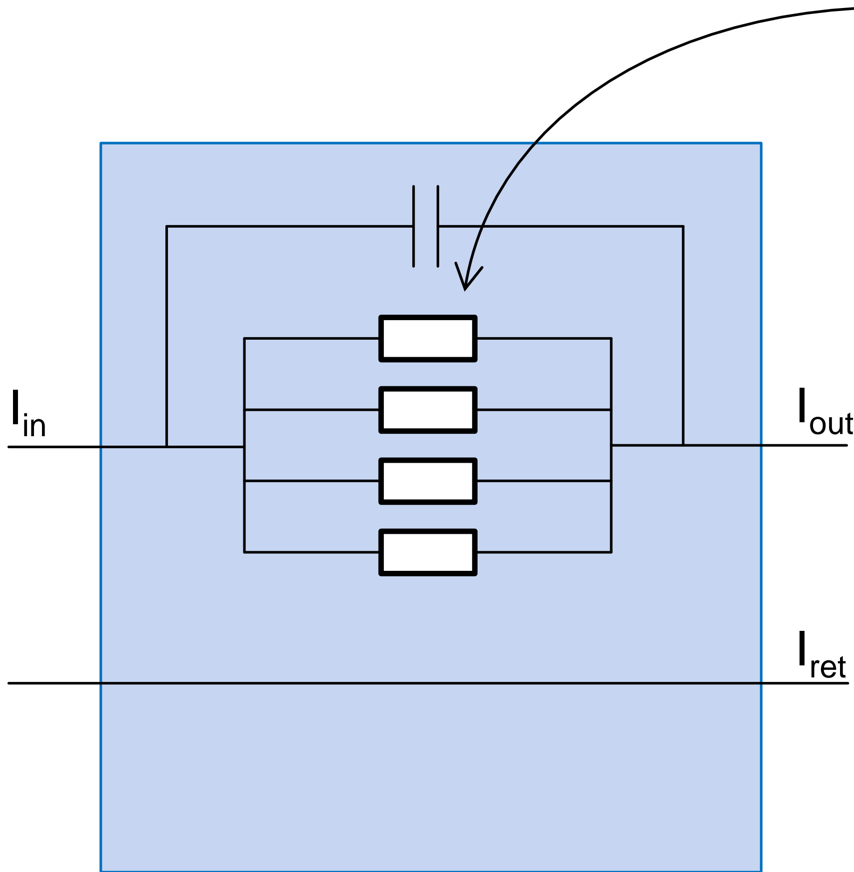
- Two major challenges:
  - Impedance and DC-resistance of eLink routing
  - Power dissipation in supply current and return current routing (of serial powering chain)
- Added a solid copper plane for return current routing
  → „closest possibility to a GND plane“
  → No problem in power dissipation of return current
  → crossing of signal lines (down-link) on bottom plane, still solid copper plane shielding the eLinks.
- Input current to chips on top layer plane
- Output current (input to next module) on bottom plane

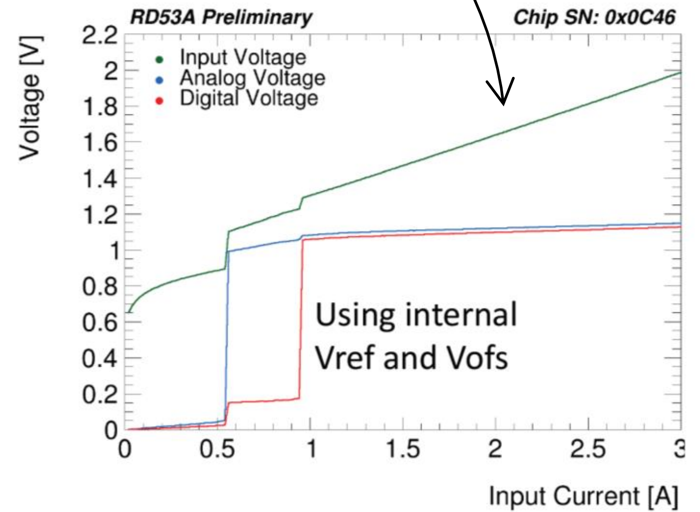


Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Coverlay	Surface Material	0.01016	Solder Resist	3.5
Top Layer	Signal	Copper	0.01		
Dielectric 1	Dielectric	Core	0.03	Polyimide	3.2
Internal Plane 1	Internal Plane	Copper	0.01		
Dielectric 2	Dielectric	Film	0.012		3.2
Bottom Layer	Signal	Copper	0.01		
Bottom Solder	Solder Mask/Coverlay	Surface Material	0.01016	Solder Resist	3.5
Bottom Overlay	Overlay				

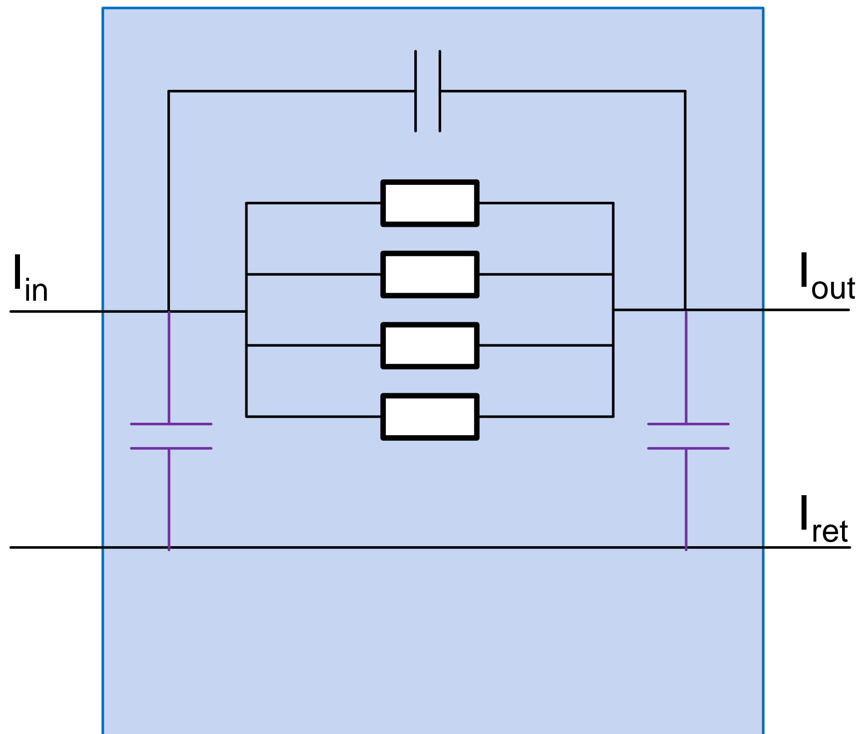
Simplified module

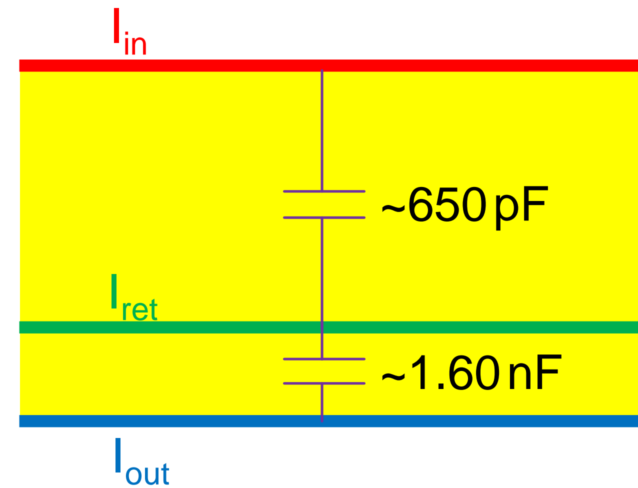
From system:
ohmic behavior with
voltage offset



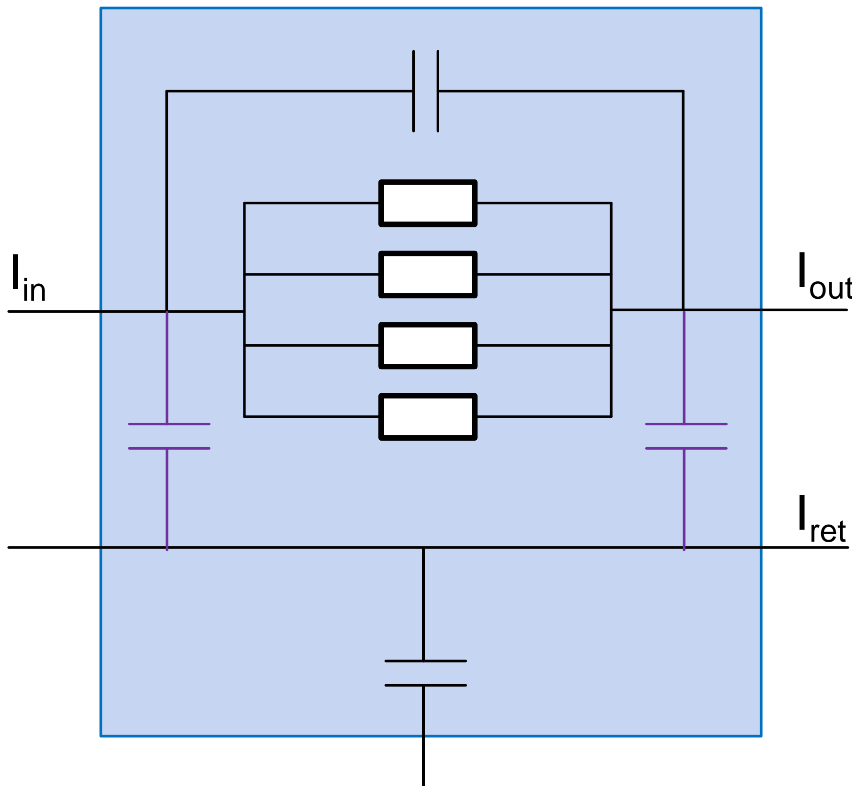


Parasitic capacitances





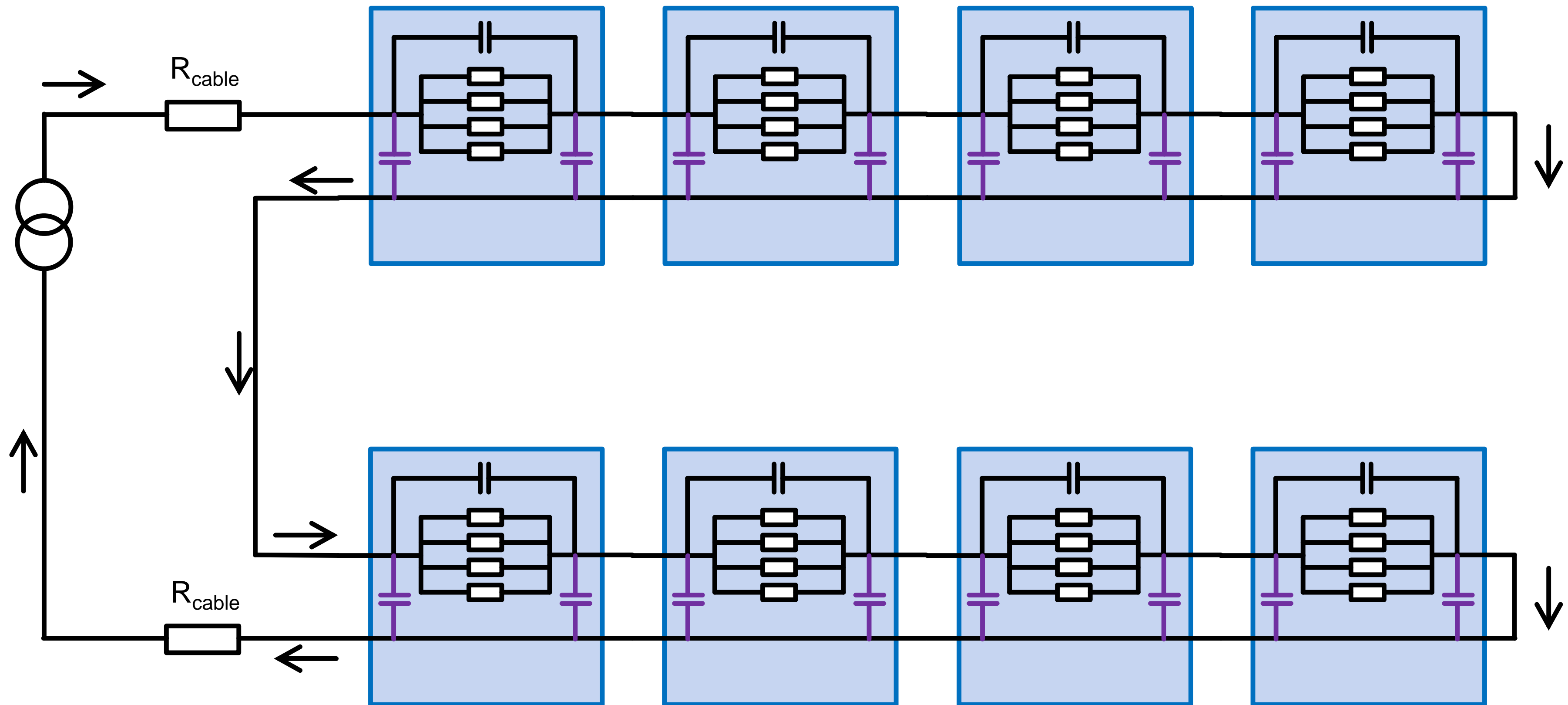
AC-coupled “GND plane”: I_{ret}



- Discussions with grounding and EMI experts ongoing
- ATLAS experts request a DC-coupled GND plane on each module “for shielding”
  → I (and also ATLAS module experts) don’t understand why, it **must not** be connected anywhere and is just parasitically AC-coupled…
- Discussion with Fernando and Alvaro: add an optional cacitance connected to system GND to stabilize the I_{ret} plane
  →” AC-coupled GND plane”

→ This allows to modify the resonance frequency of the circuit.

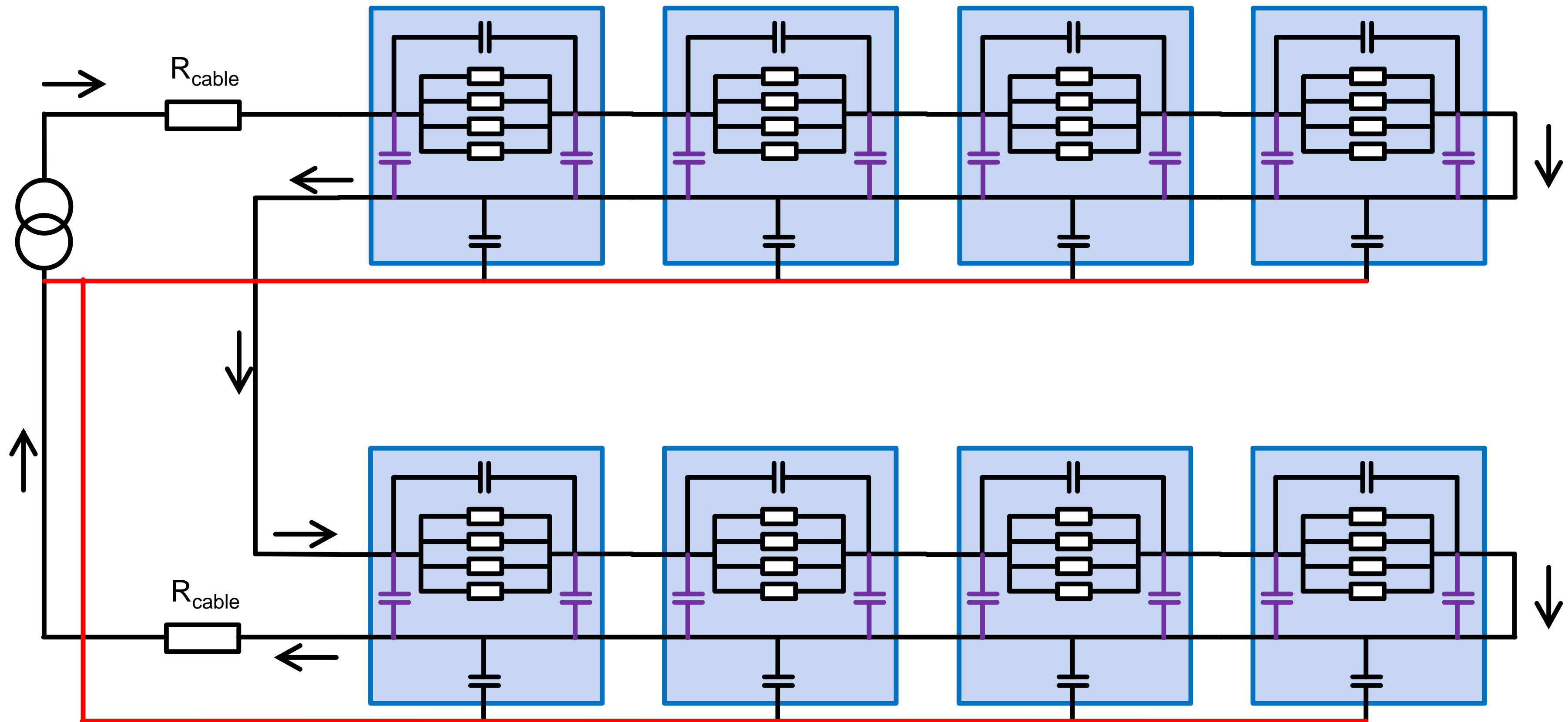
Serial Powering Chain without AC-coupled I_{ret}



ETH zürich

Serial Powering Chain with AC-coupled I_{ret}

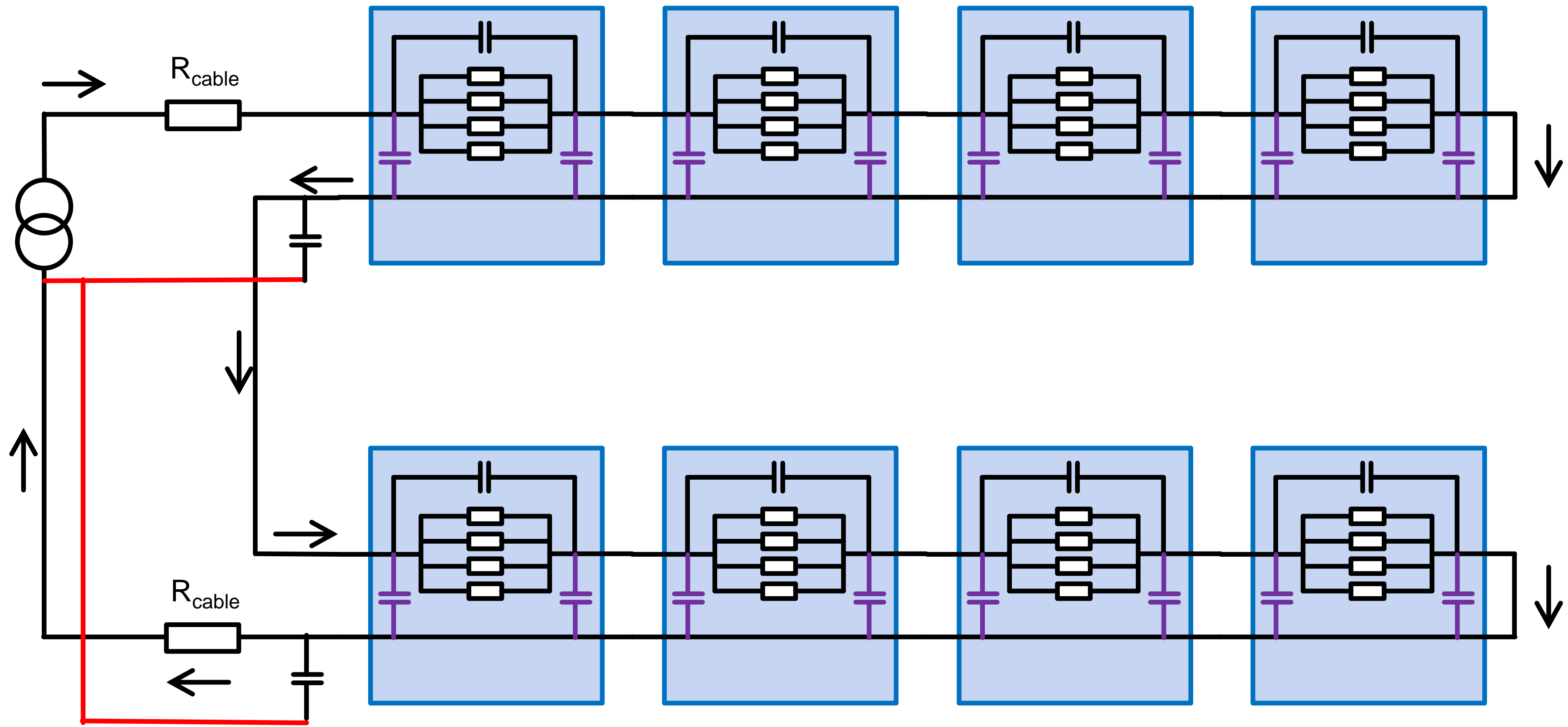
Option 1



IPA

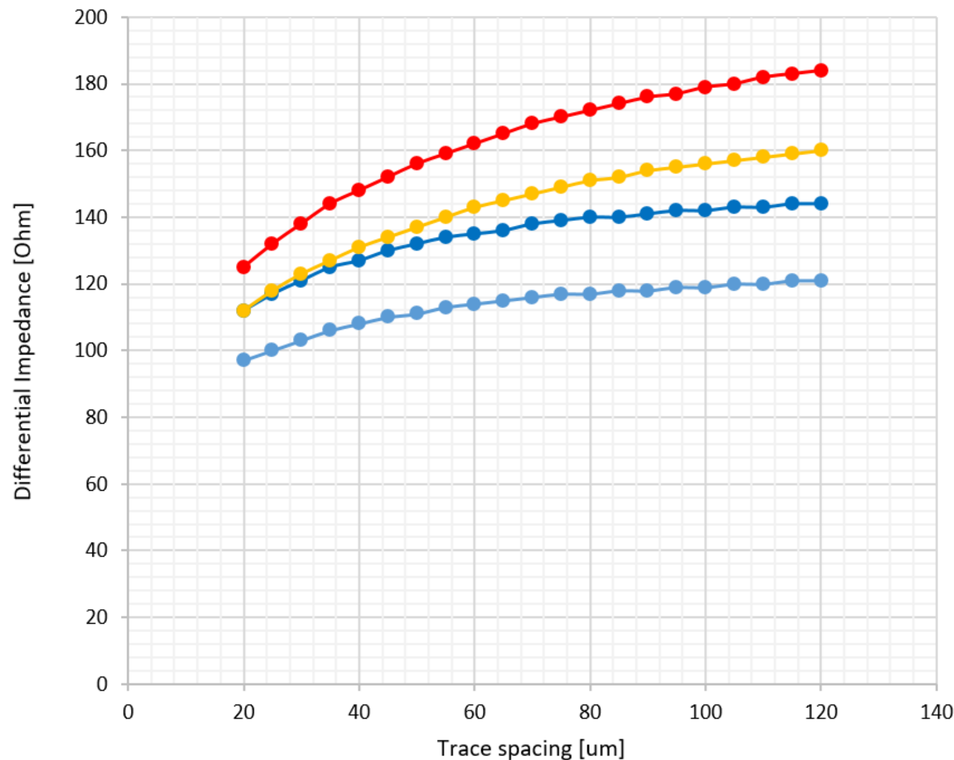
Serial Powering Chain with AC-coupled I_{ret}

Option 2



LVDS differential impedance: trace spacing

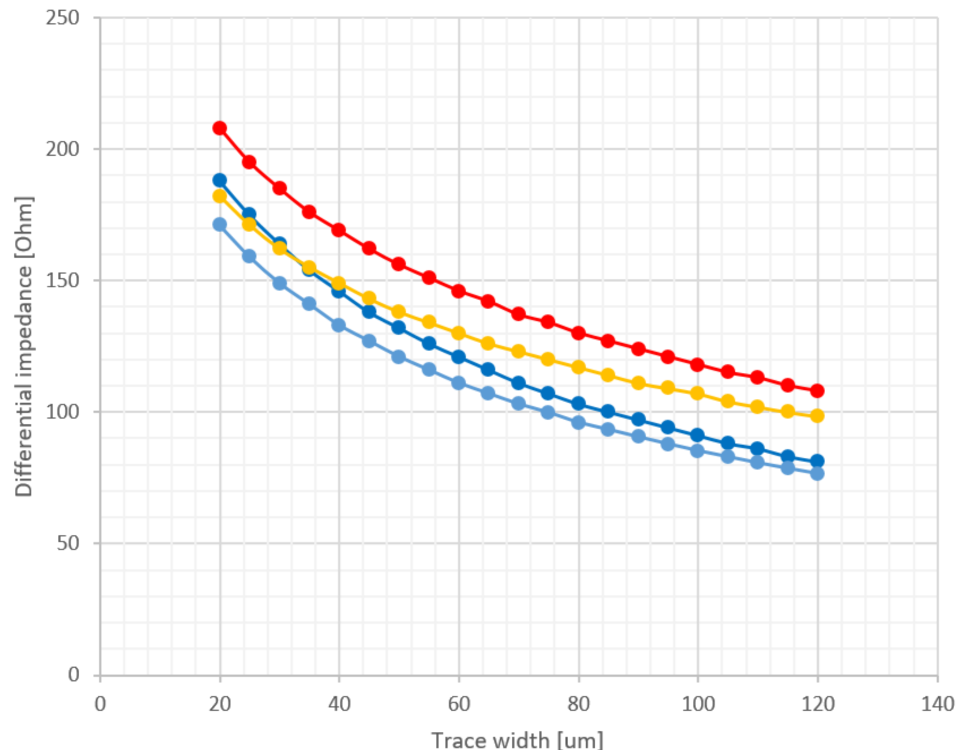
- Calculated the differential impedance for different dielectric thicknesses, trace widths, and trace spacings



→ 20um spacing variation (50%) results in 8 Ohm impedance variation (< 10%)

LVDS differential impedance: trace width

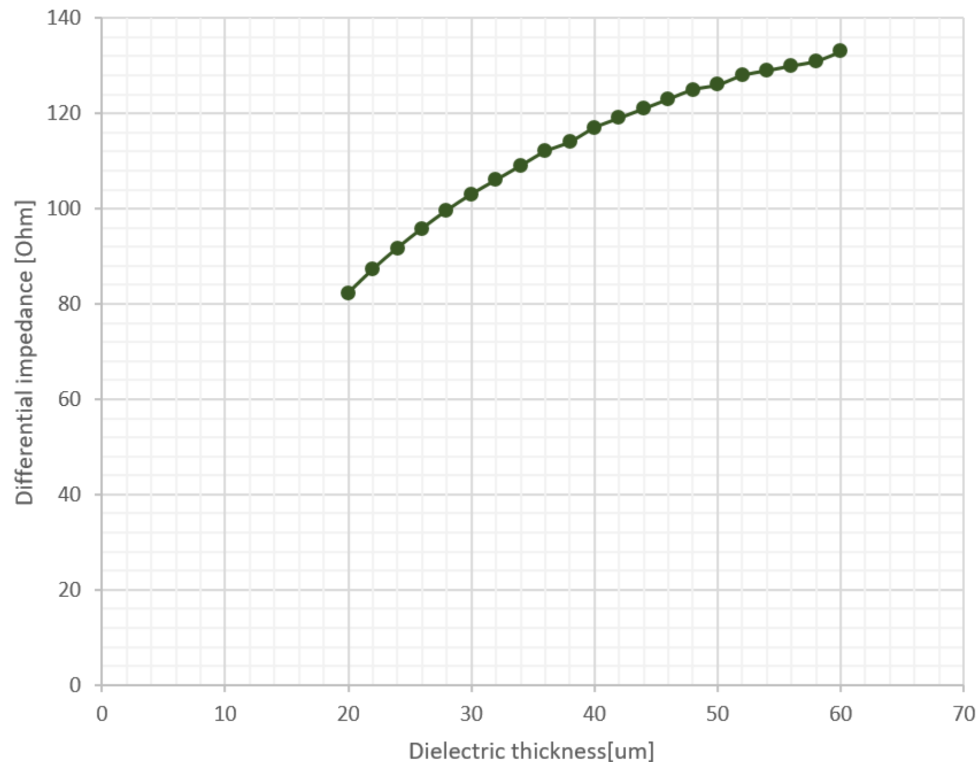
- Calculated the differential impedance for different dielectric thicknesses, trace widths, and trace spacings



→ 20um width variation (25%) results in 18 Ohm impedance variation (< 20%)

LVDS differential impedance: trace width

- Calculated the differential impedance for different dielectric thicknesses, trace widths, and trace spacings



→ 8 um width variation (27%) results in 13 Ohm impedance variation (< 15%)

LVDS line check

- Alvaro and Fernando (ITAINNOVA) are checking with HSS-Siwave
  - Impedance simulation,
  - Power distribution,
  - Crosstalk,
  - Noise

  based on the actual layout

- DC resistances:
  - < 0.6 Ohm per line, ~1.2 Ohm per link (on HDI only)

HDI power consumption: rough estimation

Assume half current (RD53A vs. final ROC) at half area…
→ 4 chips x 1 A max. = 4 A

- On pigtail:
  - Length: 4.5 mm, width: 3.8 mm, thickness: 10 um
    → pigtail resistance: <0.2 Ohm per line
    → power consumption pigtail: < 2 x 32 mW (I_{in} + I_{ret})
- On module:
  - I_{in}: estimated current and resistance of long wires and bottlenecks
    → power consumption: ~75 mW
  - I_{out}: estimated current and resistance of long wires and bottlenecks
    → power consumption: ~40 mW
  - Iret: plane + connector routing
    → ~30 mW
- **Total: ~210 mW !**
  → Significant power consumption on the module HDI

Summary

- Phase 2 module developments started last year
  → WG can build on significant experience in two CMS pixel detectors, and also ALTAS
- Now work concentrates on RD53A modules
  - HDI
  - test system
  - assembly procedures

  → they will be one of the work horses for further R&D:
  - Wire bond protection
  - Spark mitigation
  - eLinks
  - serial powering system validation
  - etc.
- A lot of further interesting ideas around. Although time is limited, we should look also away from baseline…