TFPX/Modules Considerations

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Some slides for the June 2018 EPIX/FPIX Workshop

Outline

The outline of this talk is (not surprisingly) quite similar to the talk prepared for the May tracker week.

1. Understanding electrical and mechanical constraints for HDI design
   - Mainly focusing on 1x2 HDI design
2. Thermal mock-up modules
3. Parylene-N coating for spark mitigation

TFPX HDI Design Issues

- Tightly coupled electrical/mechanical/thermal constraints
- Need a relatively realistic design to begin meaningful discussions with flex circuit vendors
- Necessary to understand which components and materials need to be qualified for radiation hardness using inexpensive test structures

HL-LHC US CMS

TFPX HDI Design Issues

- Basic material properties:

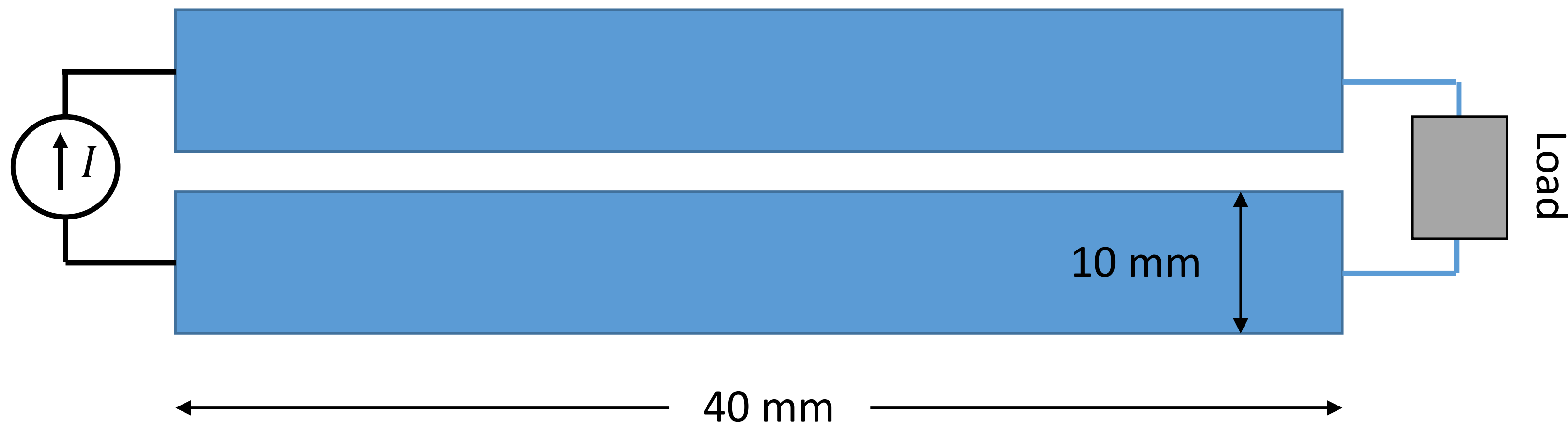
Material	X_0 (cm)	λ_I (cm)	κ	G (mho/cm)
Silicon	9.370	46.52	-	-
Copper	1.436	15.32	-	5.959×10^5
Aluminum	8.897	39.70	-	3.500×10^5
Polyimide	28.57	60.20	4.3	-
G10-FR4	16.76		4.5	-

- Properties of conductor planes:

Material	Thickness (µm)	X_0 (%)	G (mho)
¼ oz Copper	8.75	0.061	521
½ oz Copper	17.5	0.122	1042
Aluminum	14.9	0.017	521
Aluminum	29.8	0.033	1042

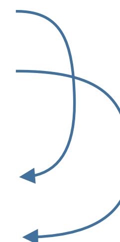
Conductor Plane Designs

- Zeroth order geometry:



- Nominal current: $I = 5\ A$

Material	t (um)	X/X0 (%)	R (mΩ)	ΔV (mV)	P (mW)
1/4 oz Cu	8.75	0.122	15.34	76.71	383.57
1/2 oz Cu	17.5	0.244	7.67	38.36	191.79
Al	8.75	0.020	26.12	130.61	653.06
Al	15.00	0.034	15.24	76.19	380.95
Al	30.00	0.067	7.62	38.10	190.48
5/30 Cu/Al	35.00	0.089	5.93	29.67	148.37



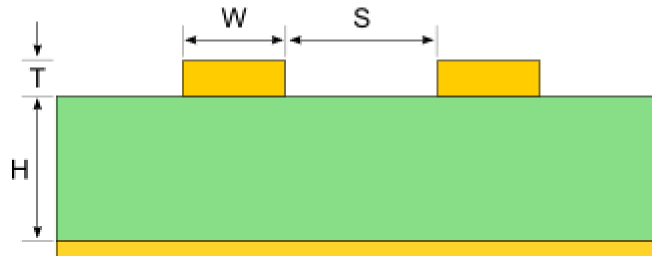
- Aluminum might reduce radiation length by factor of 4.

Conductor Plane Designs

- Radiation length of sensor+ROC is about 0.4%
  - Assuming a 200 µm thick sensor and a 150 µm thinned readout chip, not including bumps
- Half-ounce copper would amount to 40% of the total radiation length.
  - Total radiation length is 0.61% X_0
- 5/30 µm copper clad aluminum foil would be 20% of the total radiation length.
  - Total radiation length is 0.46% X_0
- Disadvantage of aluminum is that vias between layers are problematic.

Differential Pair Designs

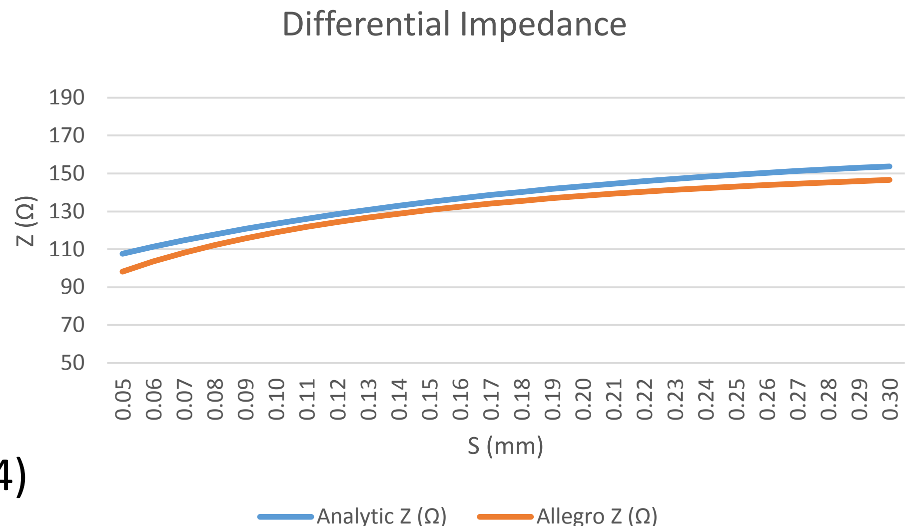
- Some pedagogy:



$$Z = \frac{(174\ \Omega)}{\sqrt{\varepsilon_r + 1.41}} \log\left(\frac{5.98 \times H}{0.8 \times W + T}\right)\left(1 - 0.48\, e^{-0.96 S/H}\right)$$

- Typically only good enough for scaling relations

$\varepsilon_r = 4.5$ (FR-4)
$T = 0.009\ mm$ (1/4 oz copper)
$H = 0.15\ mm$
$W = 0.10\ mm$



More detailed treatment in IPC-2141A (2004)

Differential Pair Designs

- HDI technology determines minimum trace with and spacing
- Larger values have advantages:
  - More vendors will place bids
  - Yields will be higher
  - Cost will be lower
  - Lower project risk
- Typical design rules:

$$W, S \geq 76.4\ \mu m\ (3\ \text{mils})$$

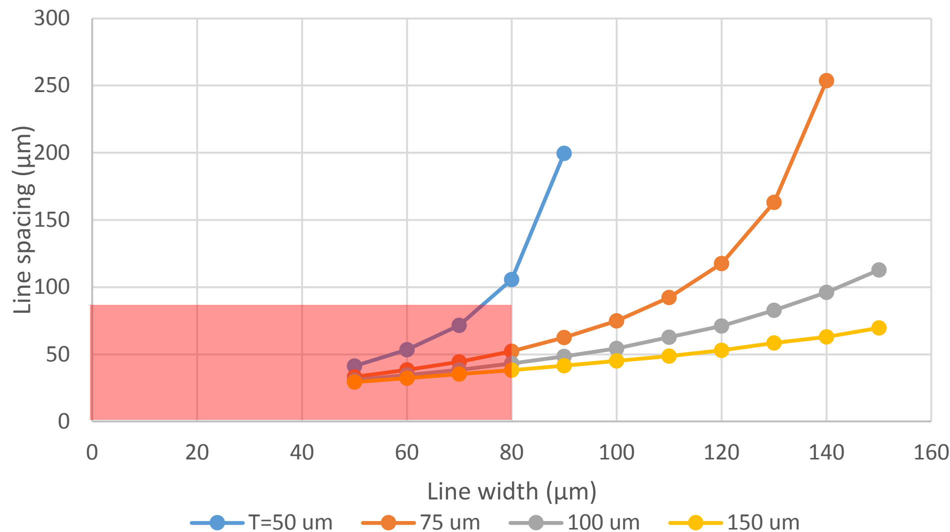
- Conservative rules:

$$W, S \geq 89\ \mu m\ (3.5\ \text{mils})$$

- Vendors with much more aggressive rules do exist.

Differential Pair Designs

- Controlled impedance line width/spacing
  - Polyimide dielectric (ε_r=3.5), 10 µm thick solder mask
  - 8.75 µm conductor thickness
  - 100 Ω edge-coupled stripline
  - Calculated with Cadence/Allegro field solver



This seems to indicate that a dielectric thickness of between 50 and 75 µm may be optimal for easily achievable design rules.

Differential Pair Designs

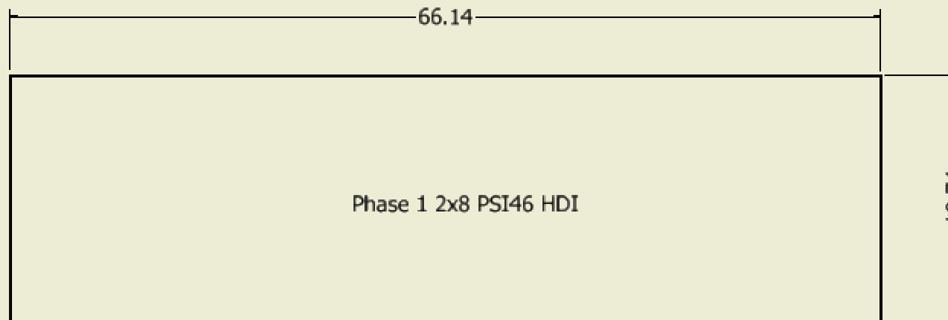
- The nominal target of 100 Ω differential impedance may not be critical provided the transmission lines are terminated appropriately
- Serial powering requires AC coupling of all differential pairs and their local ground reference
  - Must we place these capacitors on the HDI?
  - This would minimize material at small R
- Width of all differential pairs:

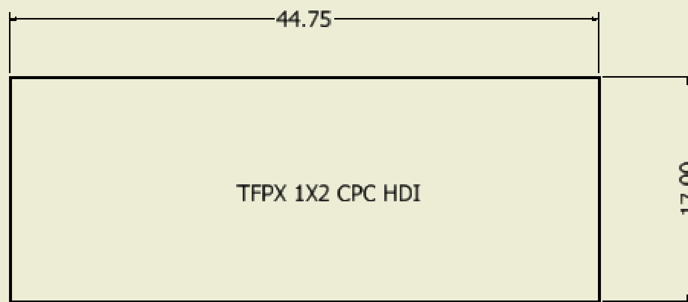
$$W = n \times (2w + s) + (n - 1) \times p$$

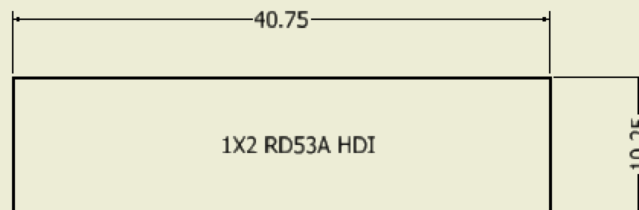
  - $n = 9$ (8 high speed links + 1 clk/cmd)
  - $w = 100\ \mu m,\ s = 190\ \mu m$
  - $p = 500\ \mu m$

$$W = 7.5\ mm$$

TFPX HDI Physical Size







This is getting pretty small…

(dimensions are in millimeters)

At least for the 1x2 HDI's, the circuit could extend past the edge of the module opposite the wire bonds.

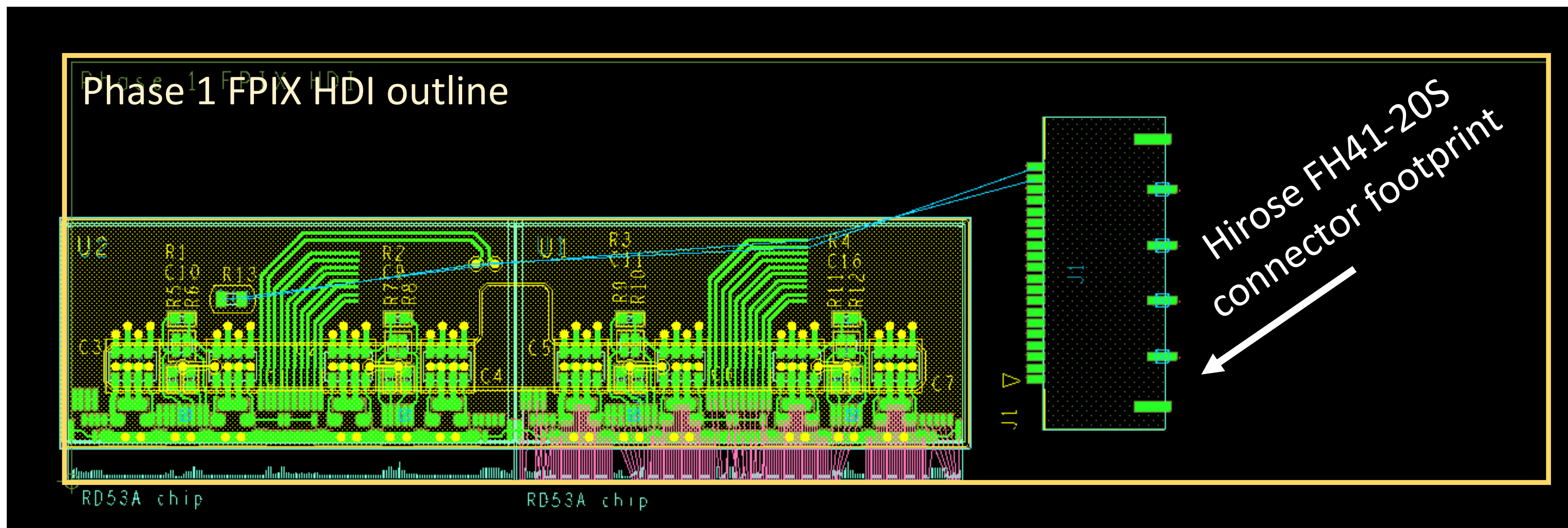
Nominal sizes: probably close but might change slightly.

TFPX HDI Physical Size

- To relax physical size constraints for the RD53A 1x2 HDI, the circuit could extend beyond the edge of the sensor opposite the ROC wire bonds.
- An RD53A HDI and a CPC HDI could have the same physical size even though the ROC's are different sizes.
- This would provide room for a ZIF connector.
  - The Phase 1 SMK EF-5D series connector is nice
  - Possible alternative: Hirose FH41-20S
- Alternatively, do away with the ZIF connector on the HDI and wire bond directly to a pigtail flex cable

TFPX HDI Physical Size

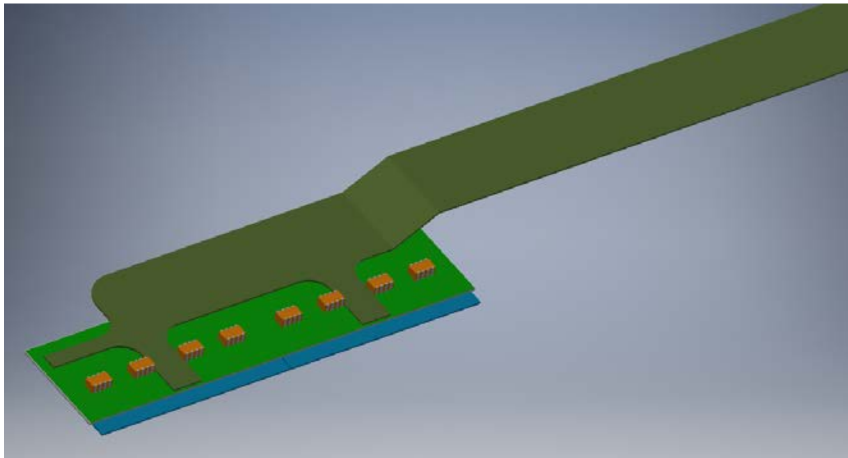
- Confronting design issues with 1x2 RD53A type HDI



- Observations:
  - Likely can be routed using mostly >100 μm line widths/spacing
  - Probably won't be able to implement development interfaces
    - Drop JTAG, alternate command input, MUX output
  - Connector size may be an issue
  - Need to implement some kind of mechanical mounting elements
  - May benefit from discrete components in array packages

Component selection

- Current design considerations:



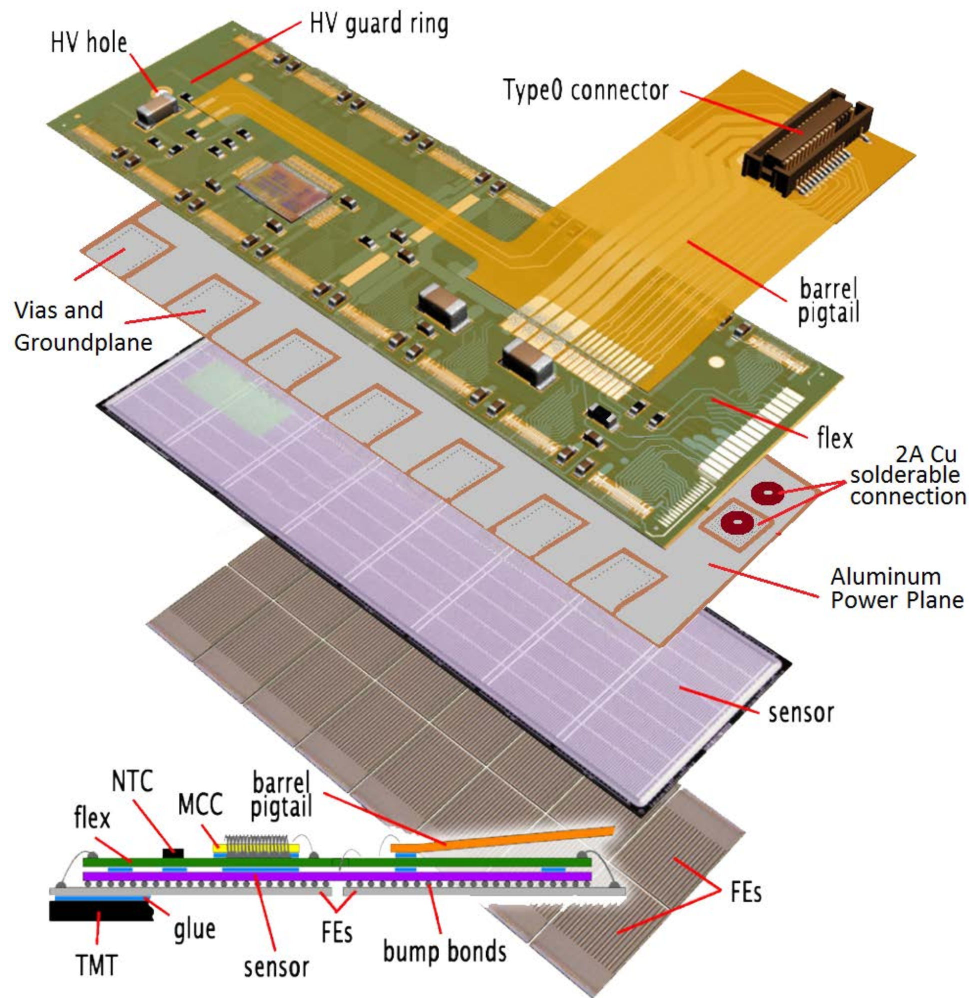
Conceptual design of a pigtail signal/bias voltage flex cable

Still need to provide (lots) of DC current…

- Capacitor arrays can save space:
  - 4 capacitors in a 2.1 x 1.3 mm package
  - Reduces number of discrete components to assemble
  - But maximum value is 0.1 μF
- Higher values (eg, up to 10 μF) in larger packages can be placed further from bond pads.
- Need to qualify these components for radiation.

Aluminum circuits?

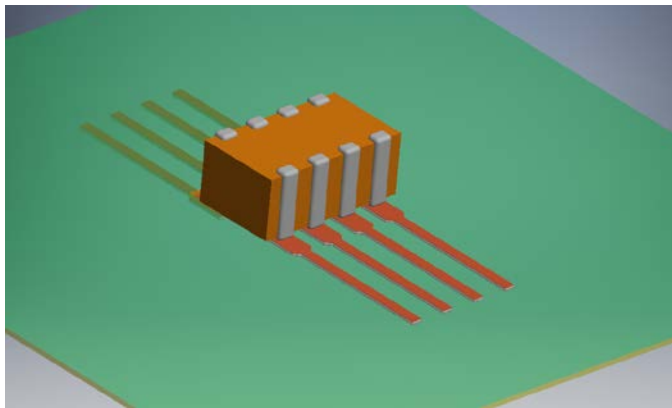
- We contacted a company (Omni) that produces aluminum flex circuits.
  - They use copper cladding as the mask during etching
  - Copper also adheres well to polyimide
- Constraints:
  - Vias in aluminum are challenging
  - Un-etched copper contributes to radiation length (5 μm)
- Need a good model for current flow in power and ground planes.
  - Installing Allegro tools for DC power modeling
  - How thin can copper power planes be made?
  - Is Aluminum really worth it?

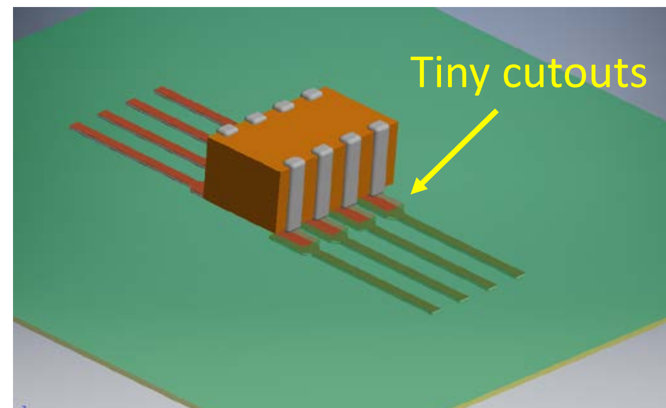


Omni circuits proposed this design based on the Phase 1 module.

Aluminum Circuits?

- Vias in aluminum are apparently not an option.
- Possible solution for filtering power planes:





- Laser ablation apparently costs $65k per cubic inch
  - Volume of polyimide removed here is $3 \times 10^{-8}\ \mathrm{in}^3$
  - This appears to be cost effective

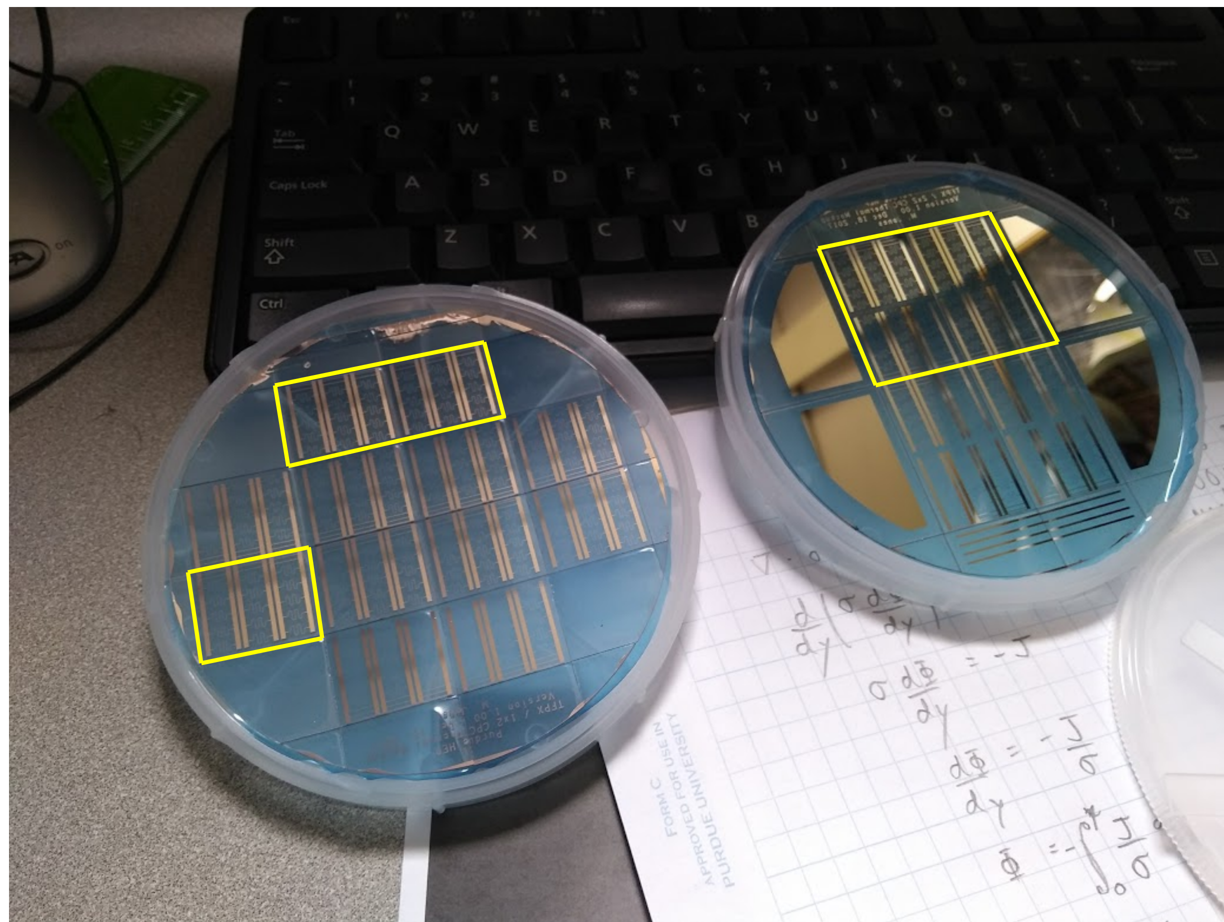
Thermal Mock-ups

Fabricated single-chip, 1x2 and 2x2 mock-ups of full-sized CPC chip modules.

Each mock-up chip can dissipate up to about 8 watts.

Wire bond pads vaguely approximate RD53A design.

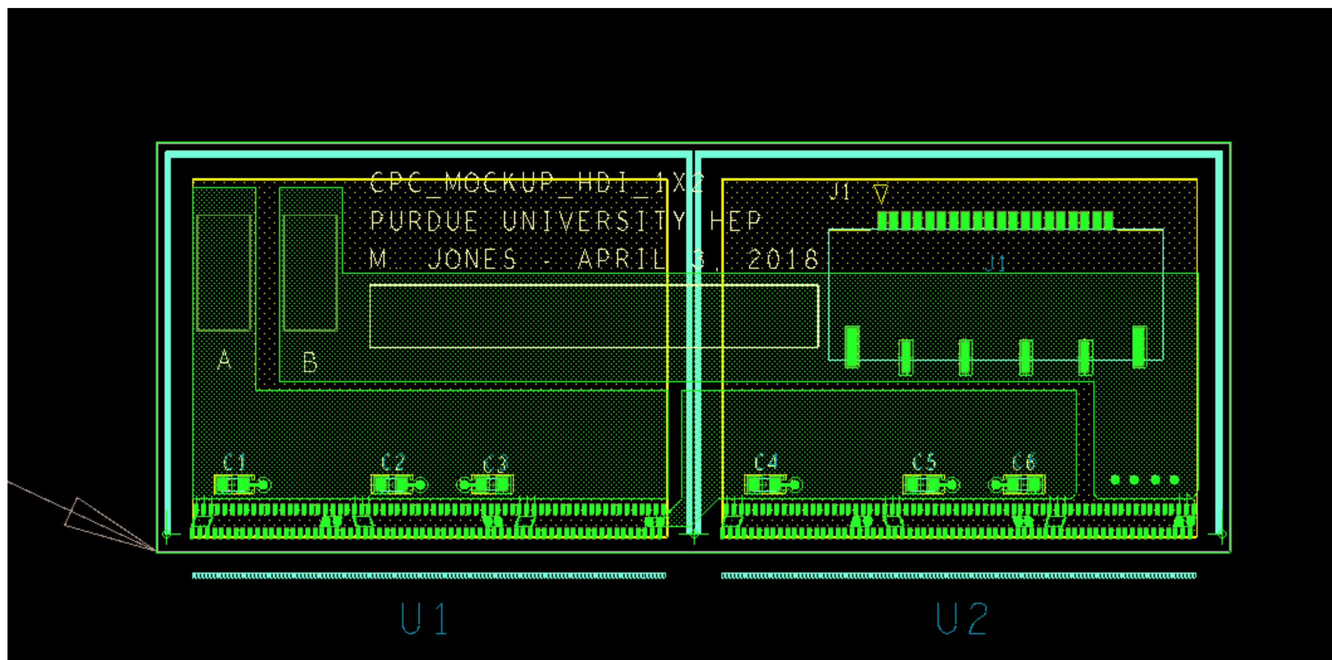
Needed for thermal/mechanical interface studies.



Please let me know if you would like any. We can make more…

"HDI" for thermal mock-ups

- Originally intended to begin the process of qualifying candidate HDI vendors.
- Best option appears to be to fabricate using a low-cost conventional 2-layer circuit
- Provides an opportunity to irradiate candidate components and materials used for assembly.



"HDI" for thermal mock-ups

- Planned changes to the first design concept:
  - Most of the advantages of high density flex circuits are not relevant for thermal testing
  - Therefore, submit a simple 2-layer conventional copper circuit.
  - Still useful to provide placement for components that may be selected for the RD53A/CPC HDI
    - Capacitor arrays
    - Tantalum capacitors
    - Resistors
    - Solders
    - Epoxies
    - Encapsulants
  - Test before and after irradiation campaign
  - Do we need to provide DC power during irradiation?

Spark Mitigation Strategies

The back-side and edge of the sensor are biased but the readout chip is at ground potential. Regions with large electric fields are prone to sparking.

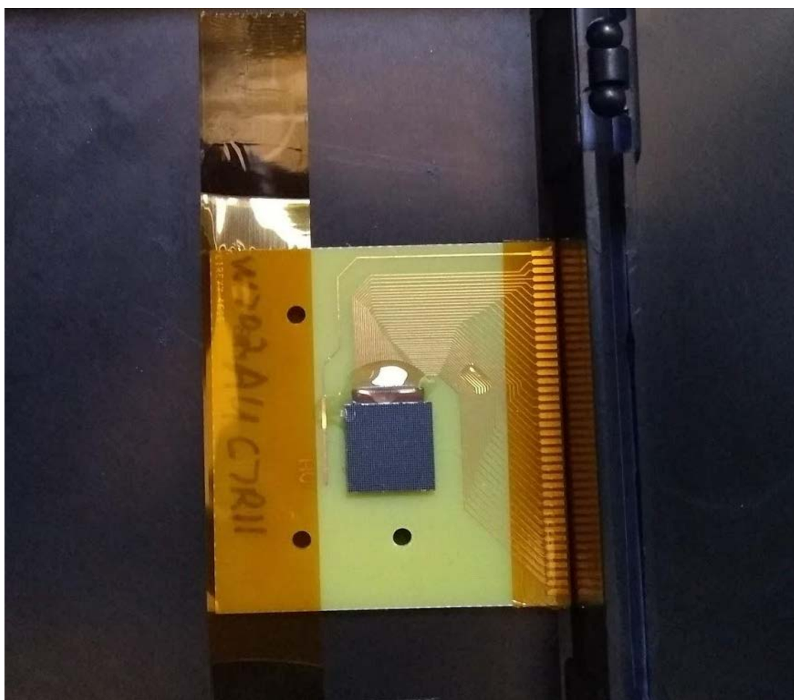
Guard ring

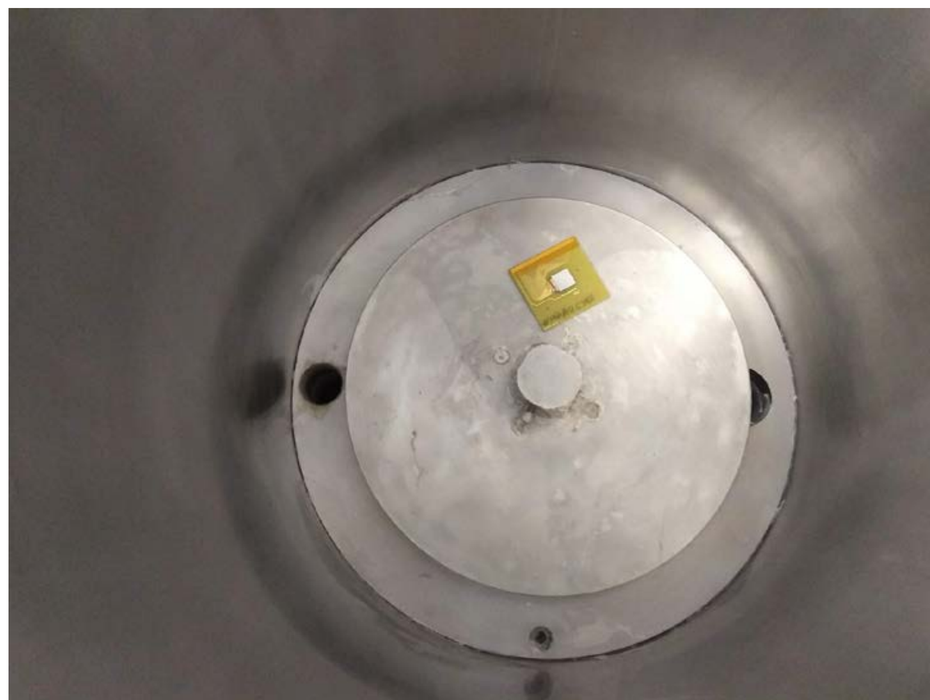
Sensor

Readout chip

Parylene-N Coating Process

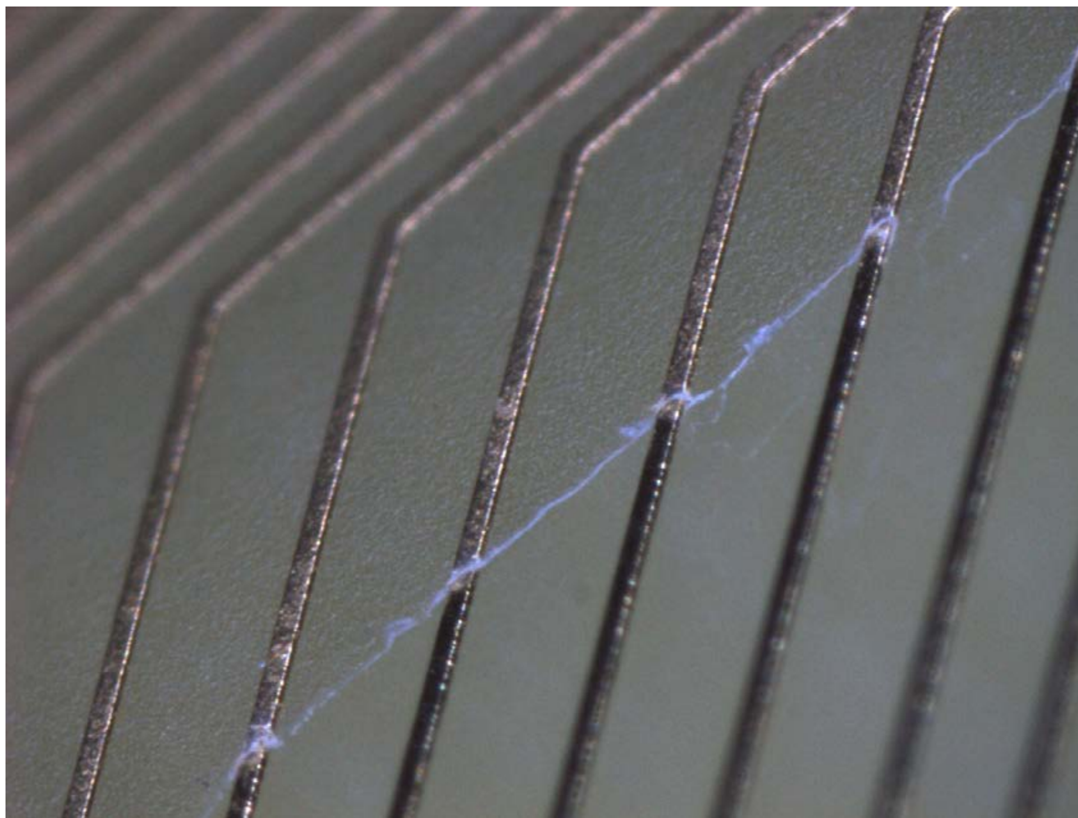
- Initial experience based on only one device:
  - Did not use an adhesion promotor
  - Masked electrical connections with Kapton tape
  - Deposited 4 um of Parylene-N





Unmasking Electrical Connection

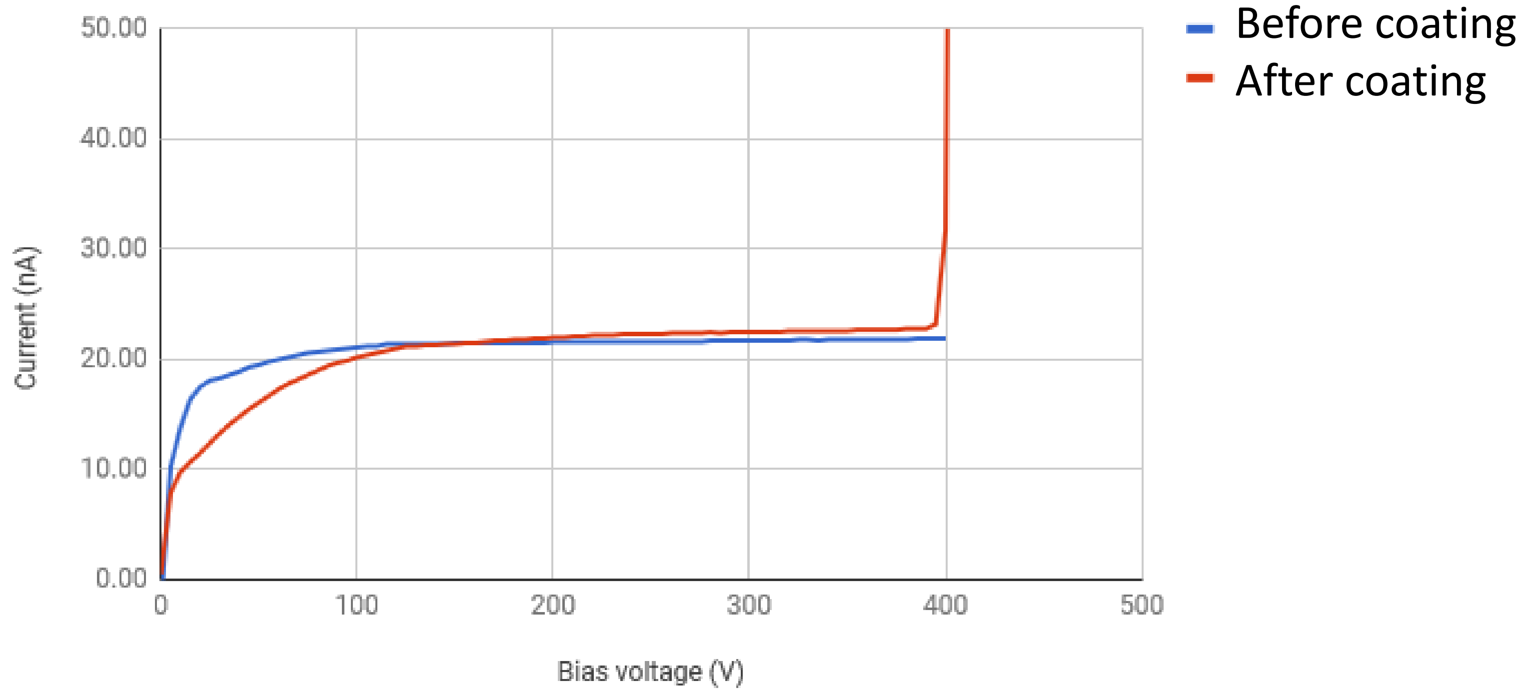
- Clean removal of Kapton tape:



Preventing Parylene from coating the internal parts of, for example, a ZIF connector will be more difficult.

Properties after coating

- Leakage current essentially unchanged after coating
- Breakdown occurring very close to 400 volts

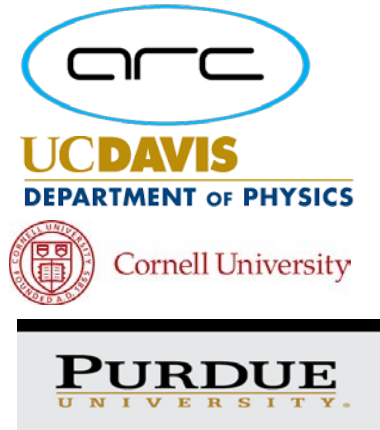


What Have We Learned?

- Parylene deposition process is straight forward
- Masking macroscopic electrical connections with Kapton tape seems to work well
- Breakdown observed at around 350-400 volts.
- Two possibilities:
  1. Breakdown voltage before coating was significantly higher than 400 volts and was reduced to about 400 volts after coating.
  2. Breakdown voltage before coating was about 400 volts and was changed slightly after coating.
- Not entirely sure how to prove that the breakdown is in the sensor and not in the gap between the sensor and ROC.

Investigation of other dielectrics

- Research partnership:
  - Advanced Research Corporation (Greg Wagner)
  - University of California – Davis (Mani Trepathi)
  - Cornell University (Julia Thom)
  - Purdue University (Matthew Jones)



- Research goals:
  - Investigate a number of dielectrics that are likely to be rad-hard
  - Model the electric field in the regions where breakdown is likely
  - Build test structures that accurately represent bump-bonded module geometries
  - Irradiation campaigns
  - Focus industrial scale application with an eye towards commercialization

Investigation of other dielectrics

- Modeling electric fields using COMSOL

Surface: Electric field norm (V/um)

Investigation of other dielectrics

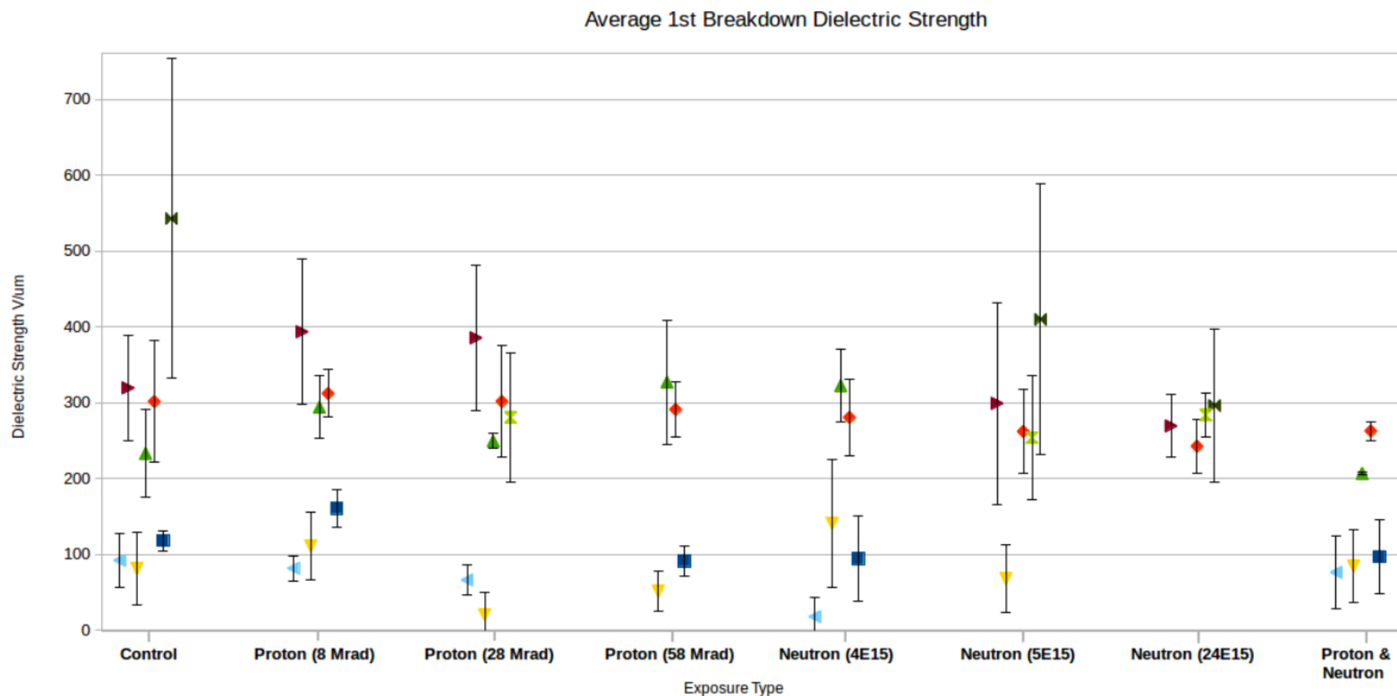
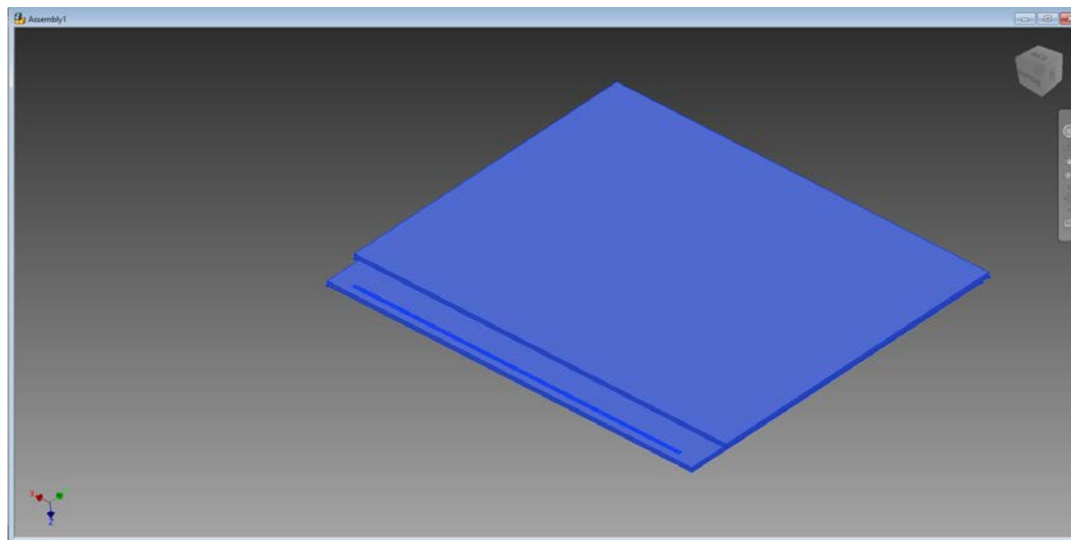


Figure 10. Average 1st breakdown dielectric strength $[V/\mu m]$ sorted by exposure type for each material. The error bars represent the standard deviation of the dielectric strength

Investigation of other dielectrics

- Next steps:
  - Fabricate electrical-mechanical analogs
  - Geometry expected for full-scale CPC chip
  - 50 µm x 50 µm bump array, representative wire bond pads
  - Perform flip-chip assembly, test breakdown properties for various dielectrics before and after irradiation



Summary

- Working on mechanical/thermal/electrical concepts for TFPX HDI design
- Thermal mock-ups fabricated for studying heat transfer
- HDI design allows for radiation qualification of components and materials
- Two approaches to spark mitigation
  - Short term strategy with Parylene-N
  - Longer term solutions suitable for module production under investigation in collaboration with industry