TEPX module arrangements

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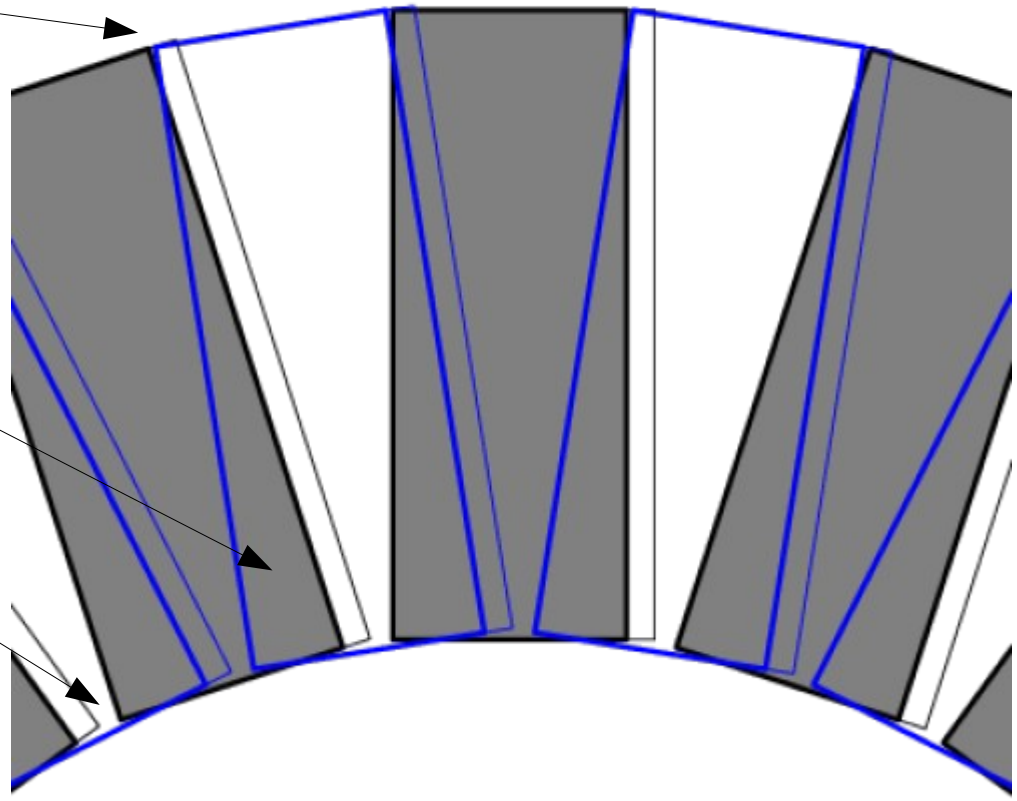
Inner Ring, TDR layout

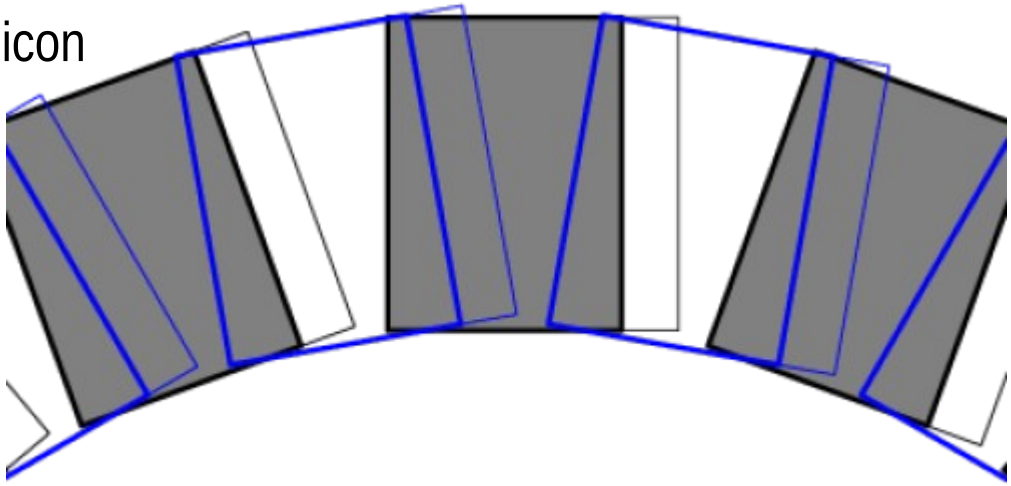
- 2x1 aspect ratio not ideal for ring geometry
- Outer radius
  - No overlap within ring

    (covered by next ring, this occurs in outer rings as well)
- Inner radius
  - A lot of (useless?) overlap
  - little clearance (2mm drawn)



Inner Ring, 1x1 layout

- 1x1 aspect ratio much more suitable
- Outer radius
  - sufficient overlap within ring, (with 18 modules)
  - Less radial overlap with next disk needed → saves silicon
- Inner radius
  - less unnecessary overlap → saves silicon
  - generous clearance (4 mm drawn)
    → potentially easier assembly



- Radial coverage:
  63.7 → 254.0 mm = 190 mm
  can be covered with 4x2 + 1
  including > 2 mm radial overlap* → saves 1 ring of ROCs

* = 1 mm in corners of outer rings

Fewer e-links and less data per link

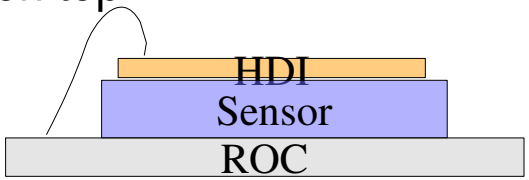
TDR	Ring 1	Ring 2	Ring 3	Ring 4	Ring 5	Total
#Modules	20	28	18	20	24	110
#ROCs	40	56	72	80	96	344
#elinks	20	28	18	20	24	110
#lpGBT	4	4	6*	4	*with Ring 3	18
#modules/lpGBT	5	7	7	5		6.1

Here	Ring 1	Ring 2	Ring 3	Ring 4	Ring 5	Total	
#Modules	18	26	18	20	24	106	-4%
#ROCs	18	52	72	80	96	318	-8%
#elinks	18	26	18	20	24	106	-4%
#lpGBT	4	4	6*	4	*with Ring 3	18	
#modules/lpGBT	4.5	6.5	7	5		5.9	

More details in Lea's talk

Module / HDI concepts

•HDI on top

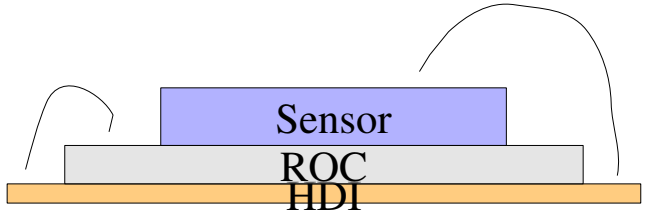


•minimal dead space around module

•1 x N or 2 x N geometry

•More complex arrangements need connections (and an extra carrier)

•HDI below ROCs



•Needs extra space for wire-bonding

•Easier assembly, no gluing onto sensor

•Flexible arrangements on single HDI without connectors / sub-assemblies

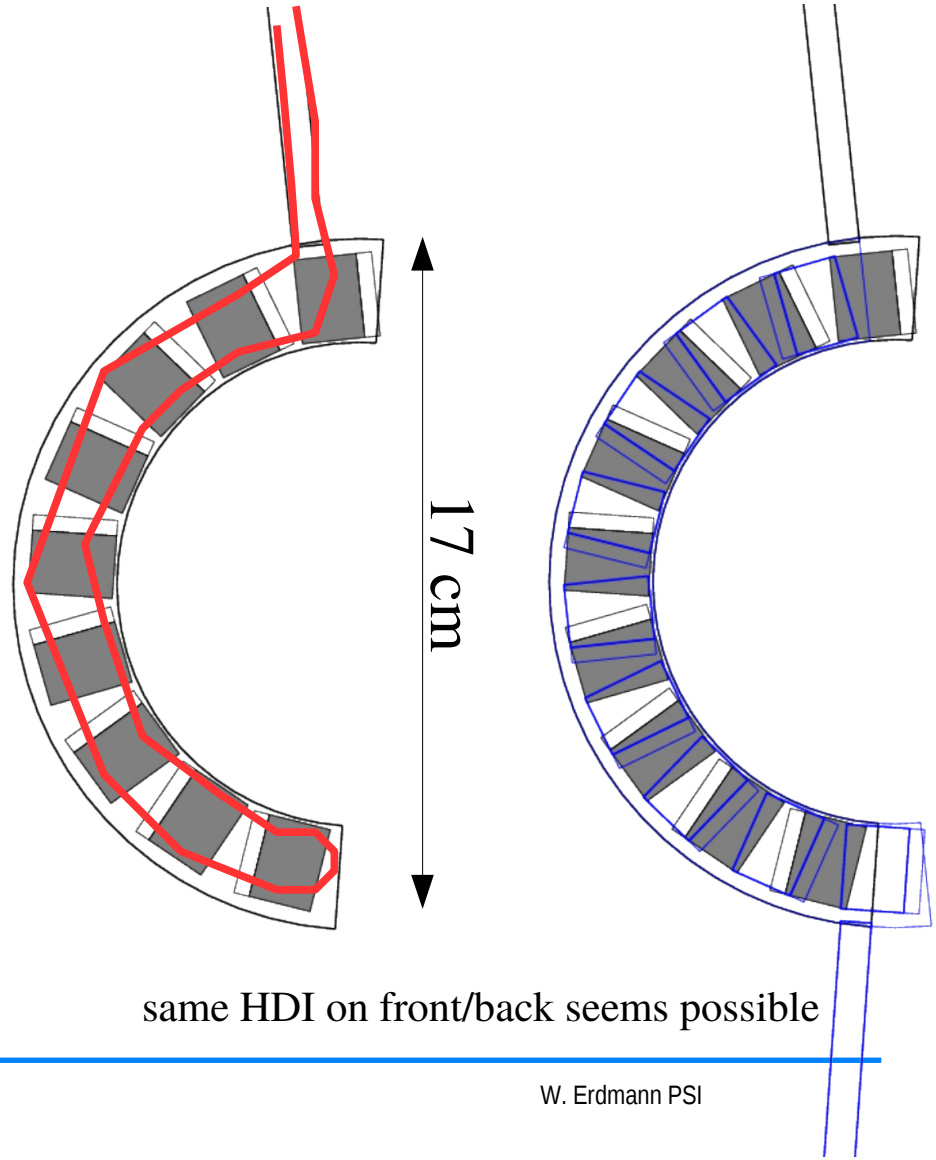
•Heat transfer through HDI

•2 K for 20 um Polyimide @ 1W/cm^2, 0.1W/mK

•4 K for 85 um Polyimide @ 1W/cm^2, 0.2W/mK

HDI concept for Ring 1

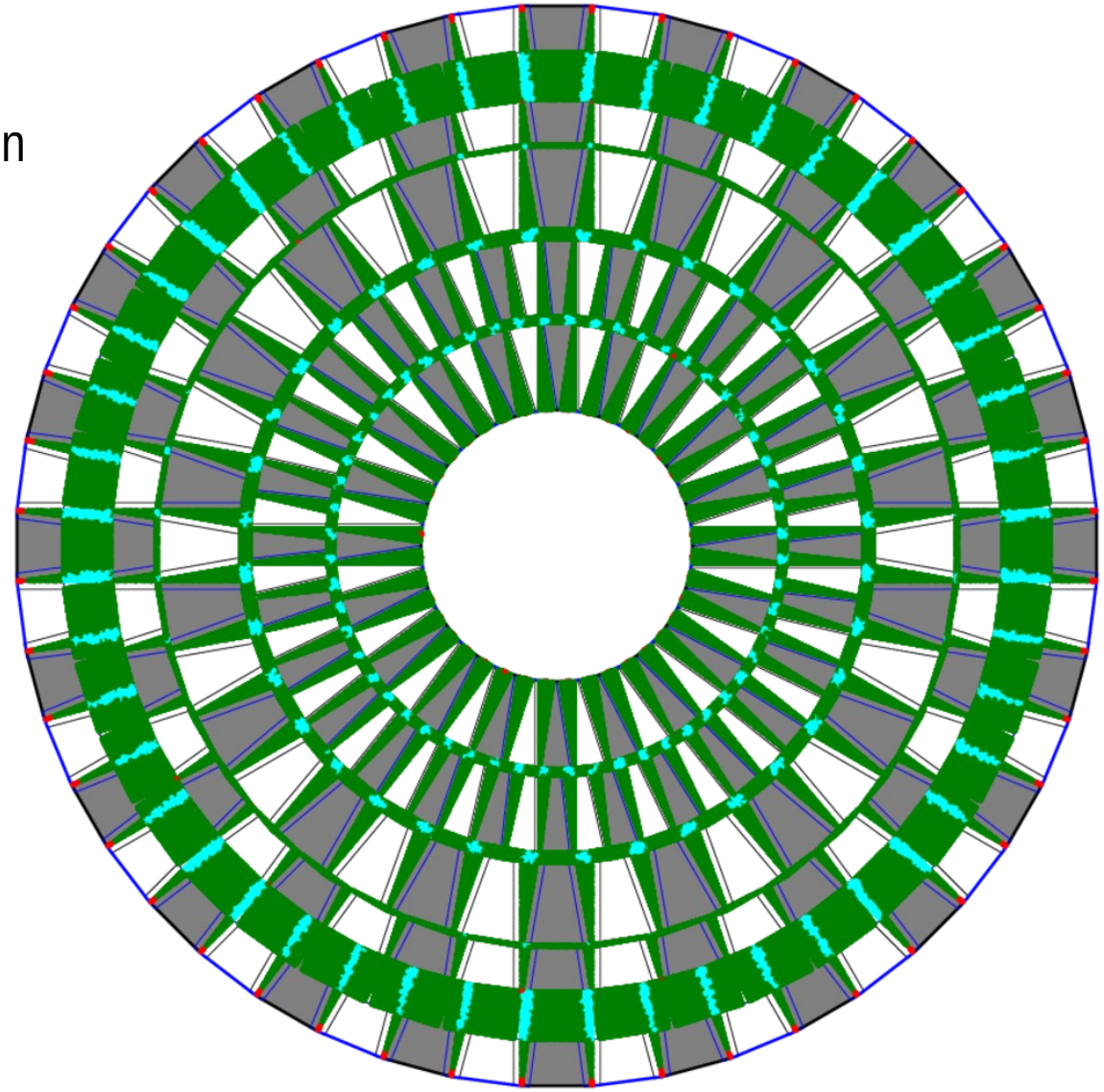
- 9 single ROC assemblies could form a unit
  - Elink/lpGBT rate ok
  - Serial powering
    - 3 x 3 allows bypassing “dead” modules
- Overall size managable
- To be clarified
  - single connector / integrated cable / mixed
  - Replacement of single Chips necessary?(yield)
  - Integration / Mechanics → Silvan’s talk



same HDI on front/back seems possible

Overlap

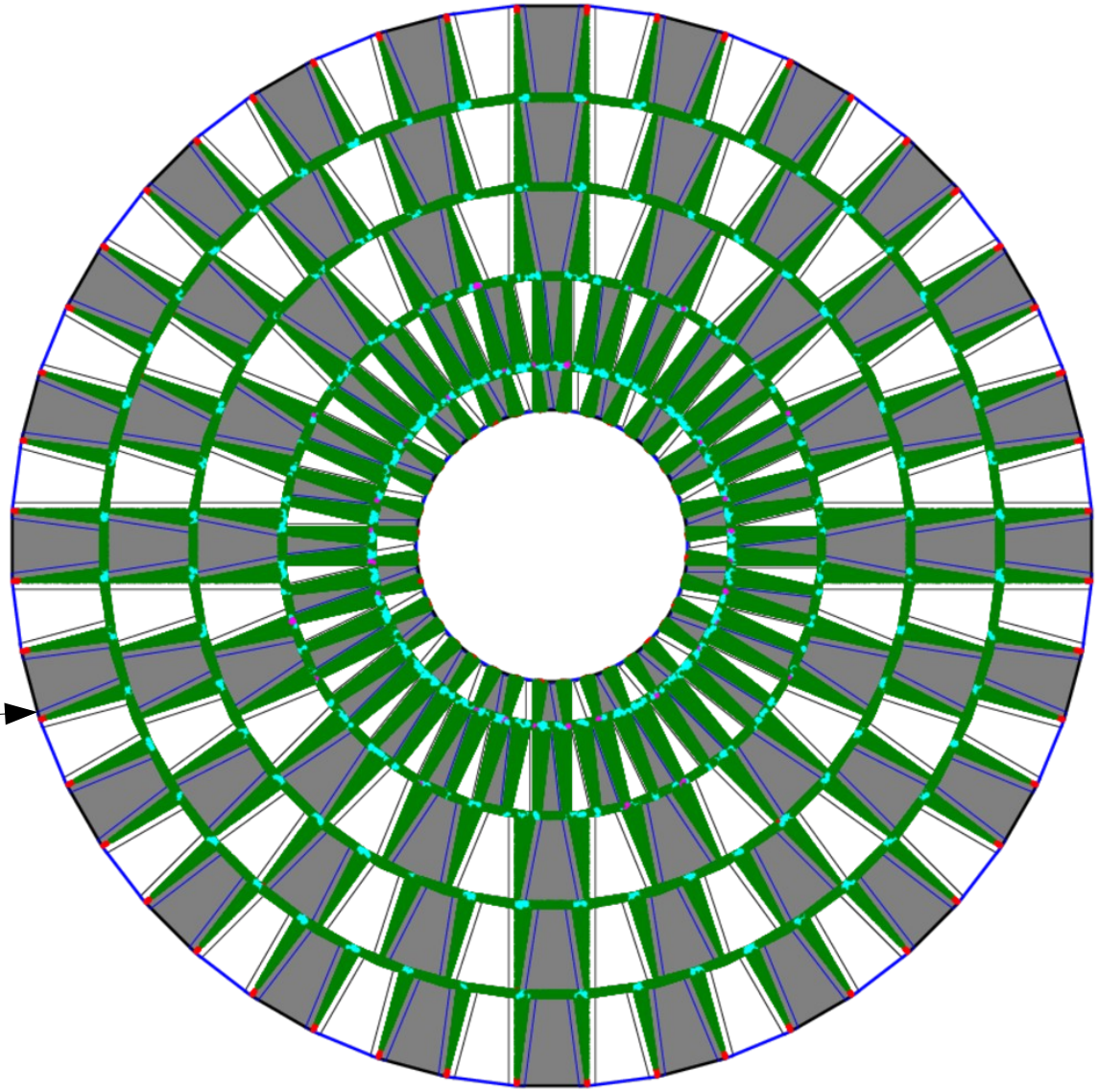
- Some overlap within disks is needed
  - Robustness against assembly precision
  - Helps alignment with tracks
  - Luminosity measurement
    - Unclear how much is needed
  - TDR layout has a lot of overlap between ring 4/5
- Picture:
  - Overlaps within one double disk
  - 2 hits (green) 25%
  - 3 hits (cyan) 3%



Reduced outer radius

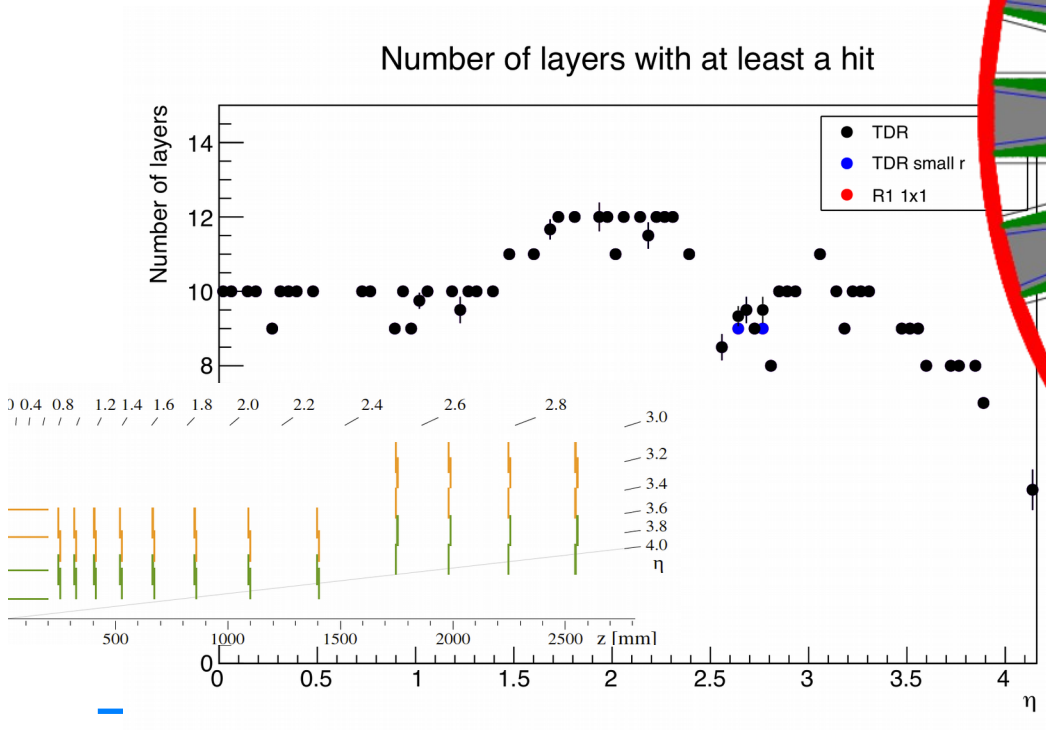
- 2 mm overlap everywhere
- 2 hits (green) 17% (TDR 25%)
- 3 hits (cyan) 1% (TDR 3%)
- Most of the reduction between ring 4/5
- Does it matter where the overlap is?

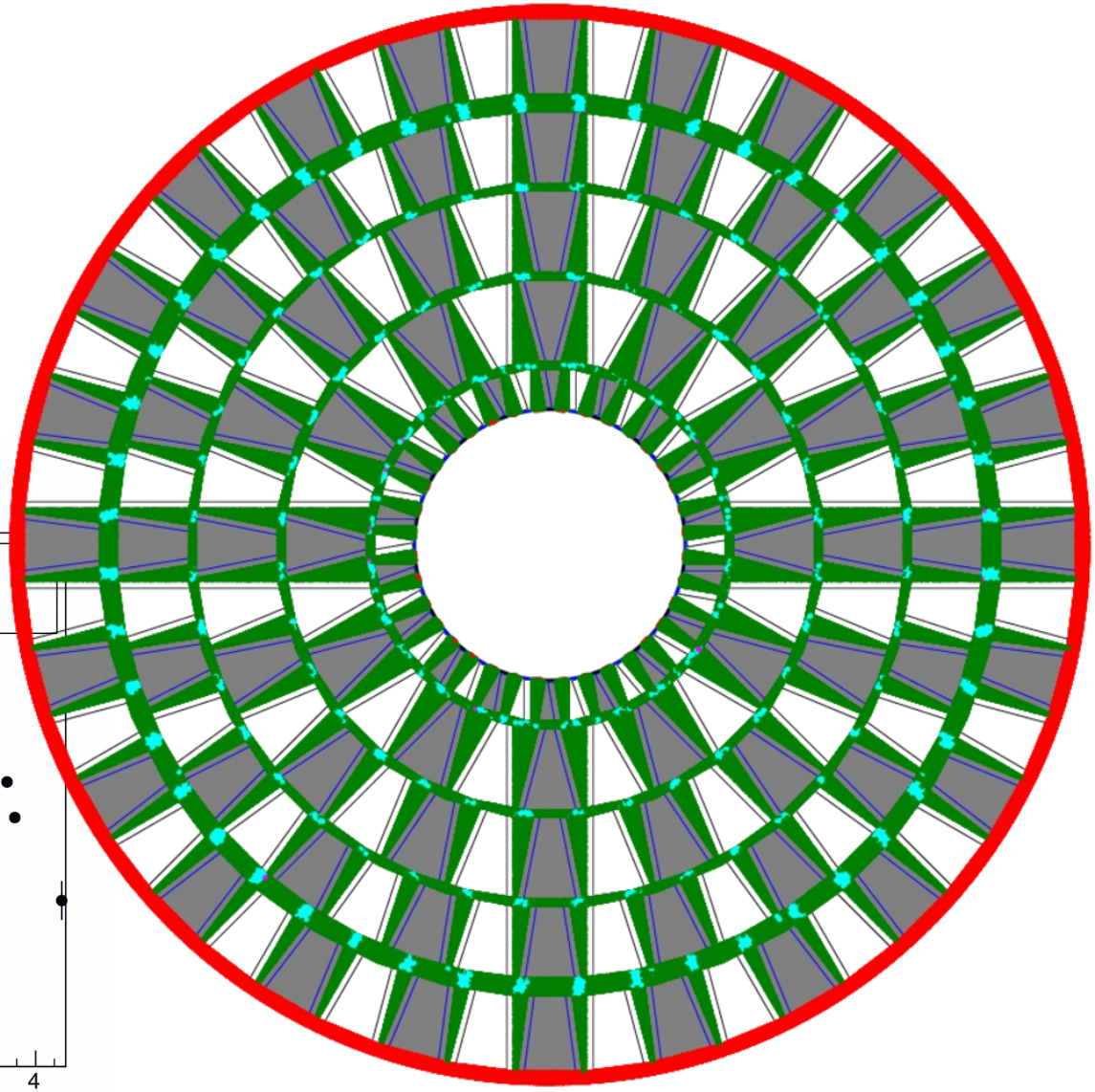
- Small regions without overlap at highest r (red)
  can be avoided by reducing the radius of ring 5
- Would also provide more overlap



Overlap with 1x1 inner ring

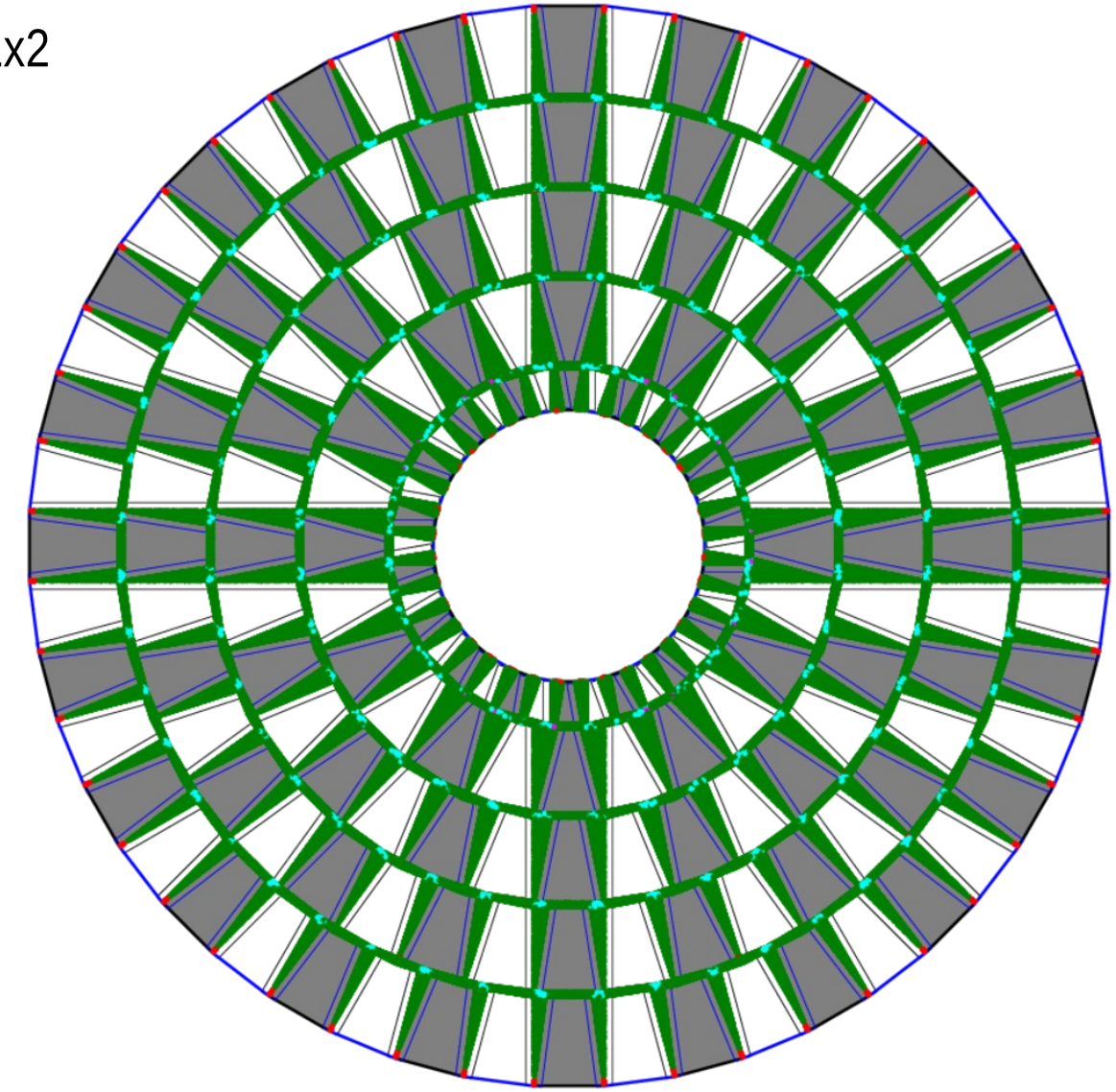
- No gaps at high r (no hits either)
- More overlap btw rings 4/5
- Small impact on tracking eta 2.6-3.0





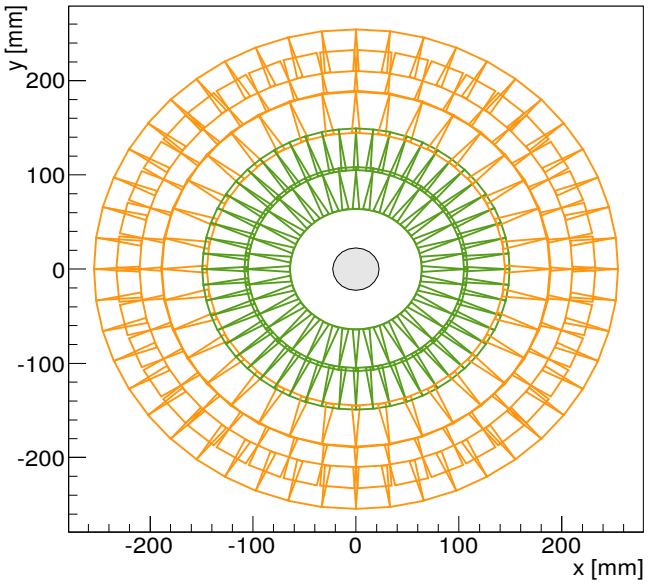
Ring 2 with 2x2 modules ?

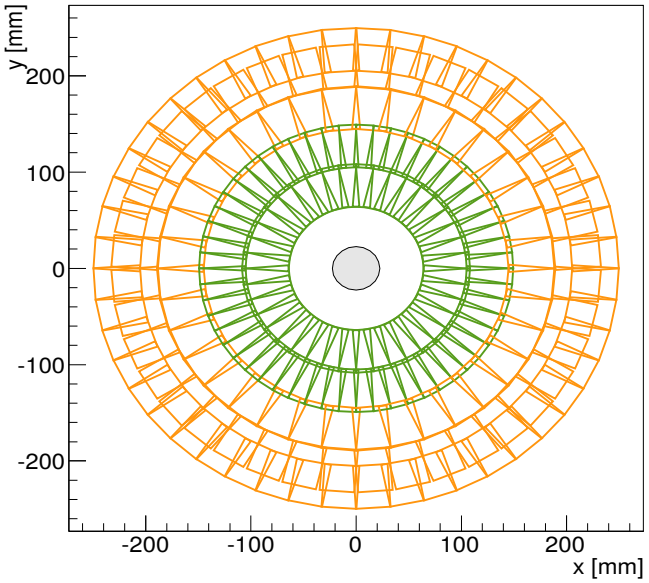
- Full coverage with 24 2x2 instead of 56 1x2
- Get rid of one module type
- Slightly less overlap (14 %)
- Any other disadvantages?

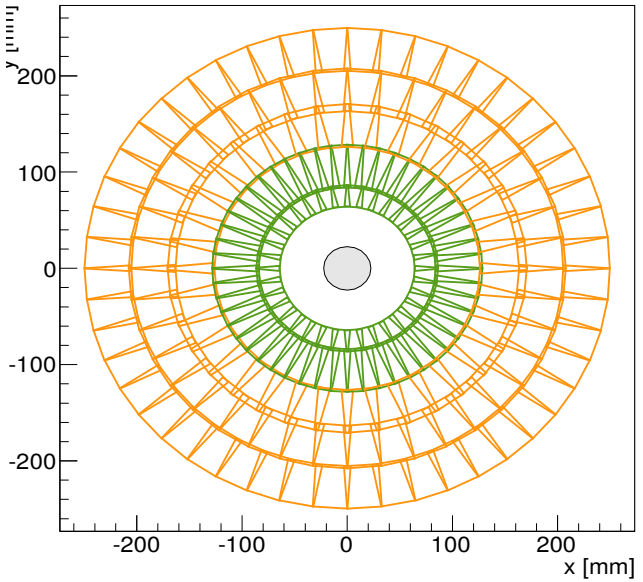


EPIX

	TDR			TDR smaller radius			R1 1x1		
	mod	#mod	r[cm]	mod	#mod	r[cm]	mod	#mod	r[cm]
Ring 1	1x2	20	6.4	1x2	20	6.4	1x1	18	6.4
Ring2	1x2	28	10.5	1x2	28	10.5	1x2	26	8.4
Ring3	2x2	18	14.4	2x2	18	14.4	2x2	18	12.6
Ring4	2x2	20	18.8	2x2	20	18.8	2x2	20	16.3
Ring5	2x2	24	21.0	2x2	24	20.5	2x2	24	20.5

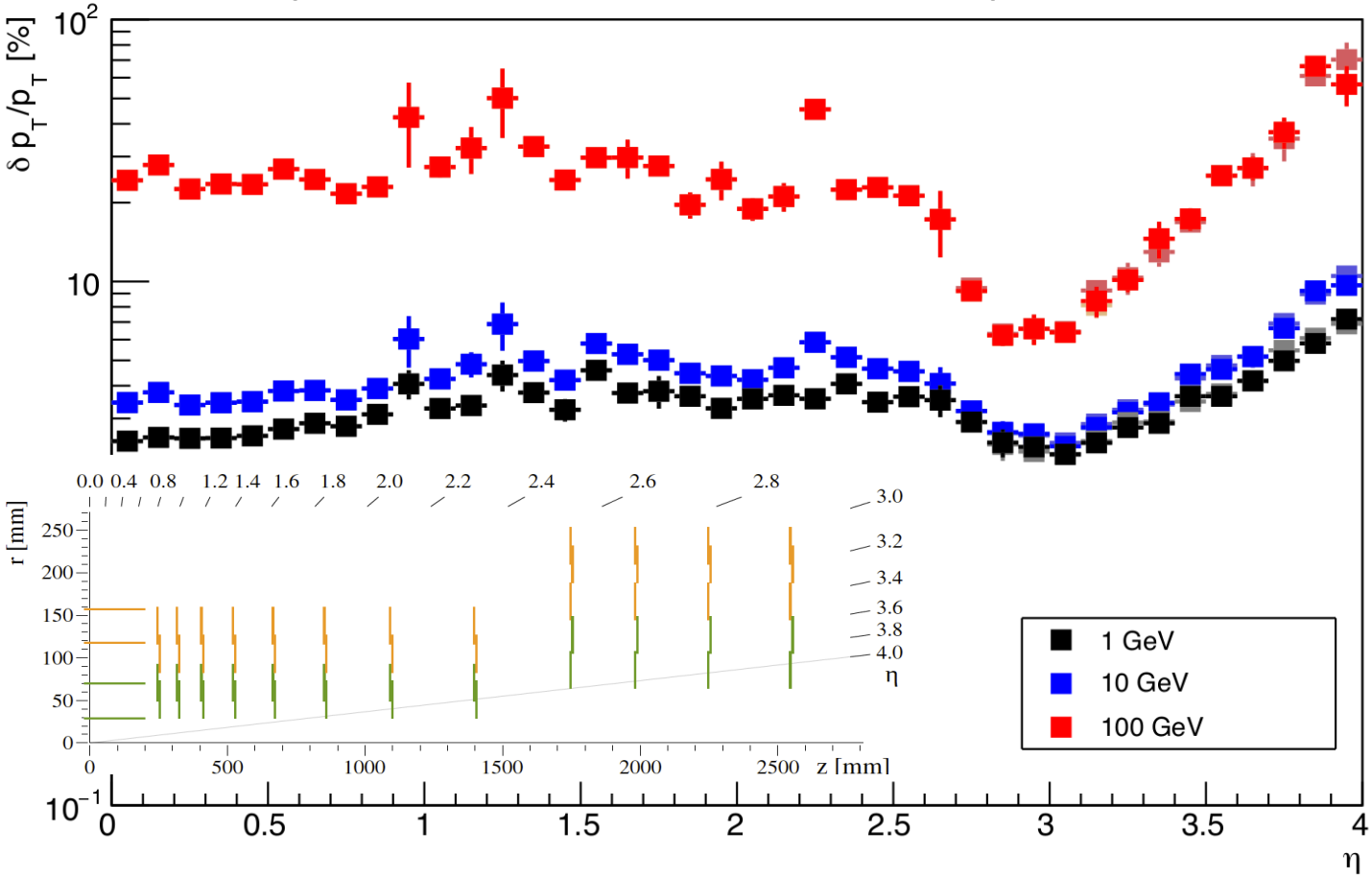


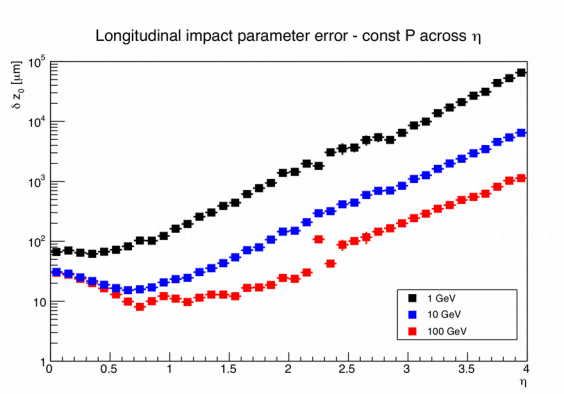


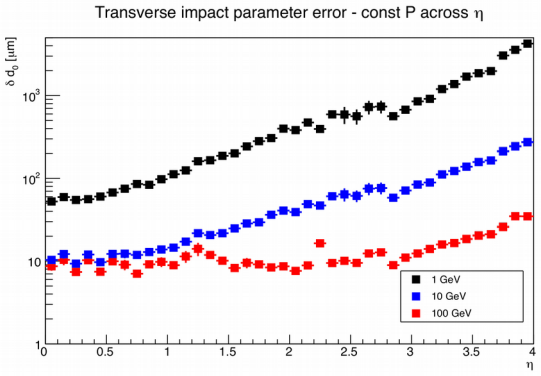


Tracking

p_T resolution versus η - const P_T across η







- No significant difference according to tklayout

Summary

- Looking at variations of the module TDR placement
  - Fewer modules
  - Fewer e-links
  - Reduced lpGBT rates
  - More room between modules on the same layer
  - Unchanged tracking performance
  - Less overlap (25 % → 17 %)
- Need some guidance on luminosity measurement requirements
  - how much overlap is needed?
  - does it matter where it is?


CMS
Compact Muon Solenoid

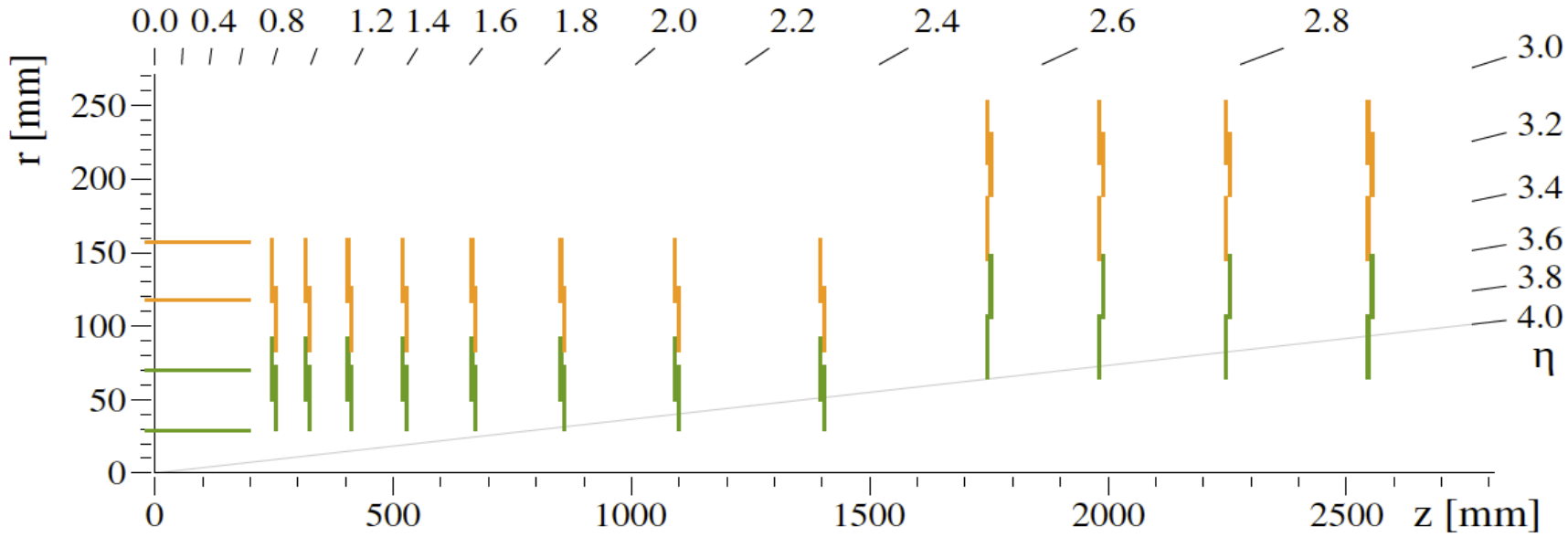


Figure 4.1: Sketch of one quarter of the pixel detector layout in the *r*-*z* view. Green lines correspond to modules made of two readout chips and orange lines represent larger modules with four chips.

elink/lpGBT connections as in TDR

Design considerations

- At most 10 modules per serial powering chain
- No forward/backward connection on same disk
- Modules connected to same lpGBT belong to same powering group