lpGBT modules (aka Port Cards)

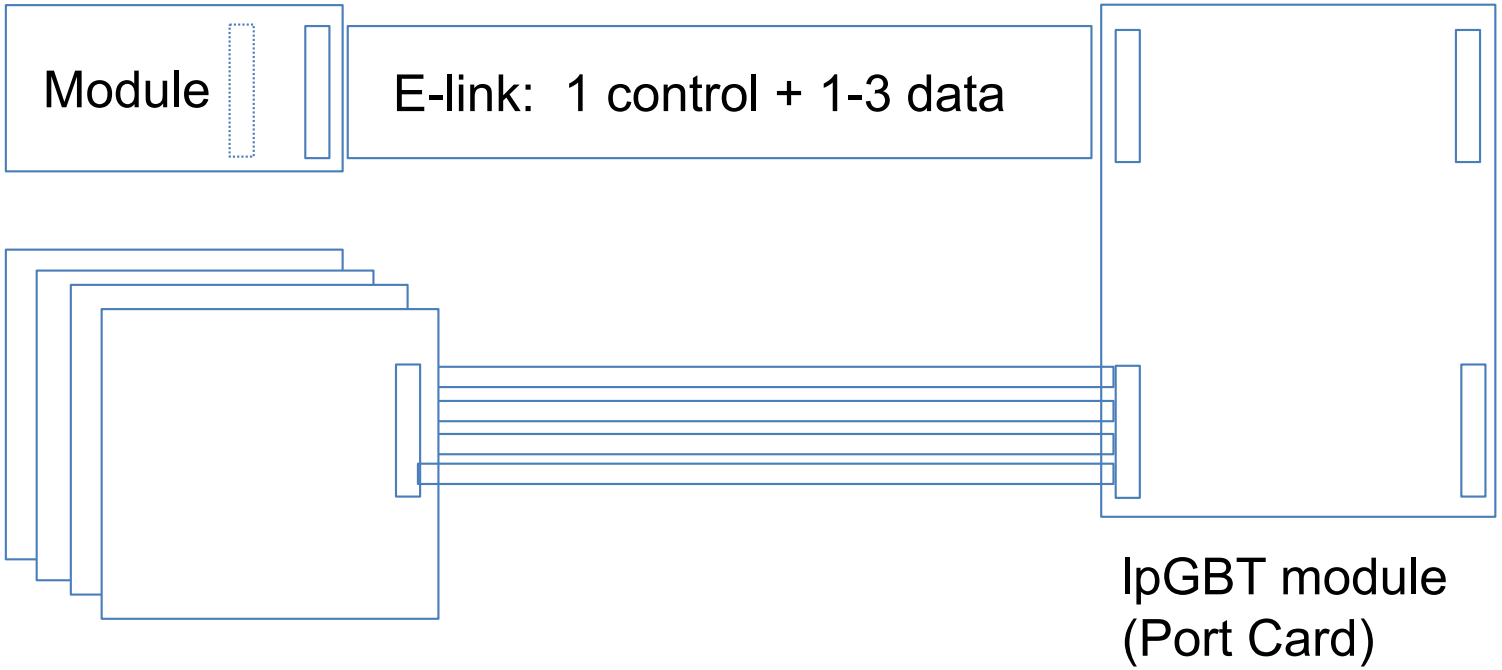
Ted Nussbaum, Karl Ecklund (Rice)

Mechanical design from Yadira's recent design models (~mid-May)
Some connected thoughts on e-link cables from port card perspective (past year)

Electrical & Optical components

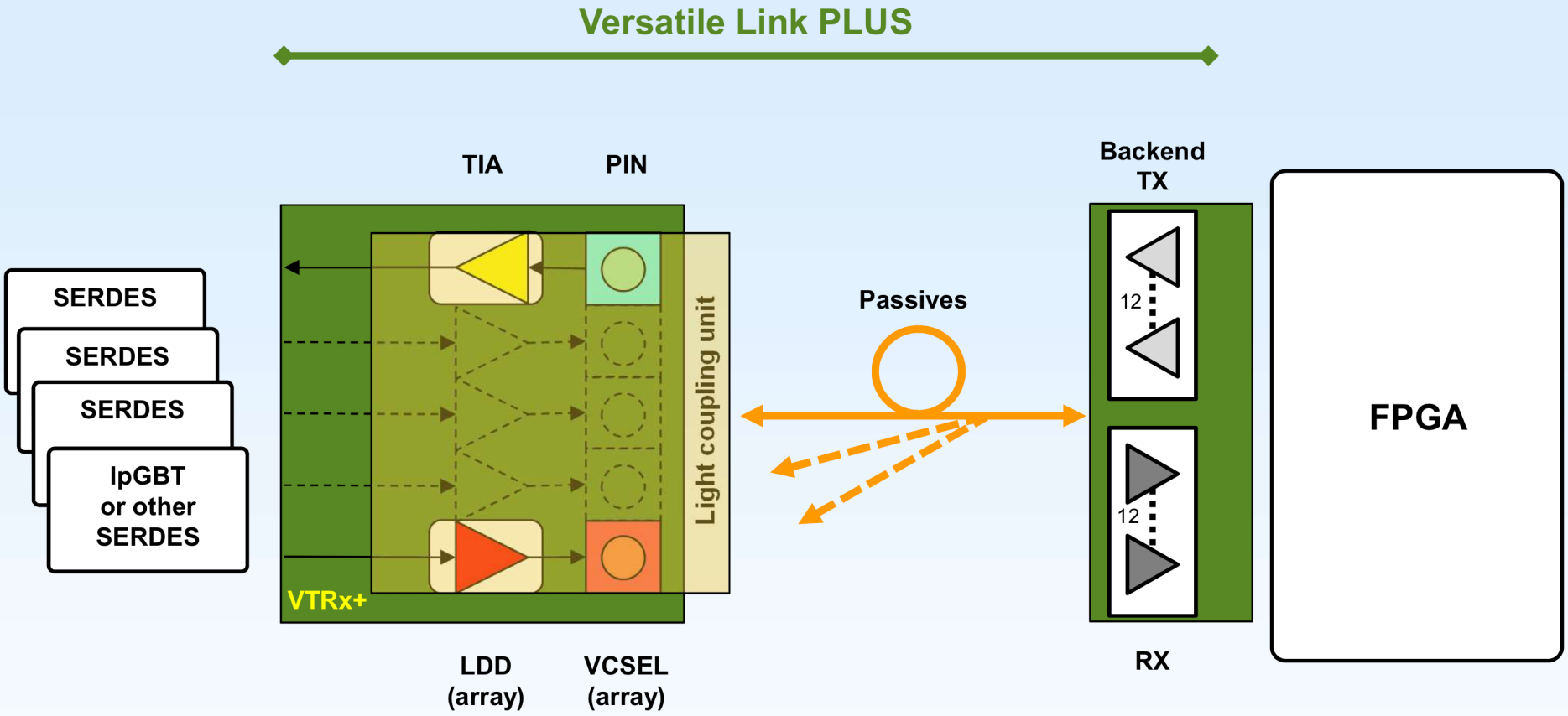
- Jointly developed for ATLAS & CMS
  - CERN, FNAL, Oxford, SMU
- Versatile Link+ System
  - Optical components for front end and back end electronics
- VTRx+ Optical Module
  - 1 Rx (2.5 Gbps) up to 4 Tx (5/10 Gbps)
  - Low profile packaging
    - Plugable Electrical connection
    - Fiber connector or pigtails
  - Radiation qualified
    - TID: 1 MGy (explore up to 2 MGy)
    - Fluence: 1E15 n /cm^2
- lpGBT - Low power GigaBit Transceiver
  - ASIC for electrical / optical
  - 5.12/10.24 Gbps data links & 2.56 Gbps control link
  - E-port concept: 7 * 1.28 Gbps uplinks; 8 * 160 Mbps downlinks
    - Other configurations possible (e.g. lower speeds, more links)

On-detector electronics concepts



- E-links might be flex cables (baseline) or possibly twisted pairs
- lpGBT module (Port Card) has **two** lpGBT & VTRx+ as baseline (other variants might be considered) and is DC-DC powered
- lpGBT modules are mounted on a frame at outer radius of service cylinder
  - TFPX (& maybe TEPX) can be integral component of Dee + portcard frame = cartridge
  - TBPX has similar port card frames mounted between downstream disks
    - Requires longer e-links from ladder to port card locations

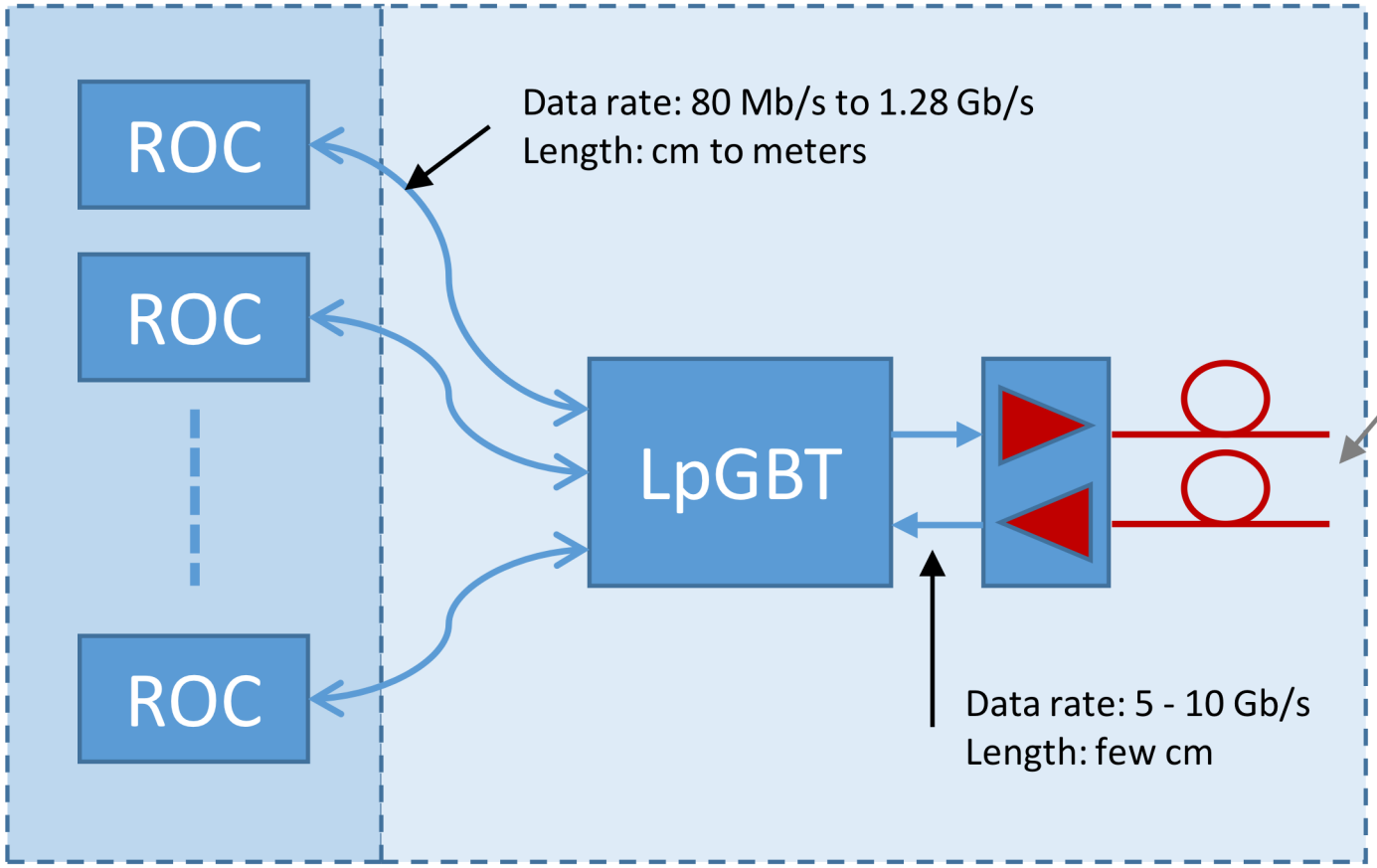
Versatile Link



On-Detector
Custom Electronics & Packaging
Radiation Hard
Up to 4Tx plus 1Rx

Off-Detector
Commercial Off-The-Shelf (COTS)
on-board 12Tx, 12Rx module

LpGBT

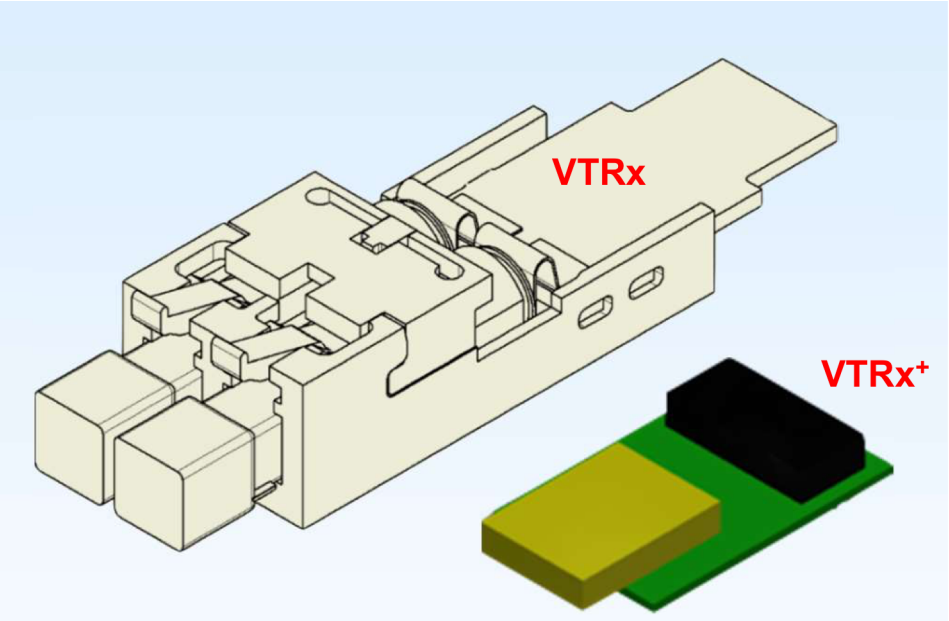


LpGBT Packaging
BGA 17*17
0.5mm pitch
9mm*9mm*1.5mm

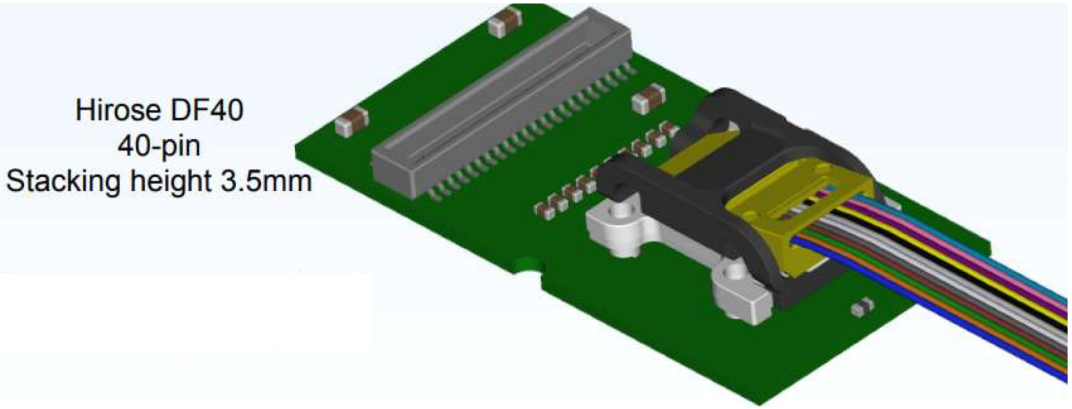
- Downlink 2.5 Gbps & Uplink 10 Gbps
  - E-ports : multiplexed Tx channels 7 @ 1.28 Gbps; 8 @ 160 Mbps (+ other speeds)
  - Phases all adjustable (no Delay25 equivalent needed)
- Link protocol includes Forward Error Correction (FEC5, FEC12)
- Radiation tolerant 200 MRad
- For data links electrical receiver has optional 100 ohm termination built in

VTRx+ Optical Module

- Evolution of VTRx based on SFP duplex fiber TRx package
  - Developed for phase 1 upgrades
- VTRx+ has a smaller form factor
  - (Also higher speed)
  - Note use of 12 fiber ribbon connection, either low profile connector or pigtail
  - Compact, lower mass

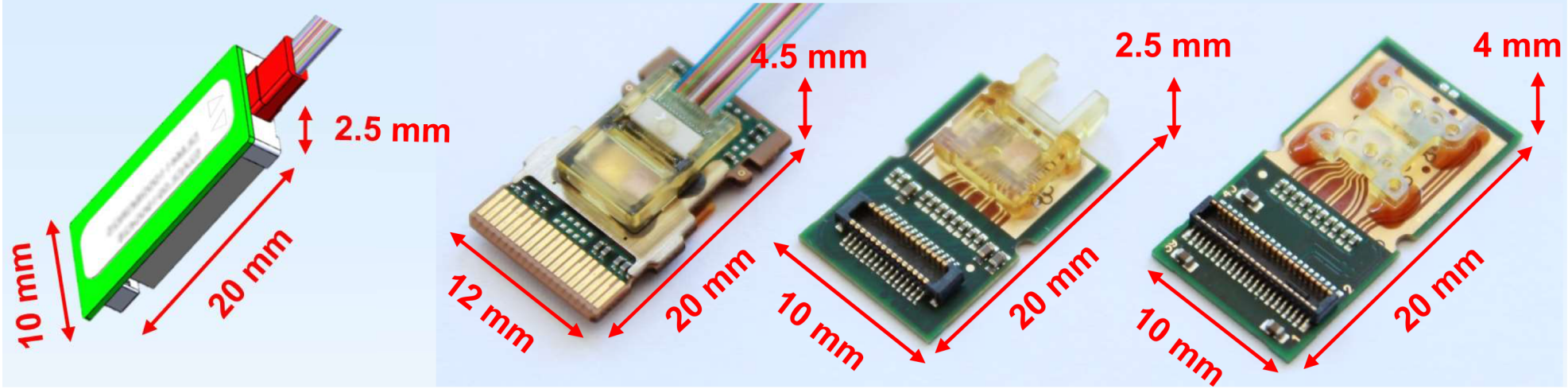


Total quantity ~50k modules



VTRx @ ACES 2018

2.5 VTRx+ prototypes

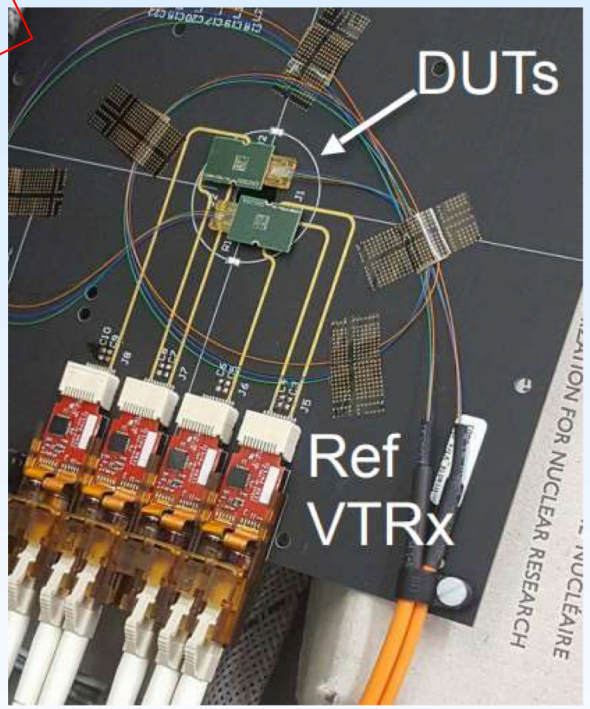


- Prototypes developed & tested
- Expect to be available for user evaluation & development end of 2018
  - lpGBT on a similar timescale

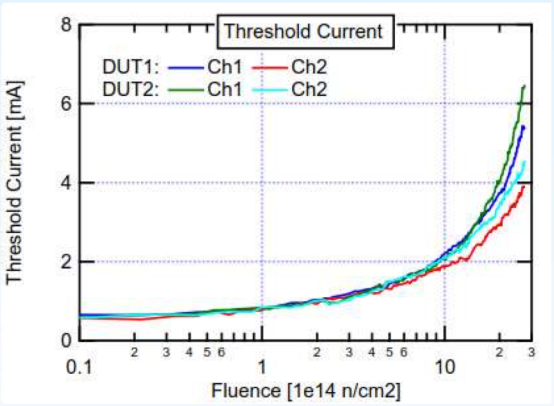
2.6 The VTRx+ performance challenge

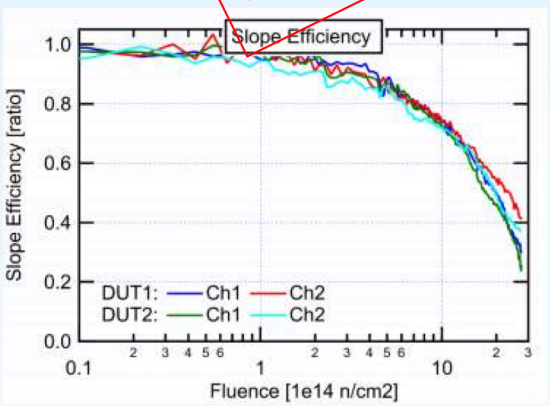
- Maintaining performance over Temperature and Lifetime (i.e. radiation) is challenging
  - requires in-depth understanding of the electronics-optics interplay
  - Optimization on-going to gain margin
  - full module results shown below

2018 irradiation of VTRx+ module V4
At -15degC, no annealing

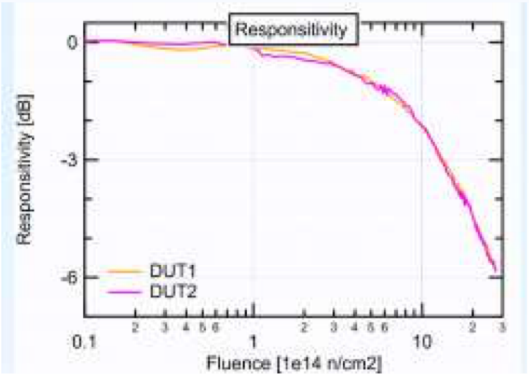


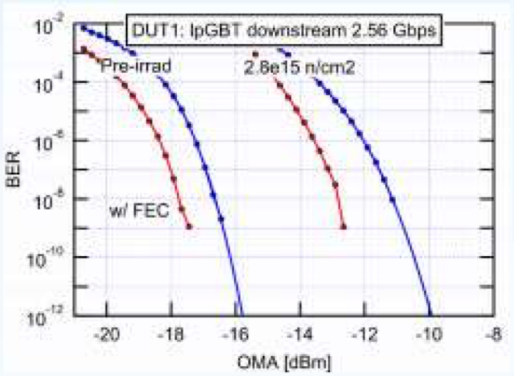
- Tx (-15degC)

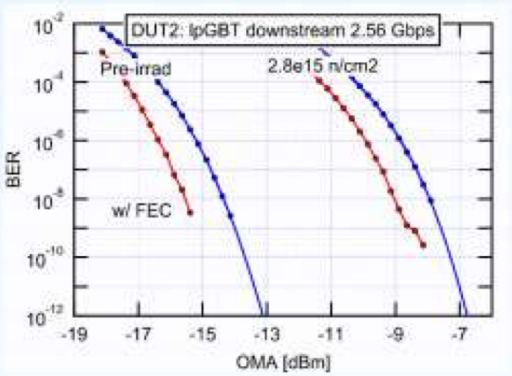




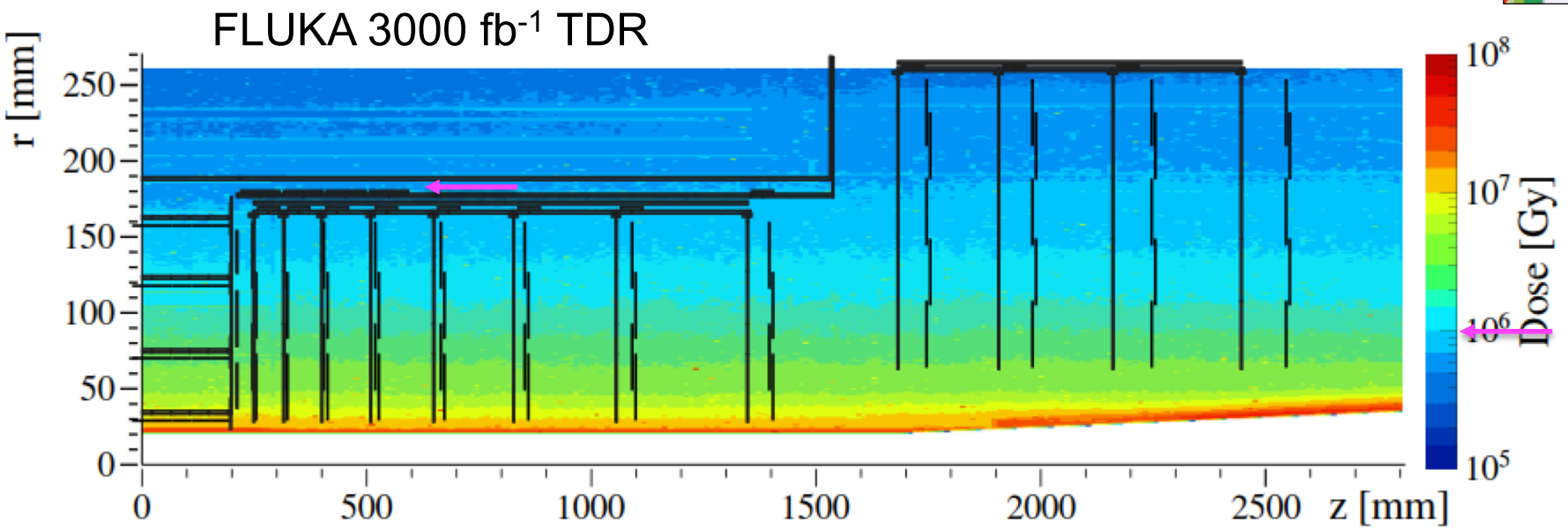
- Rx (-15degC, GaAs PIN)







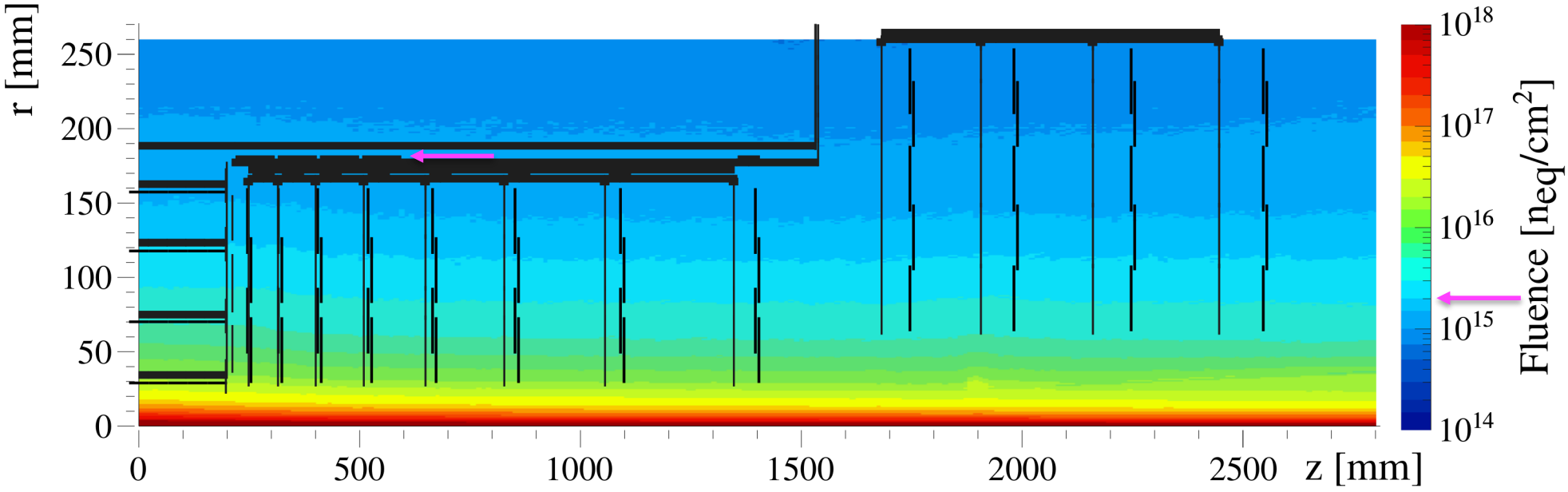
Radiation Tolerance



- Up to 1E15 n/cm^2 fluence and 1 MGy (100 MRad)
  - The laser transmitters VCSELs are sensitive
- Drove thinking about placing opto-hybrids at outer radius of TFPX disks in TDR and subsequent design work; highest radius available
  - Note TBPX links can be put in the same location
  - Dose expected at 16 cm : ~1 MGy
  - Fluence at 16 cm : ~2E15
  - VTRx optical modules need to be replaceable during YETS
  - Does will be lower for TEPX – safely(?) below 1 MGy

Fluence Prediction

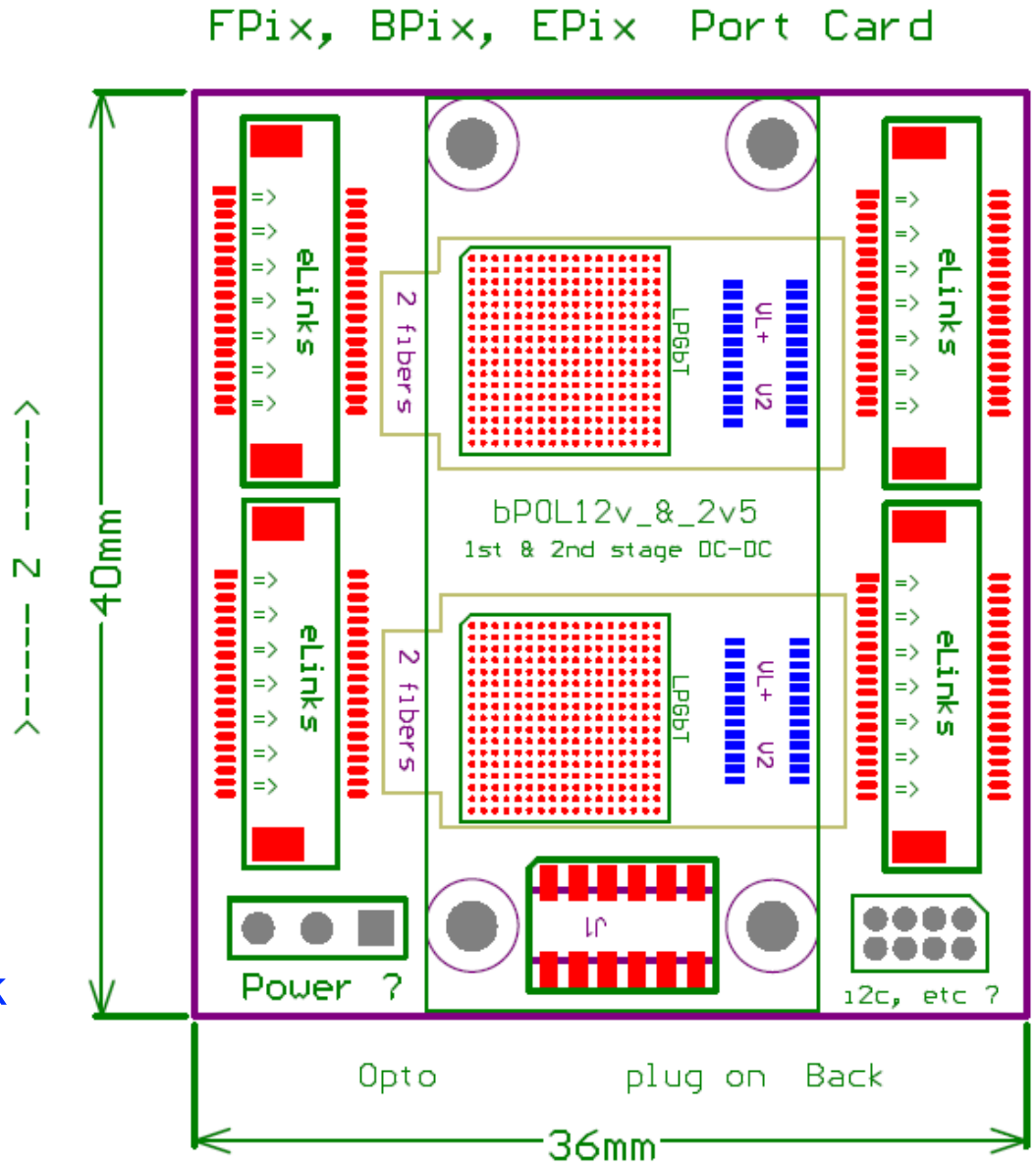
FLUKA 3000 fb^{-1} TDR

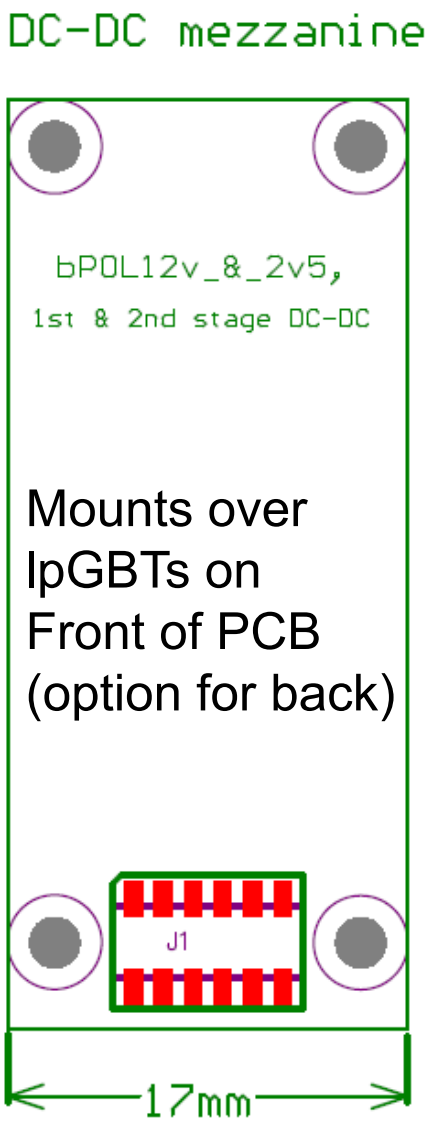


lpGBT port card & E-link cables

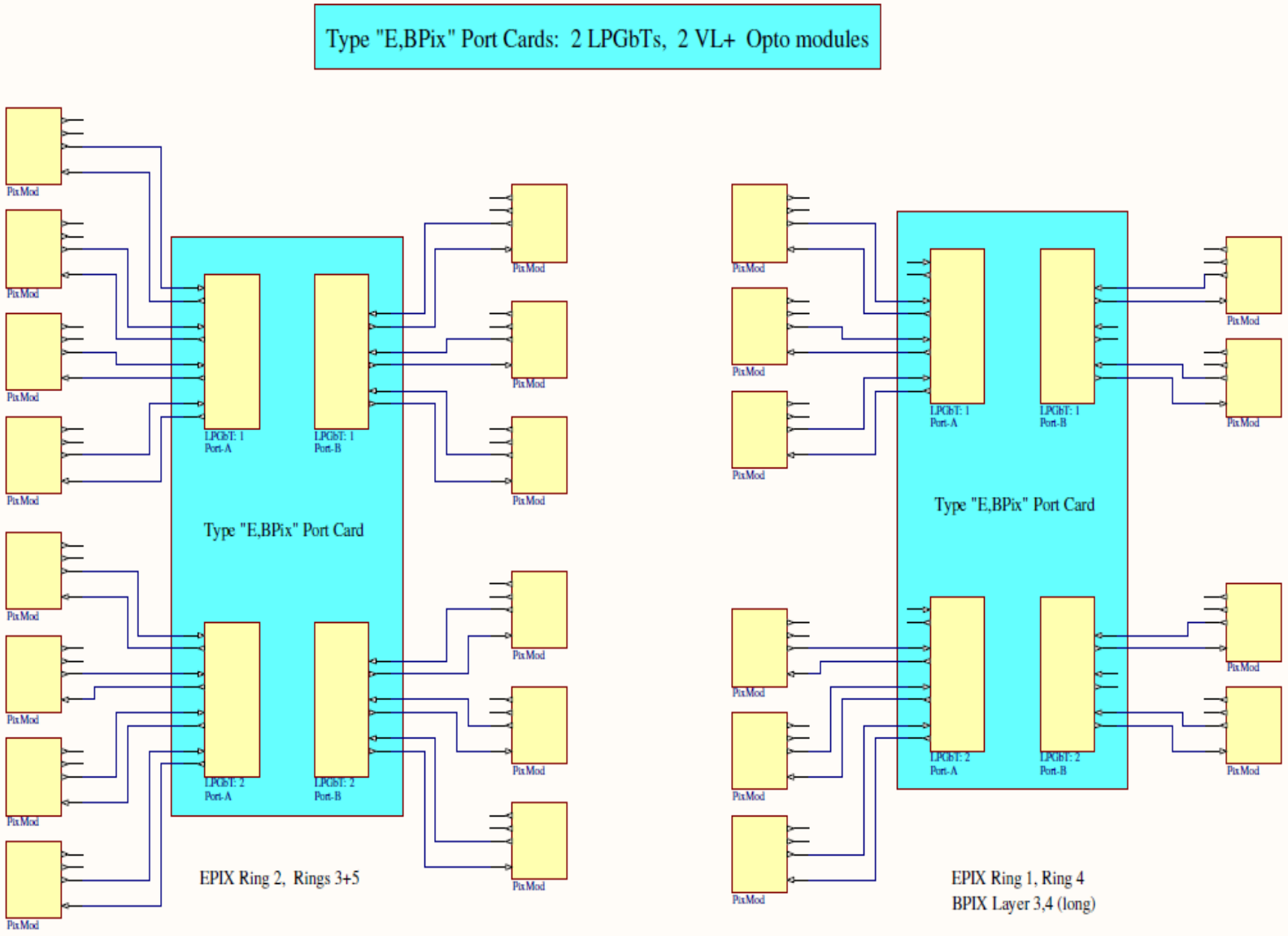
- For each lpGBT ASIC / VL+ optical link we aim to use
  - Up to 7*1.28 Gbps electrical data links from modules
  - Up to 7 electrical control/command links
- Each Module uses 1 down link and 1–6 data links
  - Data link counting relies on data “compression” in ROC
    - Compression can be clustering & local address scheme (studies ongoing)
    - In TDR studies a factor ~2 would be needed over RD53A protocol
- Mount lpGBT PCBs in half ring frames inside service cylinder
  - Two lpGBT ASICs VL+ optoTRx per lpGBT module / port card
- E-link cables between modules and lpGBT module can have up to 6 uplinks and as many as 4 down links (serving <=4 modules)
  - L1 1x2 module has 6 up links and one control link
  - TEPX modules have 1 up link/1 control link – up to 7 per lpGBT
- Looks possible to use same module connector and e-link pin definition for all modules / lpGBT modules
  - Up to 6 data links and 4 control links on a e-link cable ; unused pairs at lpGBT module can be left unconnected

lpGBT Module / Port Card





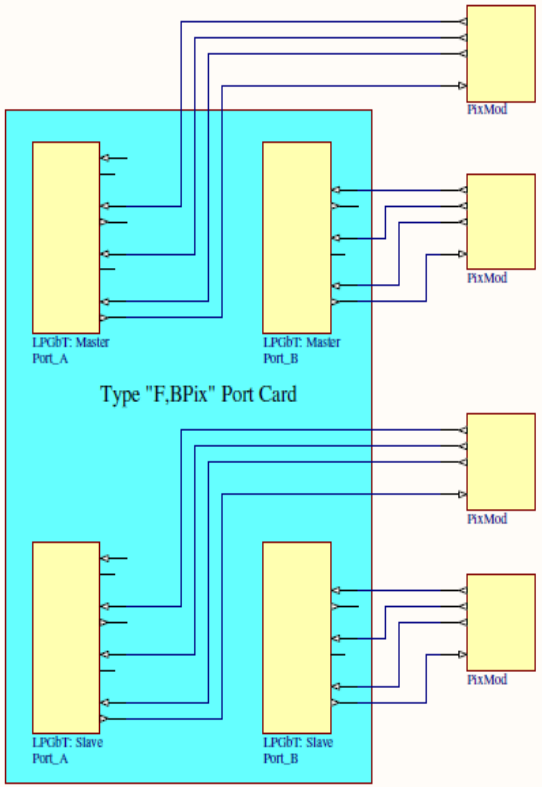
Red = front
Blue = back


Type "E,BPix" Port Cards: 2 LPGbTs, 2 VL+ Opto modules
PixMod
LPGbT: 1
Port-A
LPGbT: 1
Port-B
Type "E,BPix" Port Card
LPGbT: 2
Port-A
LPGbT: 2
Port-B
EPIX Ring 2, Rings 3+5
EPIX Ring 1, Ring 4
BPIX Layer 3,4 (long)
Title
Type "E,BPix" port card -> Pix Modules
Size
B
Number
Revision
Date:
2/28/2018
Sheet of
File:
C:\Users\...\E,Bpix_PortCard+Modules.Sch
Drawn By:

F,BPix, "M-S" Port Cards : 2 LPGbTs, 1 VL+ module & CMD fiber

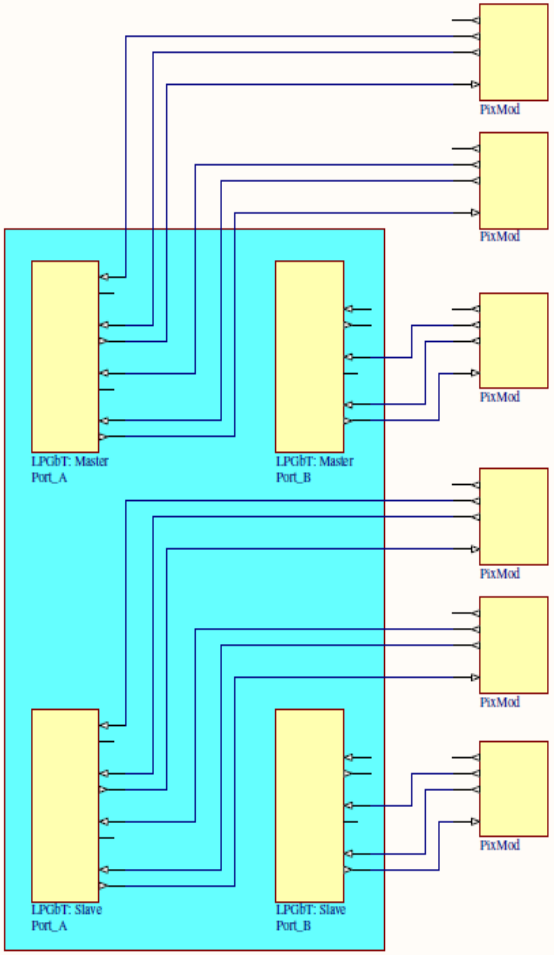
Master / Slave LPGbTs => Max. 4 Pix modules / LPGbT

Eiminates 320 FPix, 222 BPix VL+ modules & fibers



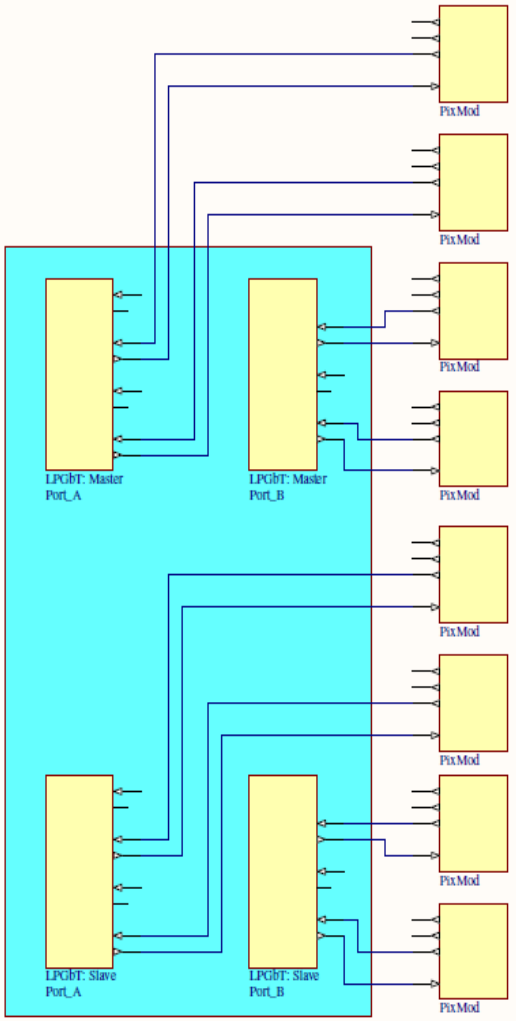
FPIX Ring 1

BPIX Layer 1 (use both A & B / Pix module) ?



FPIX Ring 2,3

BPIX Layer 2

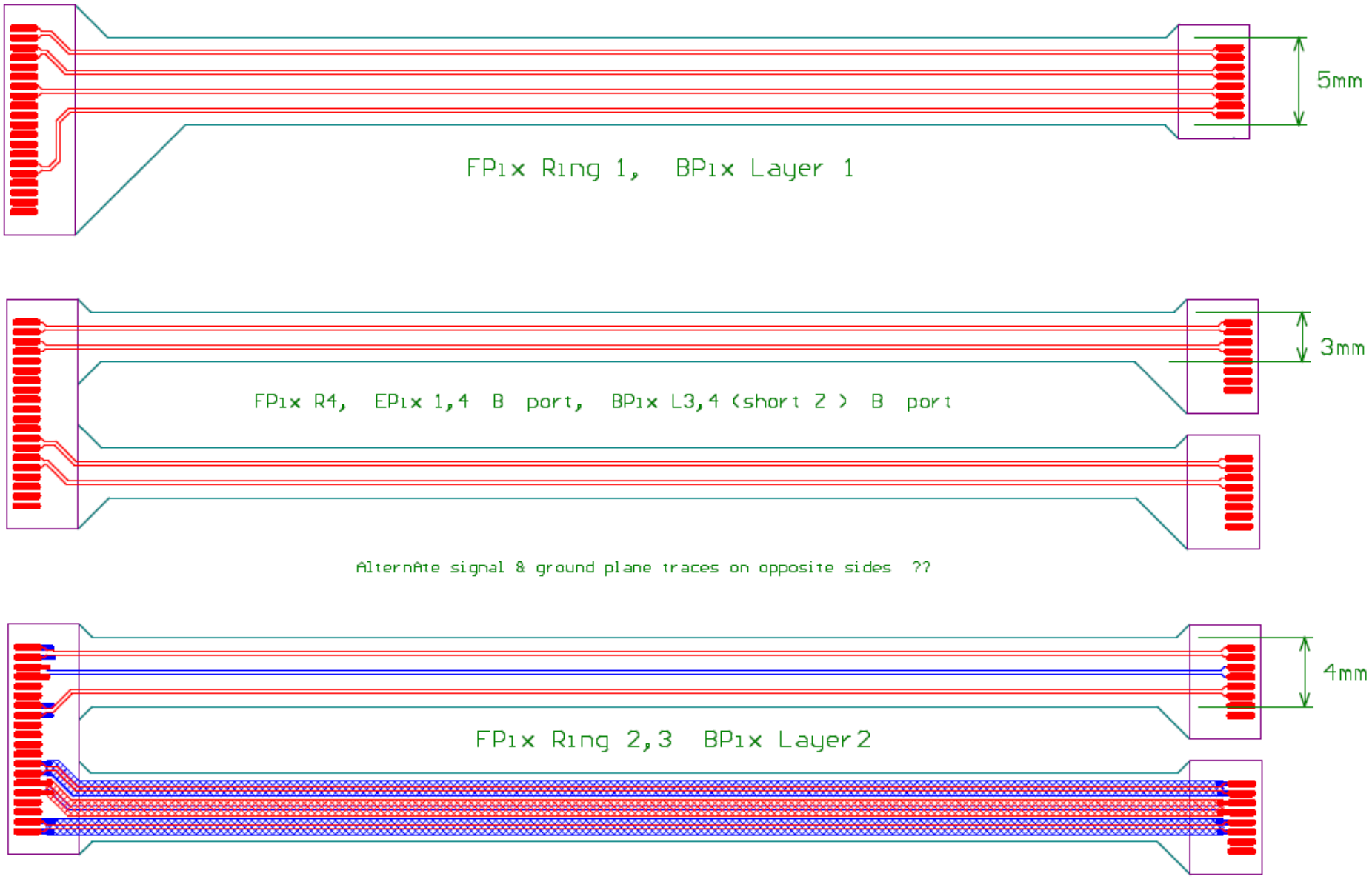


FPIX Ring 4

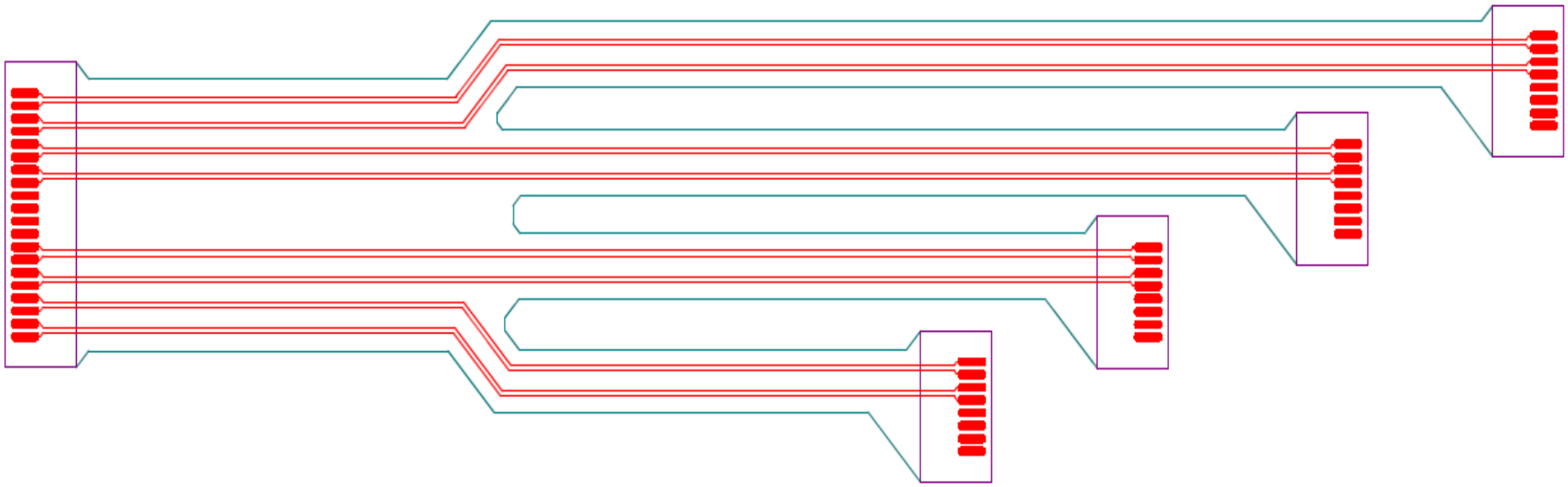
BPIX Layer 3,4 (short)

Title: Type "M-S" F,BPix Port Cards <--> Pixel modules		
Size: B	Number	Revision
Date: 2/27/2018		Sheet of
File: C:\Users\..\F,Bpix_PortCard+Modules.Sch		Drawn By:

F,E,BPix FPCs


5mm
FPix Ring 1, BPix Layer 1
3mm
FPix R4, EPix 1,4 B port, BPix L3,4 (short Z) B port
Alternate signal & ground plane traces on opposite sides ??
4mm
FPix Ring 2,3 BPix Layer2

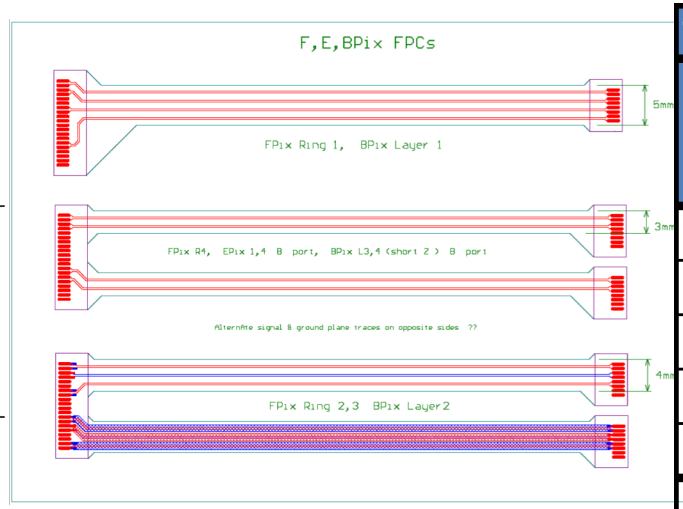
EPix & BPix: 3 & 4 Pix modules, 1 Data each

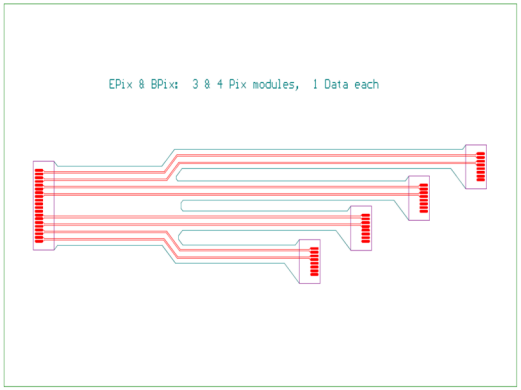


TFPX FPC Design Flavors

6x2 lengths = 12

- F1_2, F1_3, F1_4 (2, 3, 4 pairs)
- F2_2, F2_3: 2, 3 pairs
- F4_2: 2 pairs



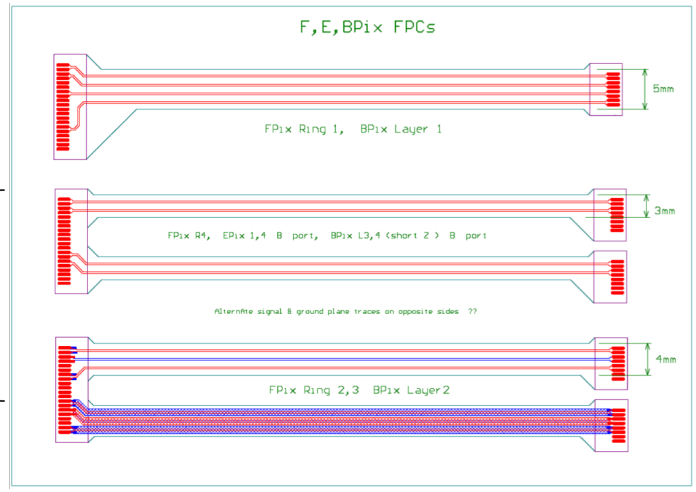


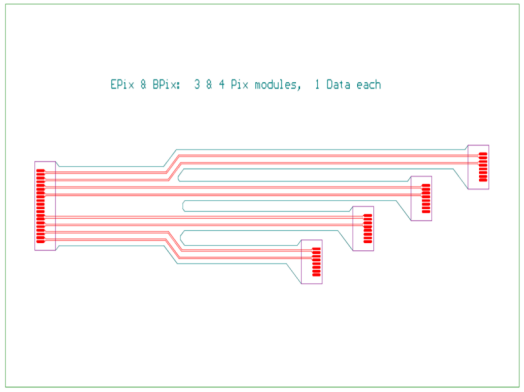
TFPX					
Portcard	Uplinks				
	Ring	#mod	links/mod	tot link	Flav.
	R1	2	3	6	F1_4
	R1	2	3	6	F1_4
	R1	1	3	3	F1_4
	R3	3	2	6	F2_3, F1_3
	R3	3	2	6	F2_3, F1_3
	R1	2	3	6	
	R1	2	3	6	
	R1	1	3	3	
	R3	3	2	6	
	R3	3	2	6	
	R2	3	2	6	F2_3, F1_3
	R2	3	2	6	F2_3, F1_3
	R2	2	2	4	F2_3
	R4	4	1	4	F2_2
	R4	4	1	4	F2_2
	R2	3	2	6	
	R2	3	2	6	
	R2	2	2	4	
	R4	4	1	4	
	R4	4	1	4	

- Reminder:
  - Each port card has max of four connectors
  - Each module requires one downlink

TEPX FPC Design Flavors

- F1_2, F1_3, F1_4 (2, 3, 4 pairs)
- F2_2, F2_3: 2, 3 pairs
- F4_2: 2 pairs



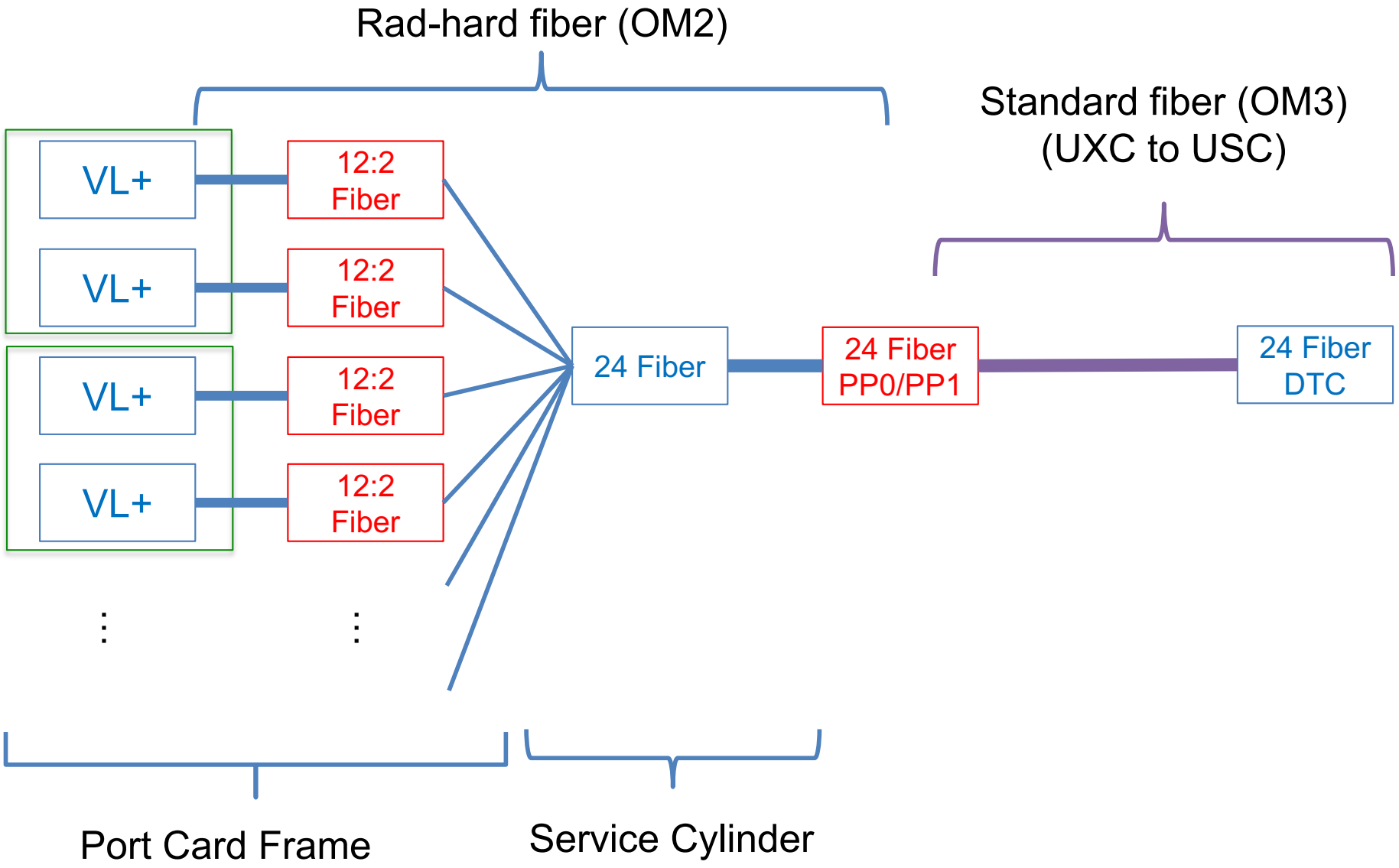


TEPX					
Portcard	Uplinks				
	Ring	#mod	links/ mod	tot link	Flav.
	R1	5	1	5	F4_2, F1_2
	R1	5	1	5	F4_2, F1_2
	R3+R5	7	1	7	F4_2, F2_2, F1_2
	R3+R5	7	1	7	F4_2, F2_2, F1_2
	R3+R5	7	1	7	F4_2, F2_2, F1_2
	R1	5	1	5	
	R1	5	1	5	
	R3+R5	7	1	7	
	R3+R5	7	1	7	
	R3+R5	7	1	7	
	R2	7	1	7	F4_2, F2_2, F1_2
	R2	7	1	7	
	R4	5	1	5	F4_2, F1_2
	R4	5	1	5	
	R2	7	1	7	
	R2	7	1	7	
	R4	5	1	5	
	R4	5	1	5	

Links per sub-detector

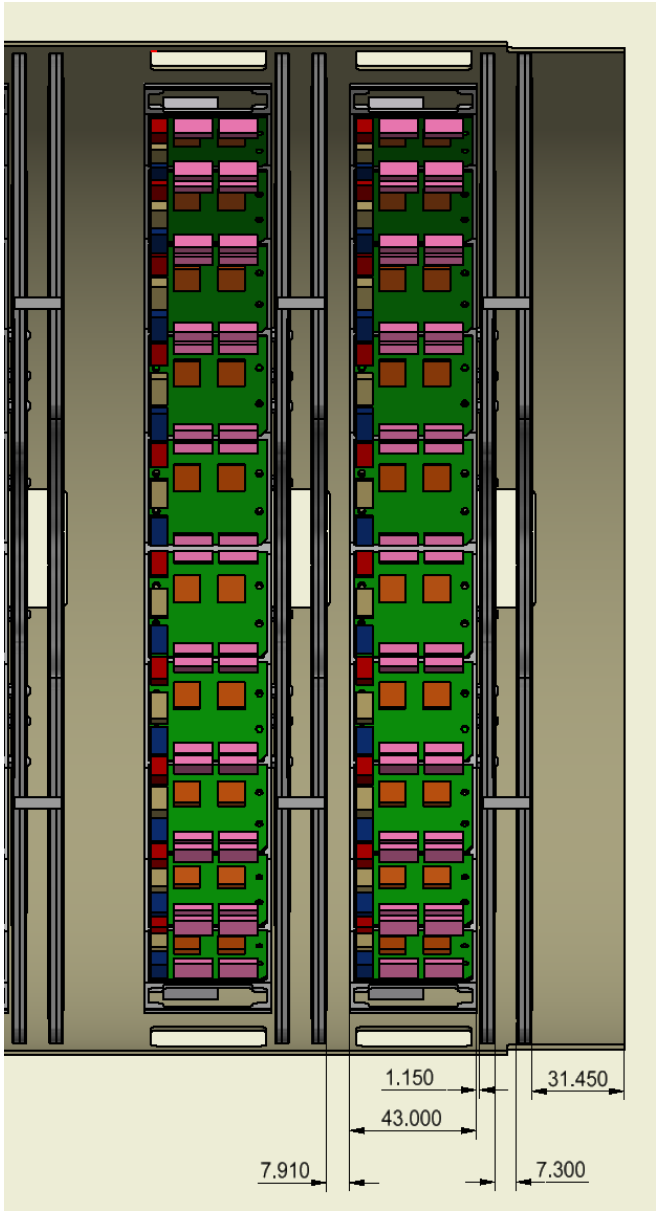
QUARTER OF IT		Multiplicity (#ladders, #disks)	#modules per ladder/ half ring	#Links per module	Total #Links (short)	Total #Links (long)
TBPX	L1	6	4 (short)/ 5 (long)	6	144	180
	L2	14	4 (short)/ 5 (long)	2	112	140
	L3	12	4 (short)/ 5 (long)	1	48	60
	L4	16	4 (short)/ 5 (long)	1	64	80
	SUM				**368**	**460**
					Total #Links for N*half disks	
TFPX	R1	8	10	3	240	
	R2	8	16	2	256	
	R3	8	12	2	192	
	R4	8	16	1	128	
	SUM				**816**	
TEPX	R1	4	20	1	80	
	R2	4	28	1	112	
	R3	4	18	1	72	
	R4	4	20	1	80	
	R5	4	24	1	96	
	SUM				**440**	
				Quarter of TBPX+TFPX	**1184**	**1276**
				Quarter of TEPX	**440**	
				Quarter of IT	**1624**	**1716**
				One end of IT	**3248**	**3432**
				Entire IT	**6680**	

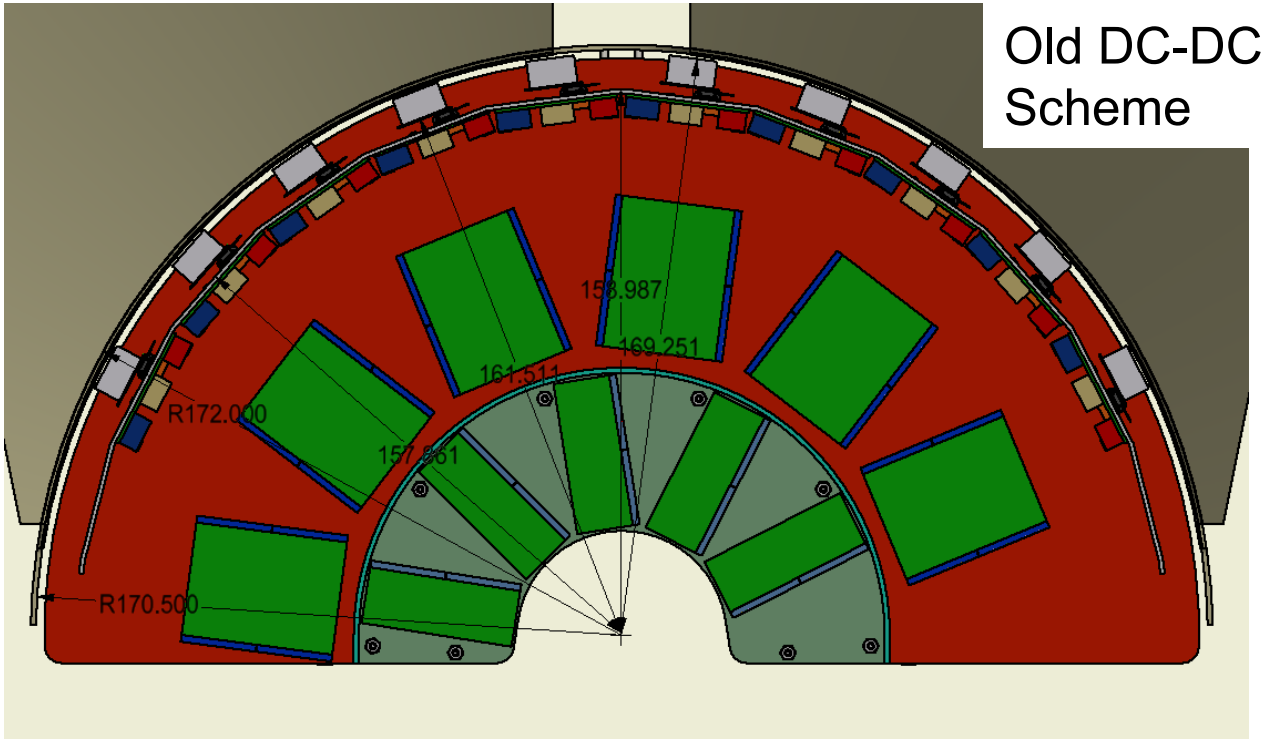
Optical Chain



Discussions underway with Jan Troska et al.

TFPX Disks





Old DC-DC Scheme

- Dimensions of port card set by
  - circumference and number required
  - Space available between disks (Z)
  - Size of VL+, lpGBT, DC-DC inductors
- Initial design 36 mm x 40 mm
  - Puts DC-DC on mezzanine card
  - Revisit when layout of card starts

IT Mechanics Design

TFPX half disks and port cards mounted together

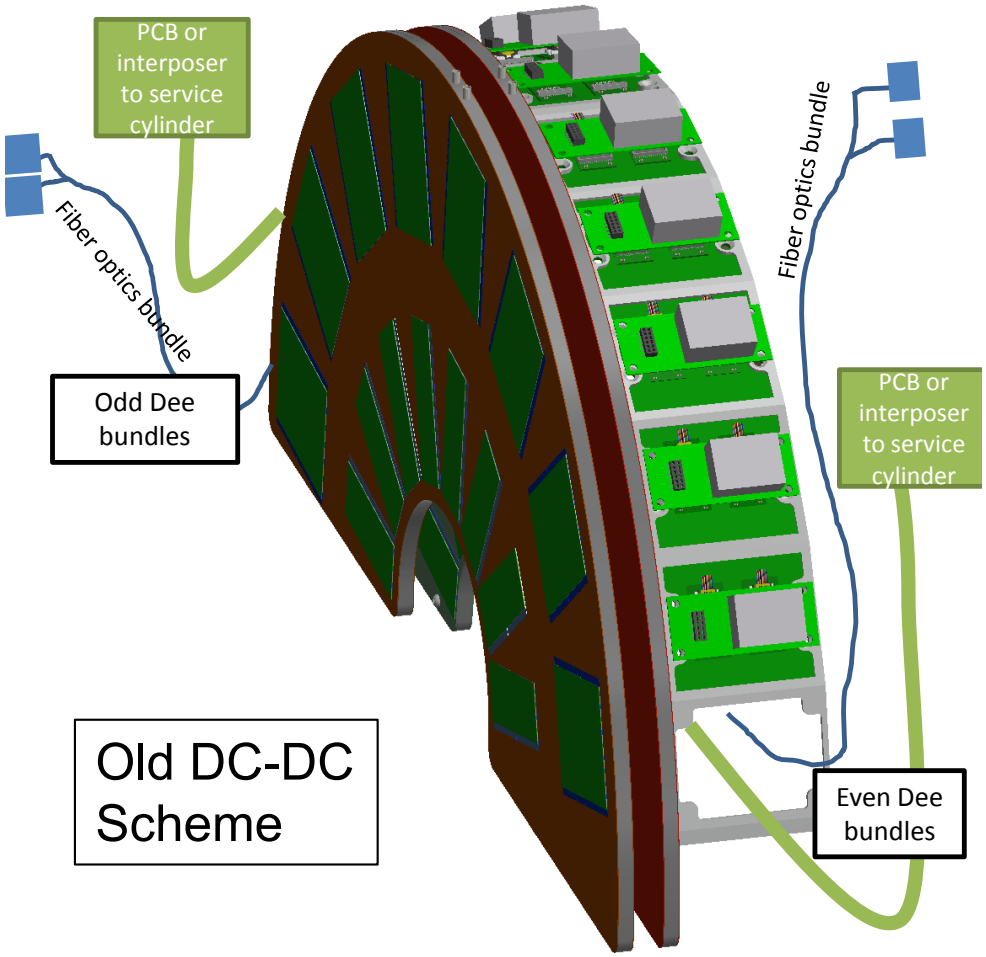
Power, cooling, fibers connect in two locations

Modular design

- Speeds assembly (& repairs)
- Factorizes testing

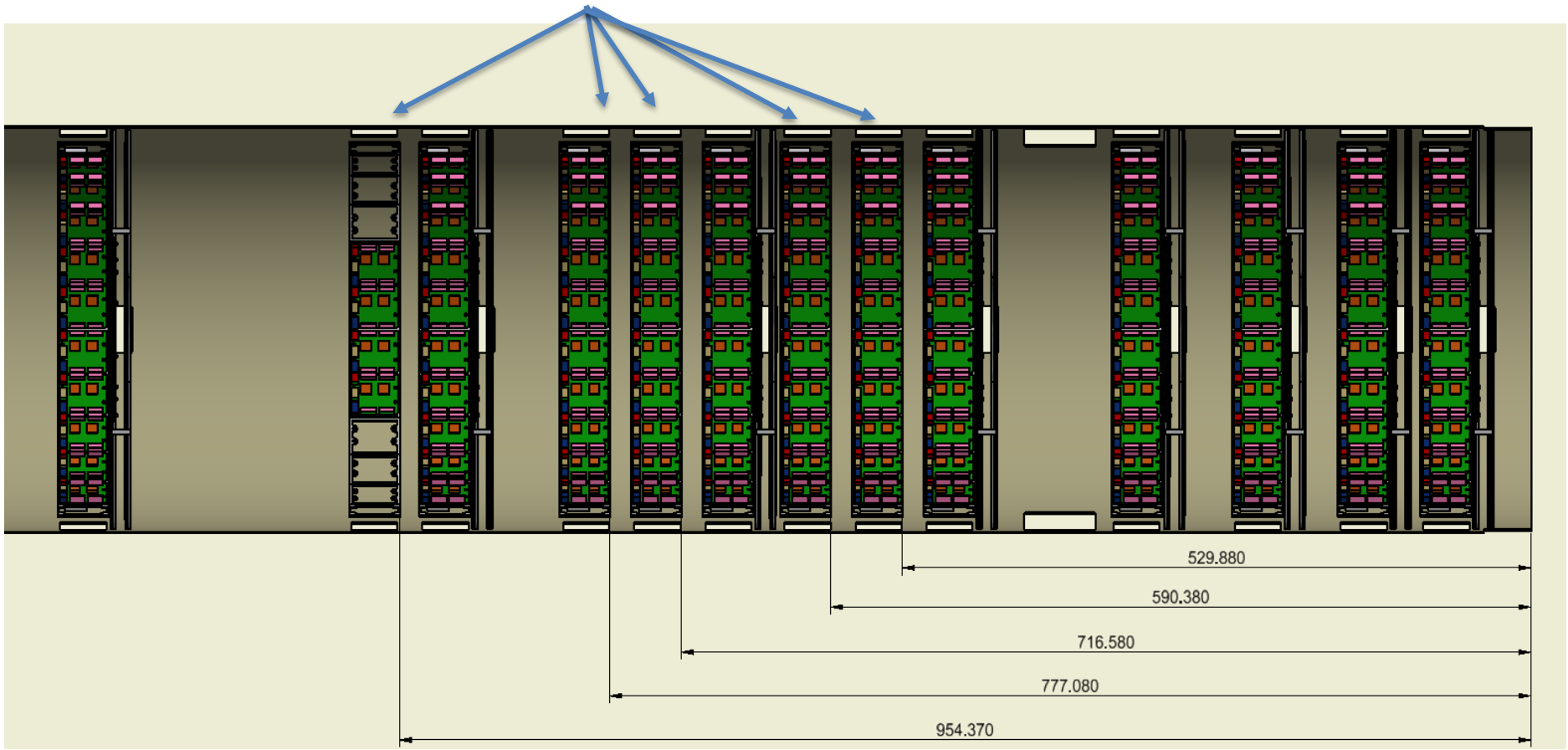
https://indico.cern.ch/event/709649/

Cartridge system



TFPX & TBPX (working) Concept

BPIX Port Cards can fit between disks in some locations

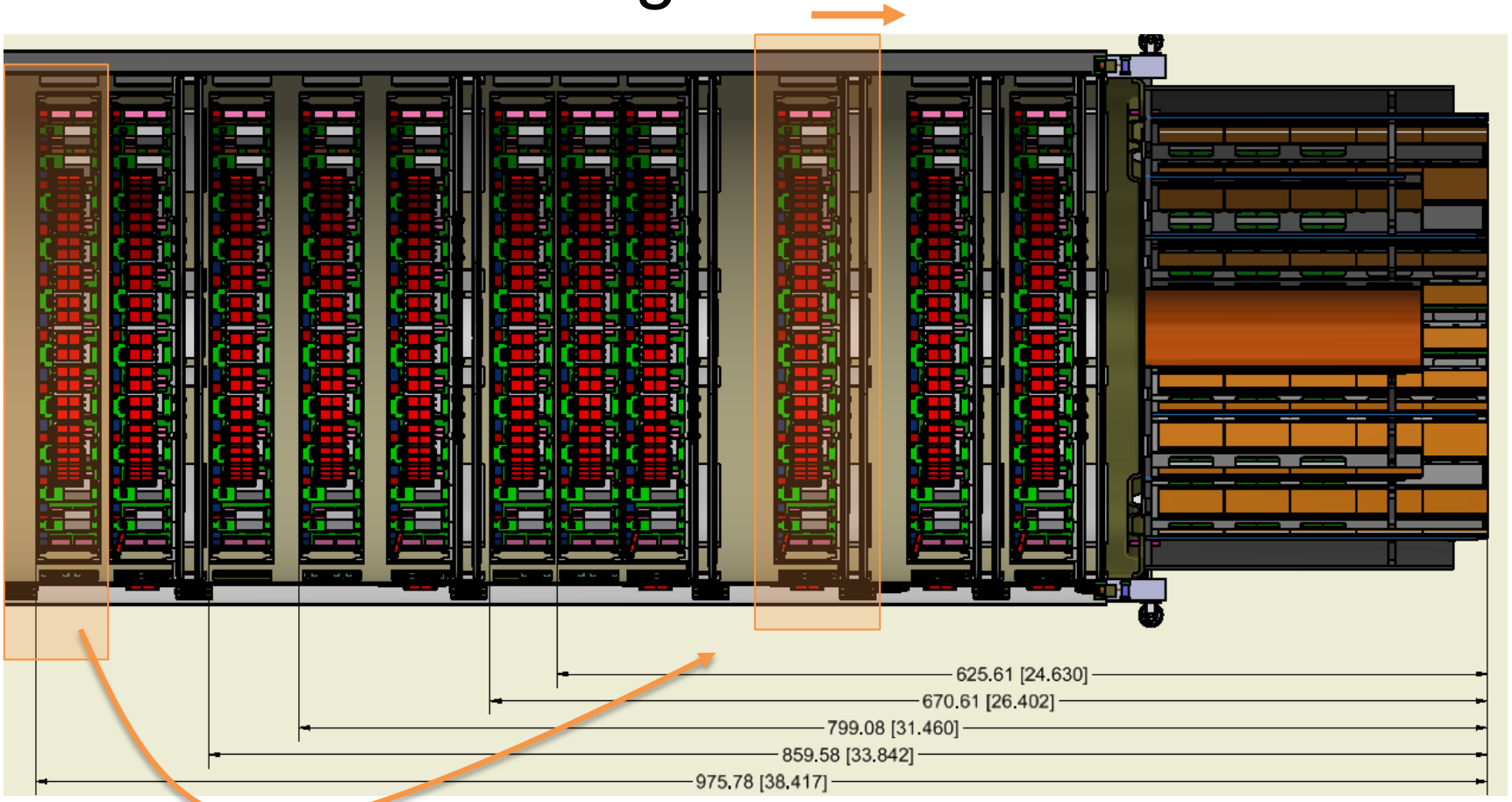


There is enough room for Port Card Frames within 1 m of from of service cylinder
Cables from barrel (right) would terminate on connector board on outer cylinder that routes to BPIX port cards (extra connection, but simple connection to frame)

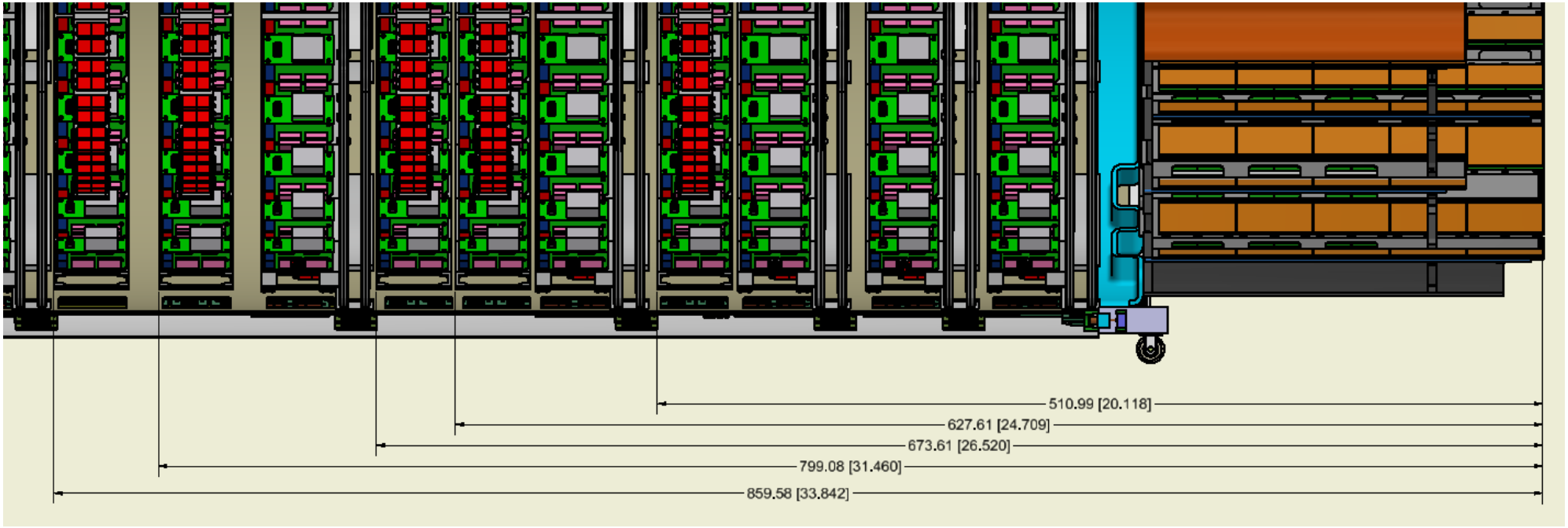
Recent work at Cornell to optimize location of TBPX port cards by nudging disks…

TBPX Port card locations

- Attempt to move last frame closer by nudging TFPX disk 3 by -15mm to make room
- Would reduce length of e-links for barrel

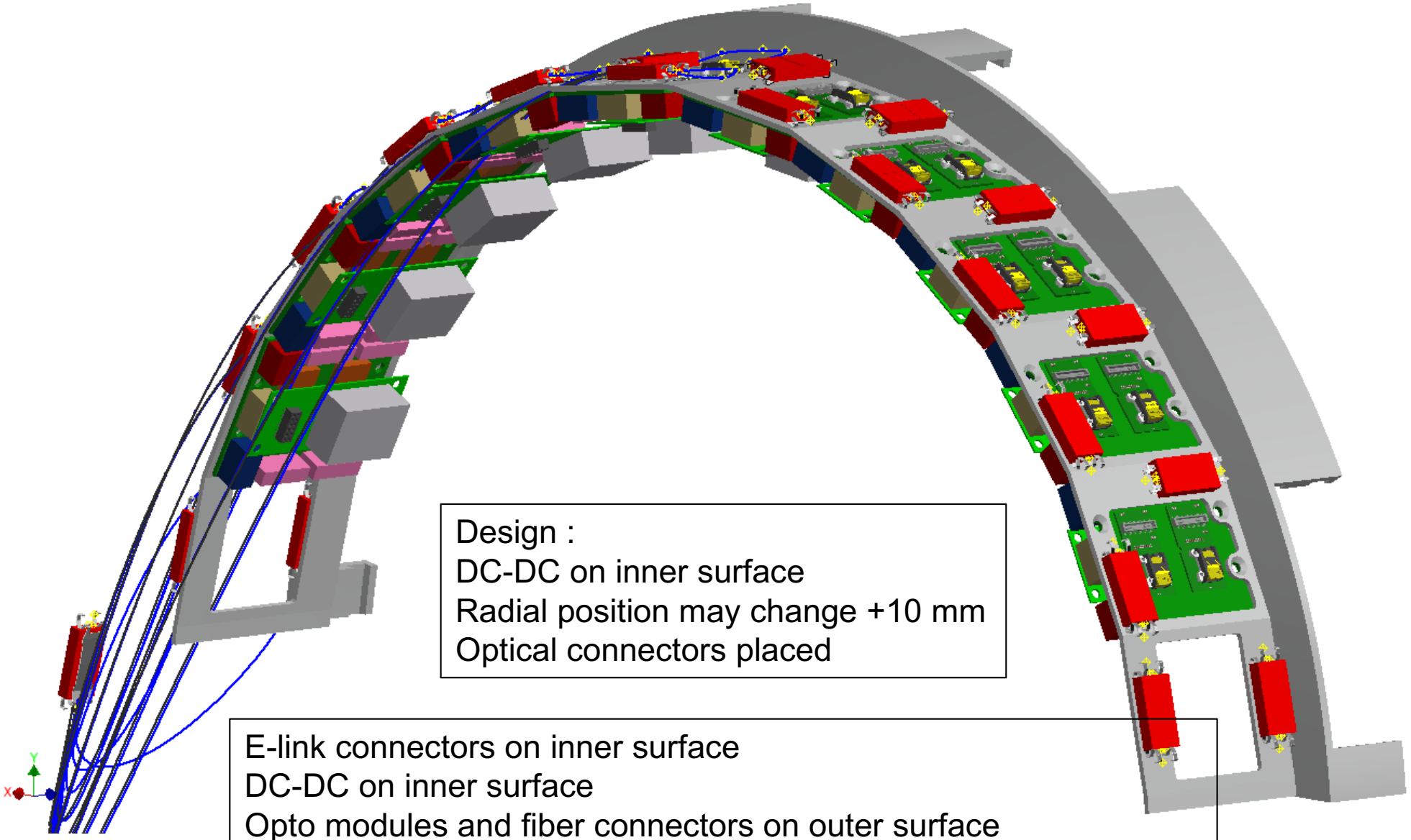


With TFPX disk 3 moved -15mm



- Fully packed – longest distance reduced by ~12cm
  - Helpful for e-link length (1.5 cm shift for 12 cm)
- To be seen if there is enough clearance
  - Mockup being made this summer
- Impact on physics studied and found minimal
  - Number of hits vs η changes by few% wrt baseline

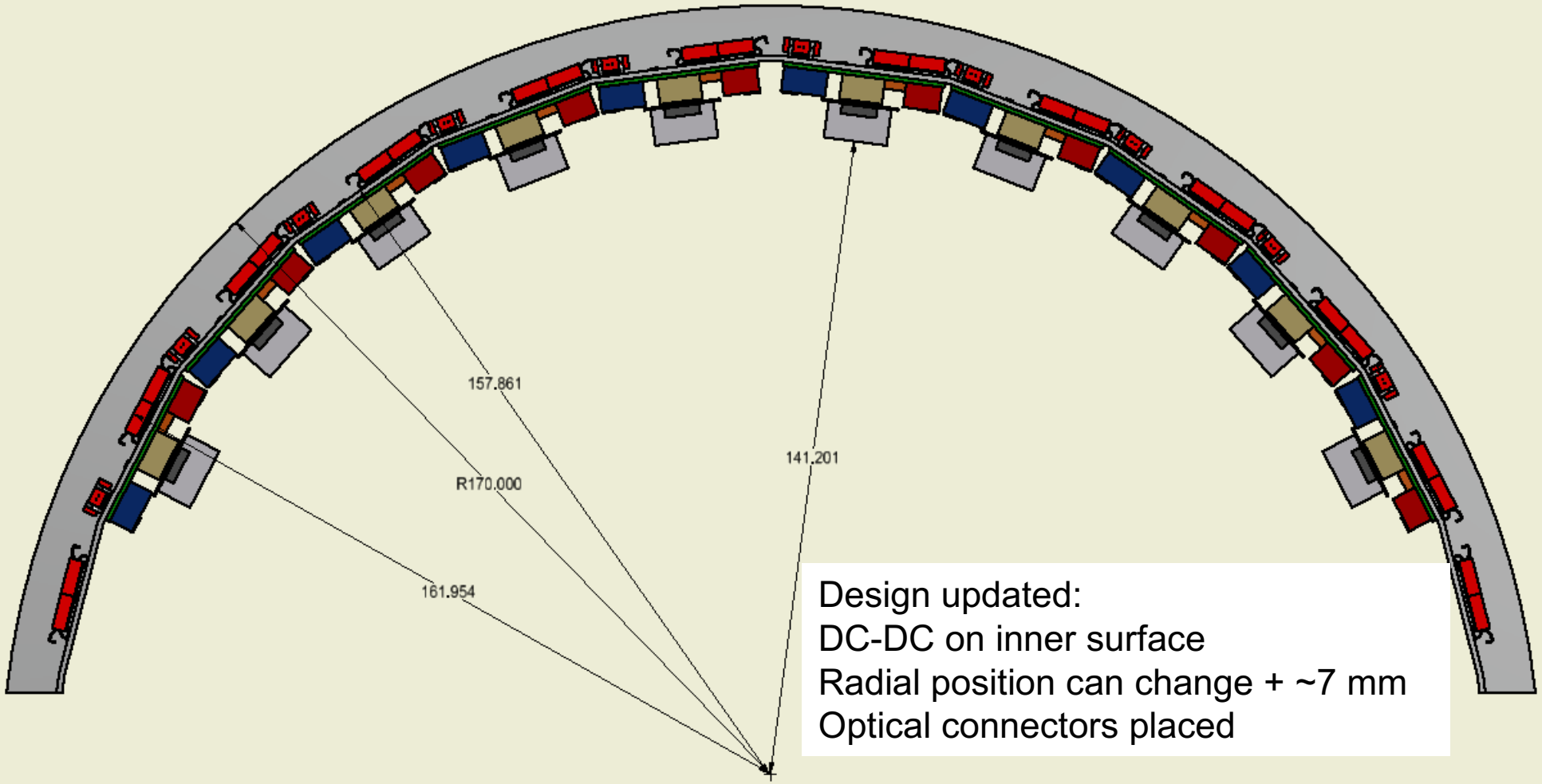
TFPX/TBPX Port Card Frame



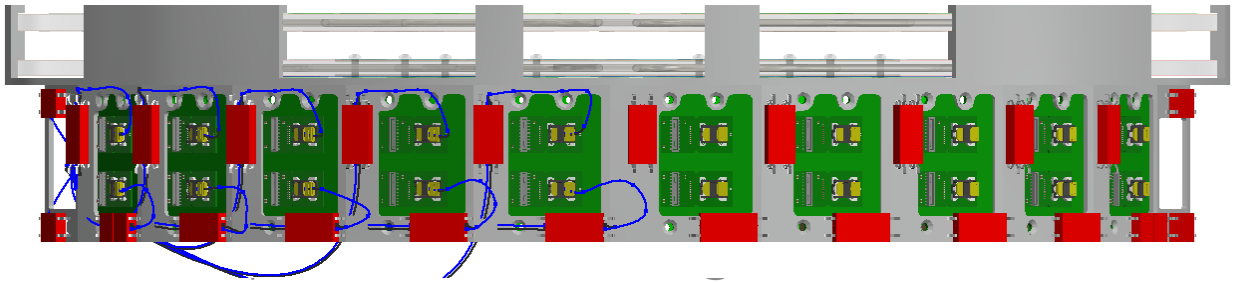
Design :
DC-DC on inner surface
Radial position may change +10 mm
Optical connectors placed

E-link connectors on inner surface
DC-DC on inner surface
Opto modules and fiber connectors on outer surface
(2 lit fibers per VL+ on 12 fiber ribbon) fan in to 24 fiber connector

Location of Port Cards



Design updated:
DC-DC on inner surface
Radial position can change + ~7 mm
Optical connectors placed



Summary of Recent Updates

- Recent work is on integration
  - Fiber connectors moved out to larger radius
  - Keep VL+ optical TRx outward in r for radiation reasons
  - DC-DC mezzanines mount inward in r
  - BPIX port card locations & TPFX disk “nudging”
  - Details also given by Yadira in the mechanics meeting May TK week
- For the lpGBT board itself
  - lpGBT pinout now available, but warning of changes to come before chip submission: waiting on submission before pushing layout
    - (Meanwhile Ted is working on irradiation / test adapter boards for sensor irradiation)
  - Settled on DC-DC mezzanine on inner radius side of port card
  - Ted has started winding & testing inductors for DC-DC
    - One sample bPol12V mounted on test board for tests
  - Still looks possible to serve TEPX, TFPX, TBPX with the same lpGBT module / port card or modified versions with same electrical design to optimize layout for mechanical reasons

To DC-DC or not?

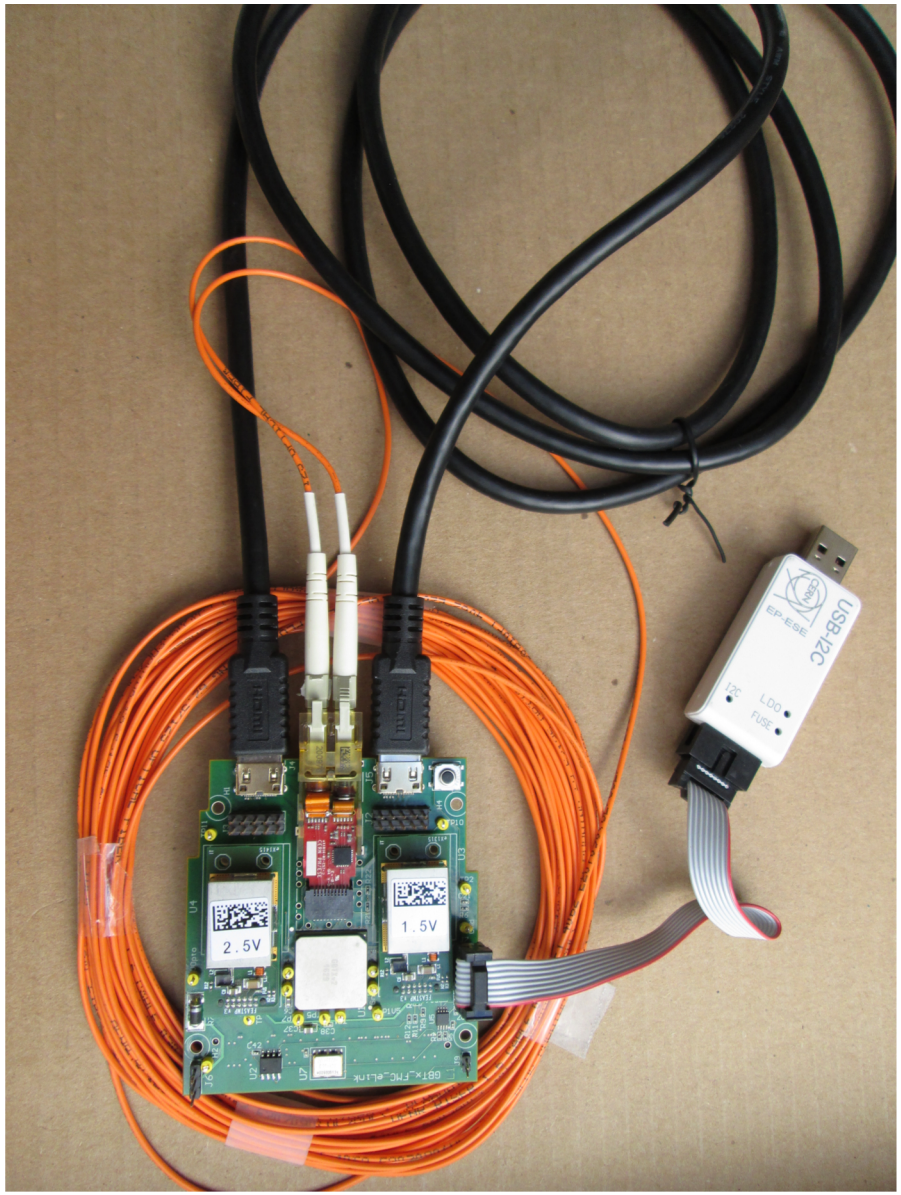
- We might consider dropping the DC-DC and just bring enough power fort port cards directly.
  - Baseline (TDR) plan had DC-DC to reduce ohmic losses on power cables
  - Follows the OT module design where lpGBT is powered by DC-DC (with everything else)
  - Two voltages
    - lpGBT is 65 nm and needs 1.2 V
    - VTRx+ needs 2.5 V for VCSEL
  - Not that much power
    - Estimate (to update) is a few Watts
      - TDR says 1.2 kW for 1260 lpGBT (no DC-DC efficiency here?)
      - lpGBT <750mW, VTRx+ <??? mW (10 mA laser bias ~25 mW)

Backup

Prototype made with GBT and VTRx

Ted made a test
Board using GBT parts

(Spring/summer 2017)



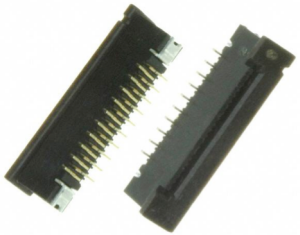
Works with basic
PRBS test mode
Control via I2C
Interface to GBT test
Board (CERN)

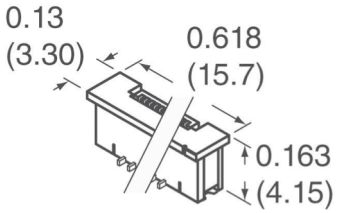
Not much use in
Further tests

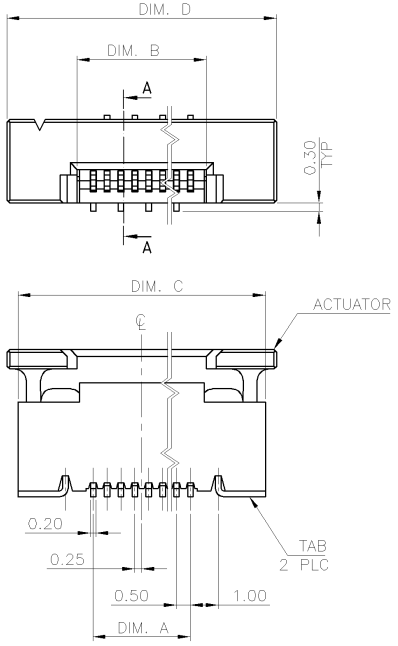
- Lower speed
- Different protocols

Connectors

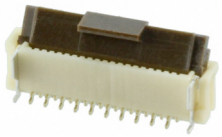
- Looking for glass filled thermoplastic materials
  - AMP : 2-1734742-0
    - Locking rely solely on friction of the fingers inside the connector to hold the cable





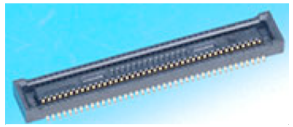


  - The bale mechanically locks the cable
- Hirose
  - FH12-20S-0.5SVA(54)

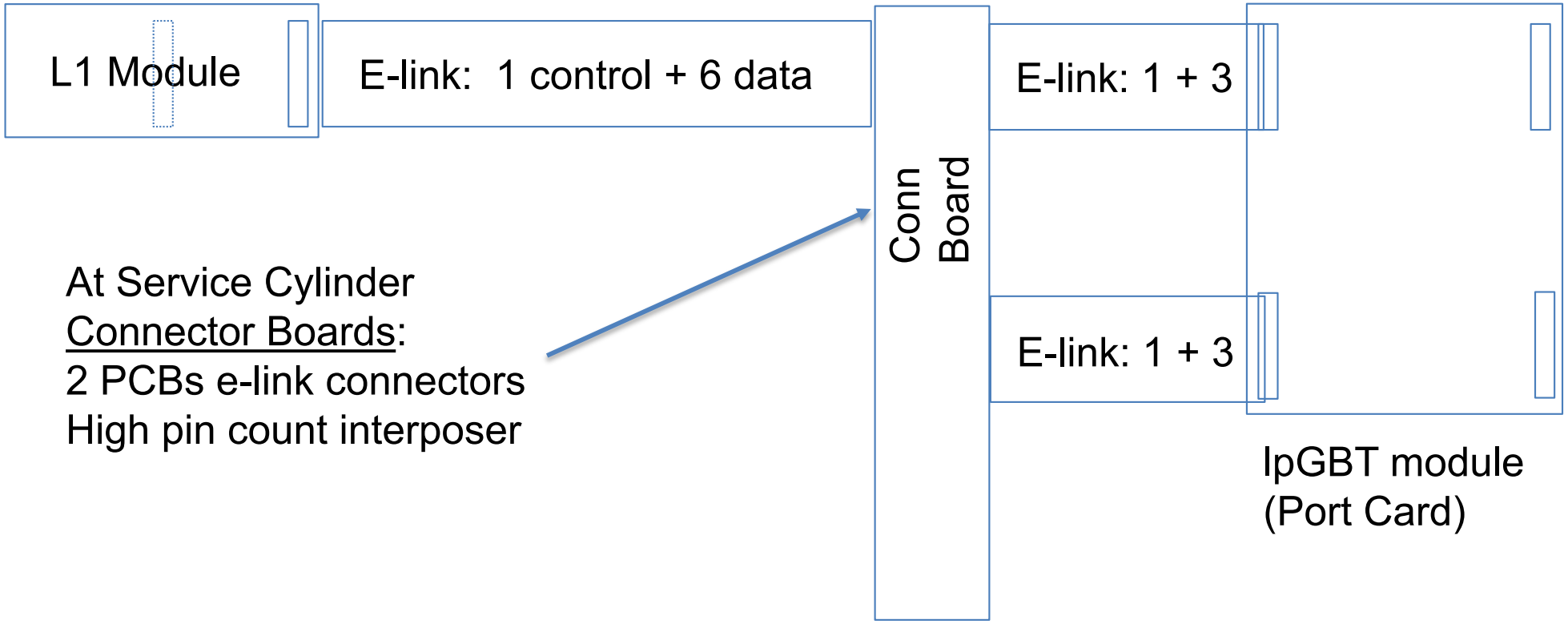


  - FH40-20S-0.5SV

  - DF40HC(3.5)-40DS-0.4V(51)



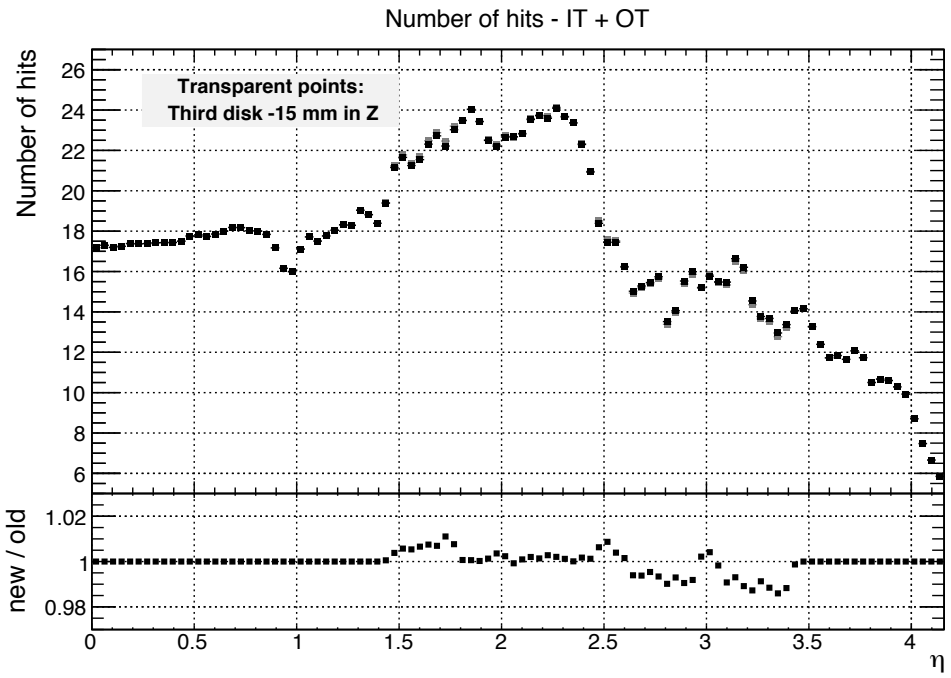
Note on TBPX E-links

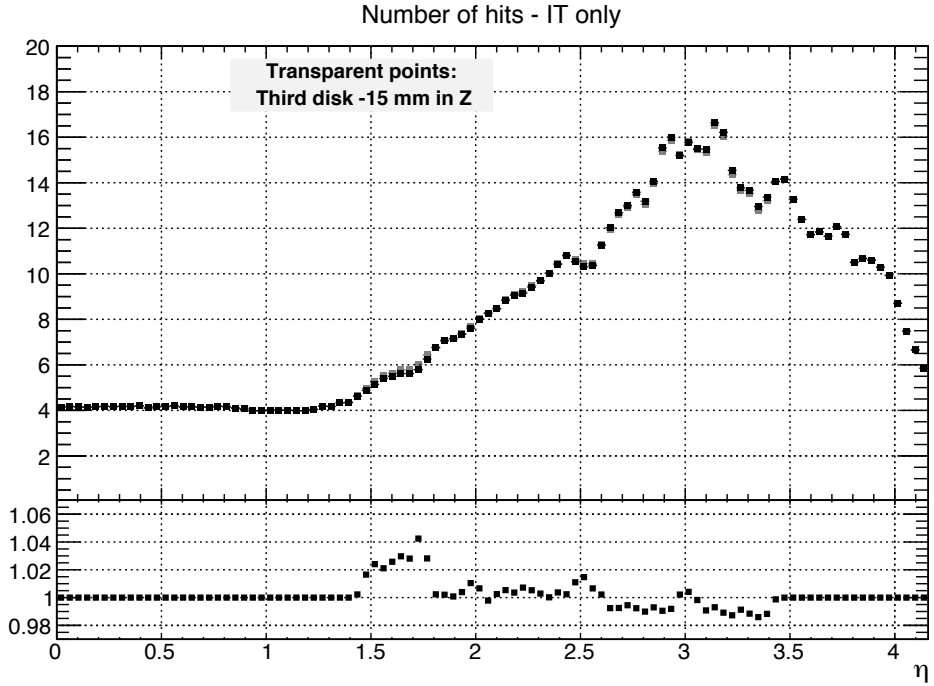


- Layer 1 modules have two ROCs and 6 data links
  - May use two 3+1 cables (space?)
  - But can also change from 6+1 to 2*(3+1) at connector board
- Connector boards – thin in r, outside of service cylinder
  - Allows connections for BPIX e-links in two (?) places each port card frame

Move of disk 3

- Andre Frankenthal (Cornell) studied in tkLayout
  - http://home.fnal.gov/~as2872/layoutsDefault/ThirdDoubleDiskZ_Baseline
  - http://home.fnal.gov/~as2872/layoutsDefault/ThirdDoubleDiskZ_Moved
- Impact on # hits at the few% level
- Resolutions are also affected at the few% level in the region of disk3
- Details at links above – see also simulation meeting





VersaLink+ Links

- OptoLinks (VL+, VTRx+ lpGBT) at ACES 2018 (Francois Vasey)
- VL+ at TWEPP 2017 (Jan Troska)
- LpGBT e-space