Elinks for the IT phase-2 Upgrade

Alice Bean, Robert Young, Sadia Khalil, James Ballard, Sam Glaser,
Tanner Lankford, Devdatta Majumder

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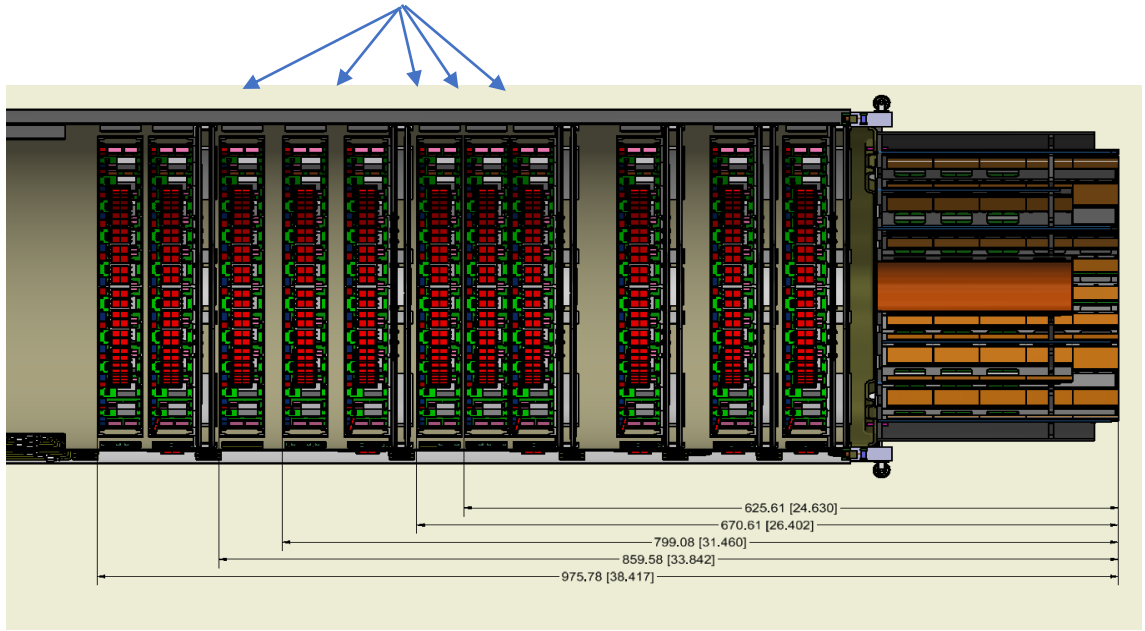
E-links: Introduction

- Each LpGBT can support 7 upstream and 7 downstream signals.
- Each module has 1 control downstream link at 160 Mb/s that receives the data via a 2.5 Gb/s downstream optical link
- Upstream readout links at 1.28 Gb/s

QUARTER OF IT		Multiplicity (#ladders, #disks)	#modules per ladder/ half ring	#Links per module	Total #Links (short)	Total #Links (long)
TBPX	L1	6	4 (short)/ 5 (long)	6	144	180
	L2	14	4 (short)/ 5 (long)	2	112	140
	L3	12	4 (short)/ 5 (long)	1	48	60
	L4	16	4 (short)/ 5 (long)	1	64	80
	SUM				368	460
					Total #Links for N*half disks	
TFPX	R1	8	10	3	240	
	R2	8	16	2	256	
	R3	8	12	2	192	
	R4	8	16	1	128	
	SUM				816	
TEPX	R1	4	20	1	80	
	R2	4	28	1	112	
	R3	4	18	1	72	
	R4	4	20	1	80	
	R5	4	24	1	96	
	SUM				440	
				Quarter of TBPX+TFPX	1184	1276
				Quarter of TEPX	440	
				Quarter of IT	1624	1716
				One end of IT	3248	3432
				Entire IT	6680	

TBPX Port Cards can fit between disks in some locations



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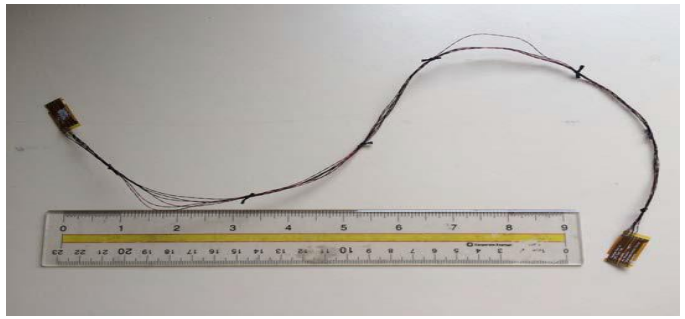
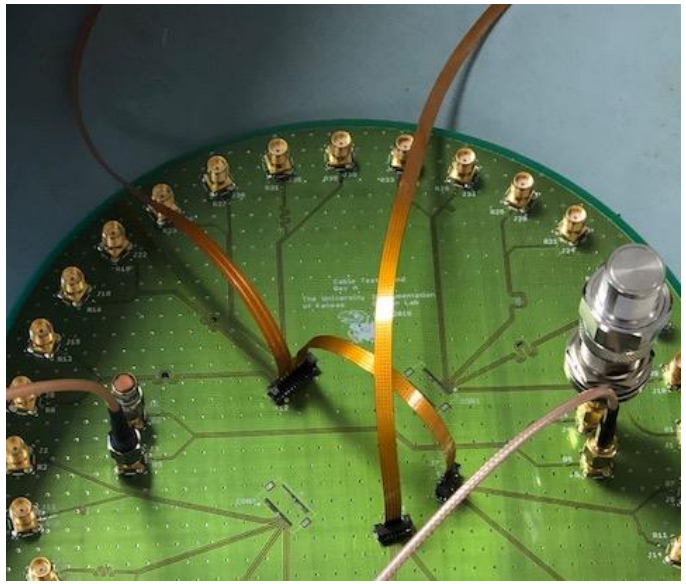
IP

TFPX & TEPX needs short eLinks

E-links Status

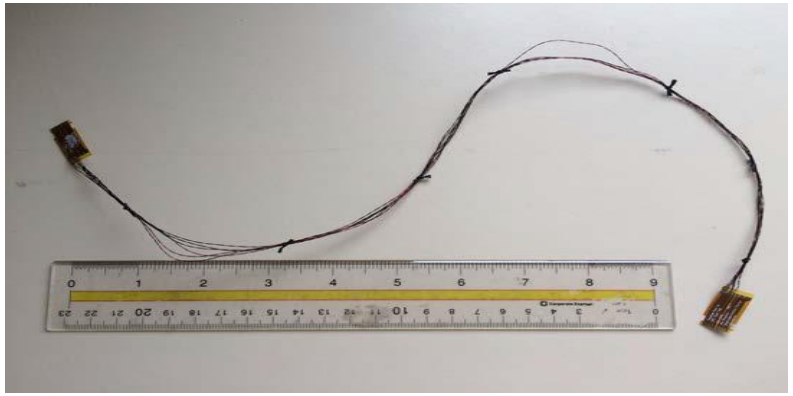
- **Cables under test**
  - FFC-bifurcated with 10cm/1.5m leg
    - Ordered 20 from ColtTech in Kansas City. Will be delivered on June 18
  - FFC-bifurcated with 10cm/1.m leg
    - Received 20 from a Chinese company on June 13
  - Manufactured 1m and 2m long micro-twisted pair cables



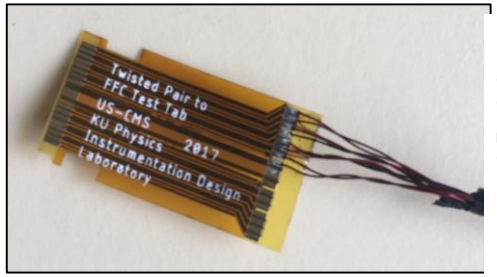


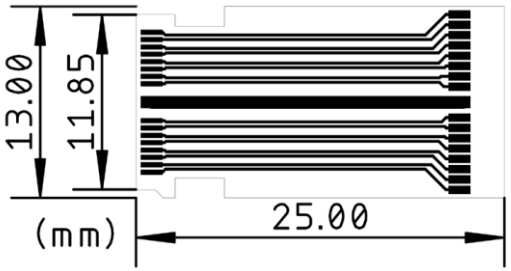
- **Activities**
  - BERT to test bit errors up to 1.28 Gbps at KU (FPGA board: VC707) and setting it up at CERN (FPGA board: KC705)
  - S-parameter tests and eye diagrams using Vector Network Analyzer (CERN) or FPGA board (KU)
  - Setting up a test stand to connect with RD53A board using small PCB cable adapter from Display Port to SMK or AMP connectors (Details in coming slides)
  - Prepare for Radiation campaigns (first in July): Delivered the TP cables, and will be sending more as they will become available

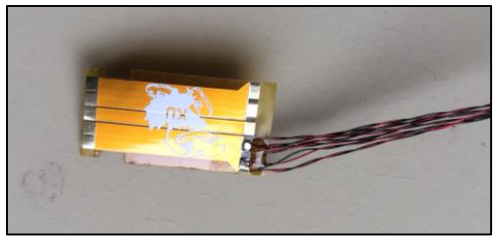
Reminder: Twisted Pair Cable

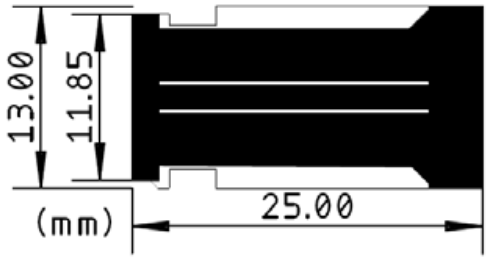


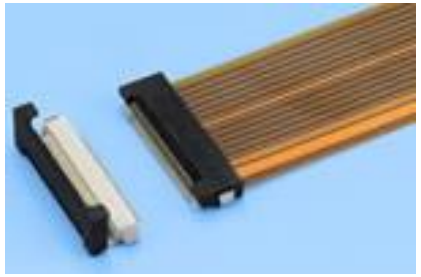
- *The material used is Cu with double QML Kapton insulation with 4 twist/inch and thickness of 36 AWG that were used for ATLAS nSQP cables*
- *The FFC tabs are connected to 4 differential pairs per cable. The front side has signal differential pairs and one heavy trace to simulate the high-voltage bias. The bottom face split up into three heavy traces to be used as grounds or to power the electronics*
- *Cables uses SMK connectors used in phase-1 TFPix*









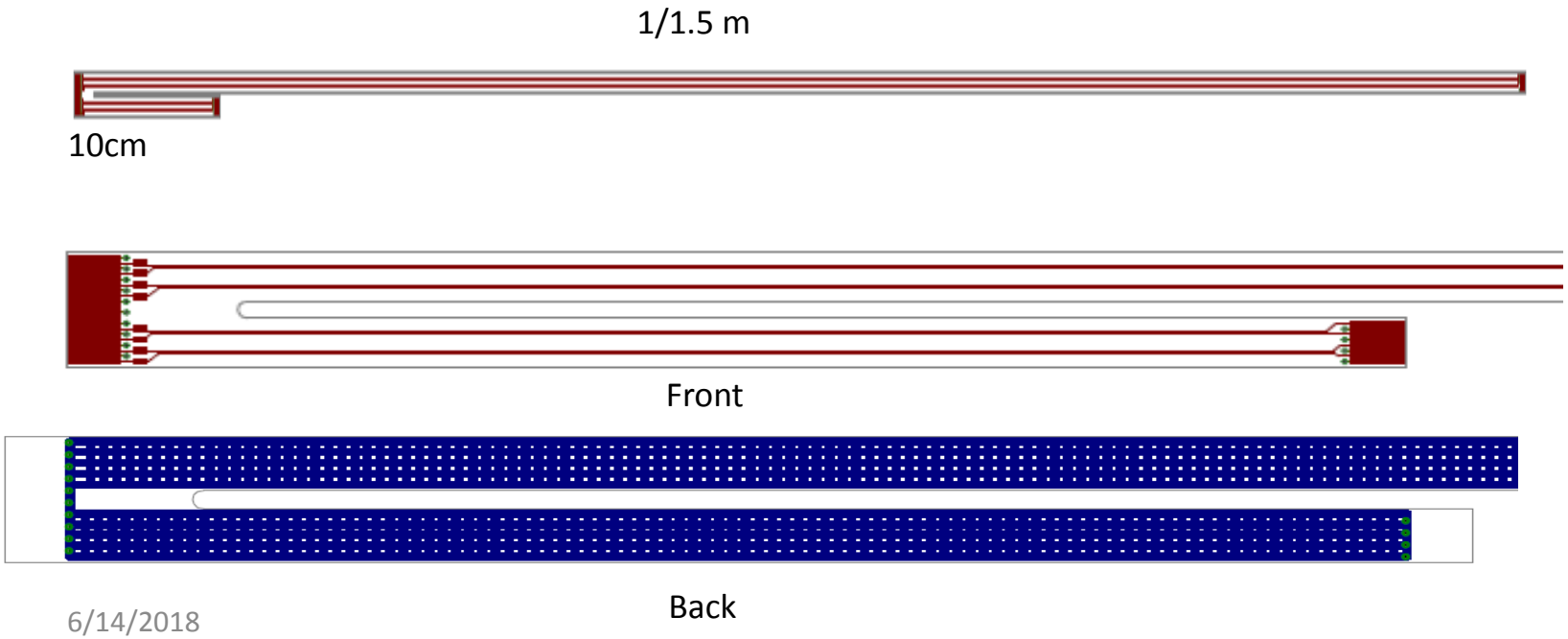


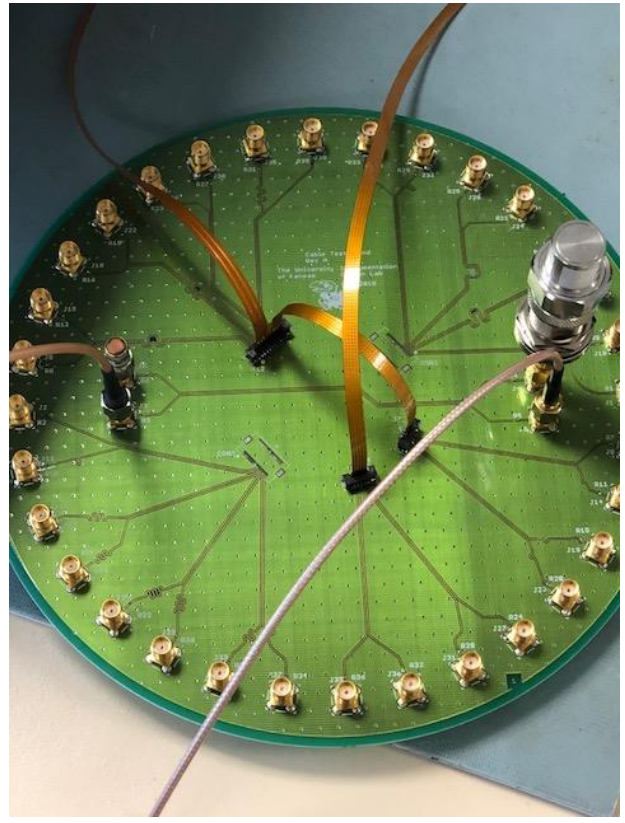
Initially, we have a shortage of these connects but now have recently recovered some from CERN (Thanks to Will Johns!)

EF-5D Series 0.5mm Pitch used for Phase-1 FPX flex cables, 20 contacts per size, 100 Mrad tested

Flat Flex Cable Prototype

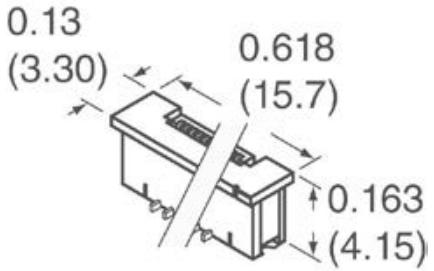
- Material and connectors
  - *The cables are made up of two 0.13 mm thick polyamide layers, with additional 0.2 mm stiffener added to meet the connector requirement.*
  - *The ends have gold fingers, with left side being connected to the 20 pin AMP connector and the two right hand sides being connected to two 8 pin AMP connectors (See next slide).*
  - *The weight of Cu traces is 1oz assuming thickness is 35 μm.*



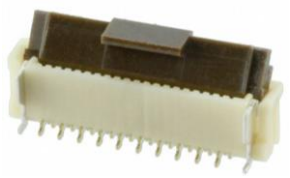


Alternate FFC Connectors (In stock)

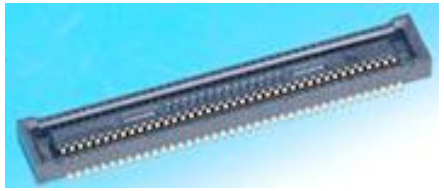
- AMP 2-1734742-0 (20 and 8 pins) and is default for bifurcated FFC
  - Has sliding bale: no locking mechanism and the connection is hard to make
  - Right now we have the 0.5mm spacing but the HDIs are looking at 0.3mm spacing



- Hirose: *FH12-20S-0.5SVA(54)*, *FH40-20S-0.5SV*, *DF40HC(3.5)-40DS-0.4V(51)*

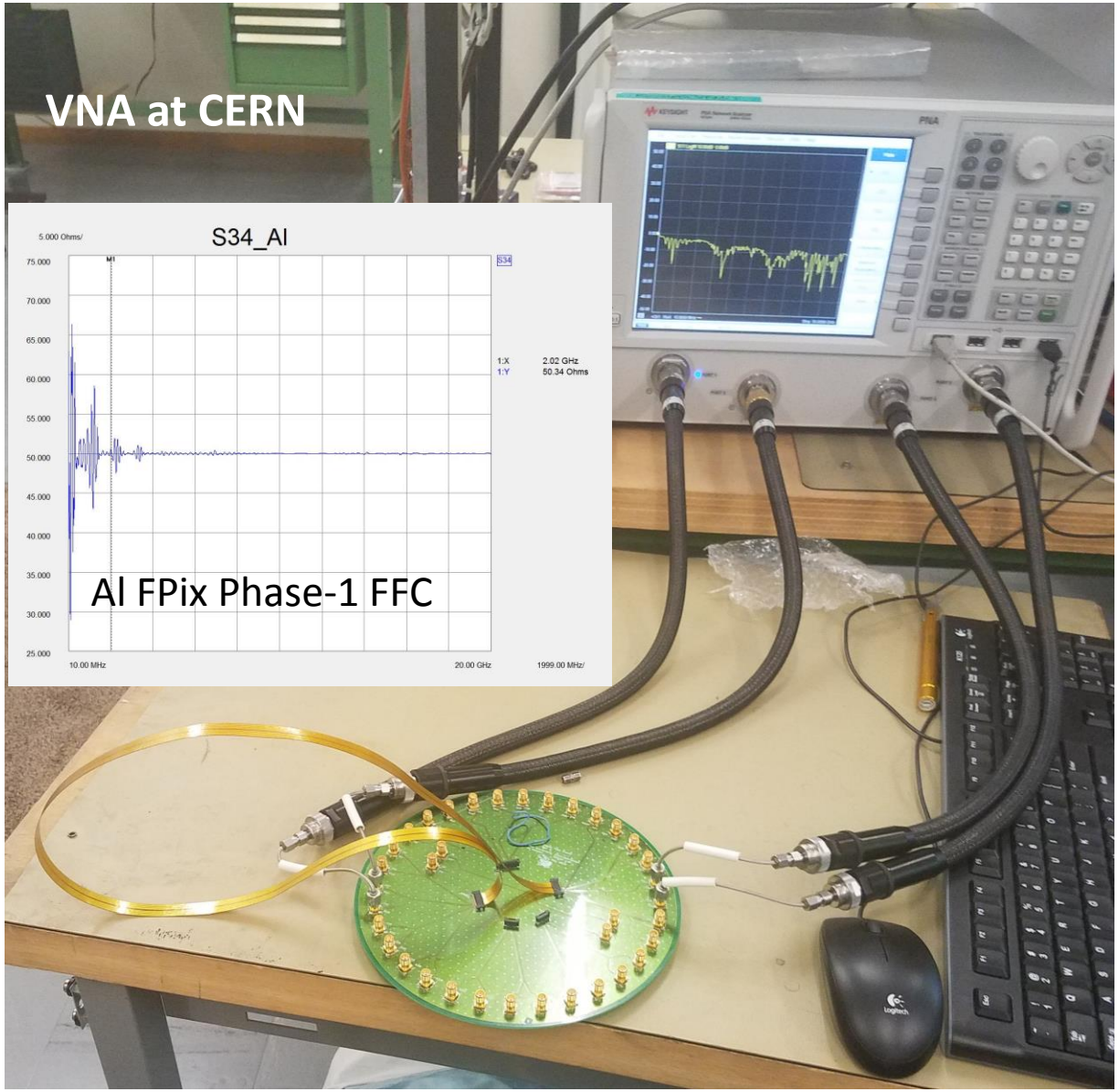


Default for now for the port cards



Cable test Round Board

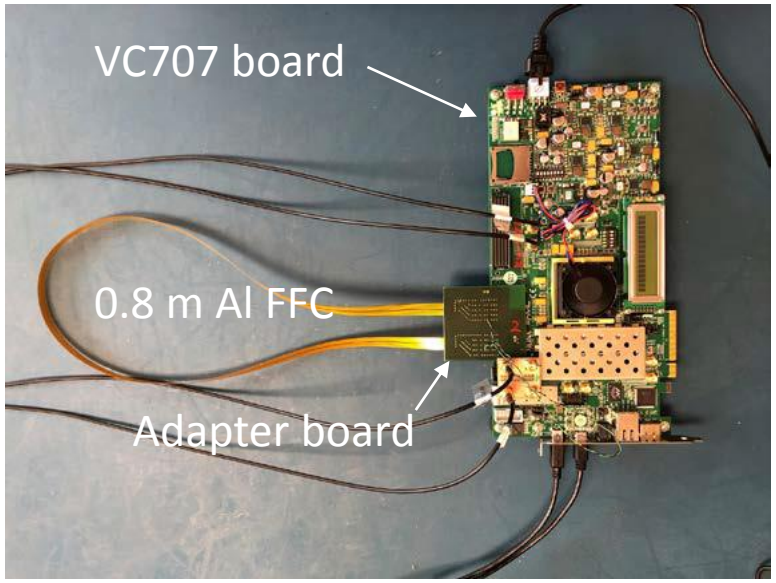
- It’s an 8 inch round board, that can connect either SMK or AMP connector for each differential pair to two SMA connectors
- Used with Vector Network Analyzer and test stand to connect with RD53A board

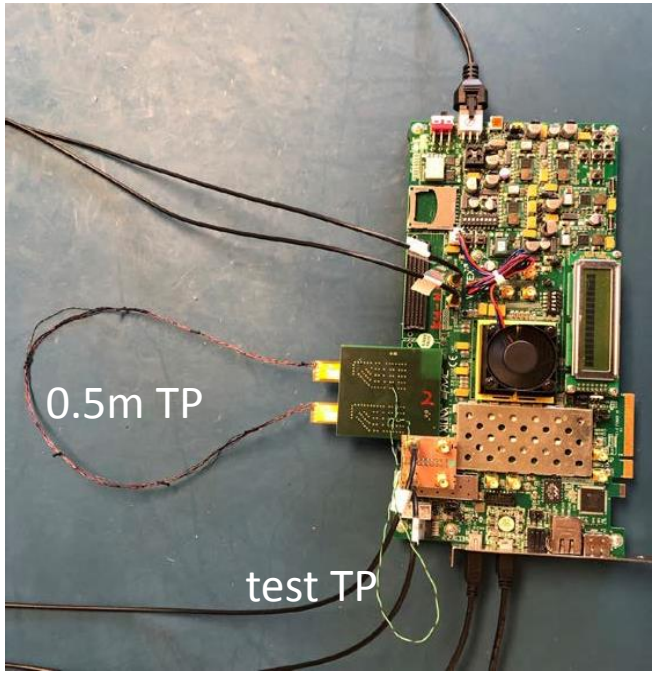


BERT at KU & CERN

- Tests run at 400, 640 and 1280 Mbps

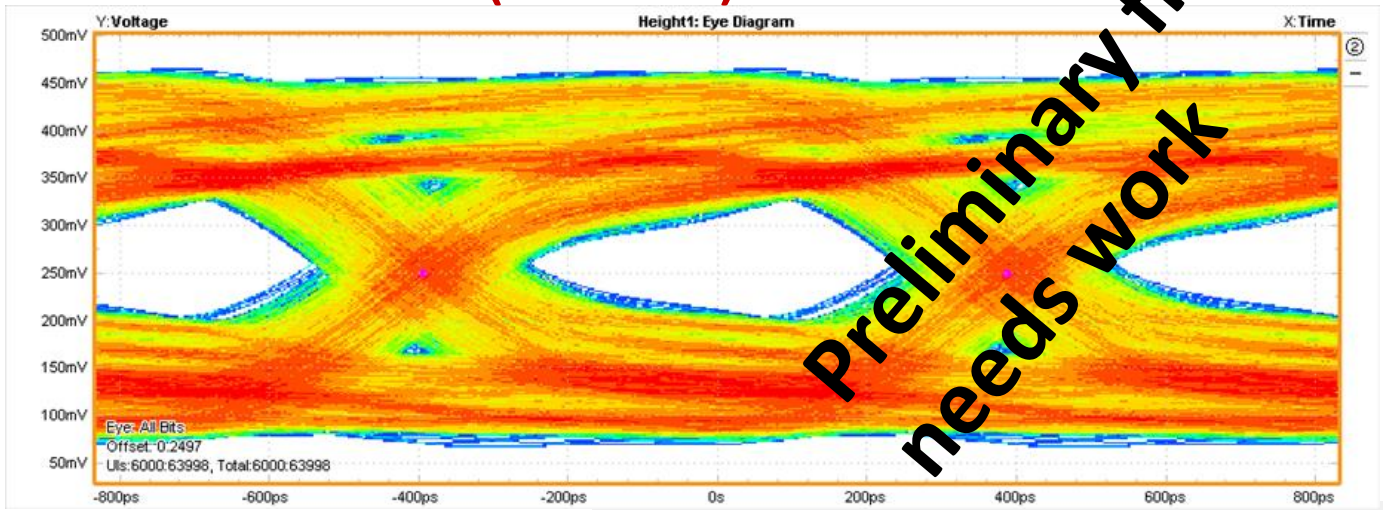
Cables	400 Mbps	640 Mbps	1.28 Gbps
0.762m Al FFC (phase1)	0 err/10^{10} bits	0 err/10^{13} bits (CERN)	
0.51m long TP	0 err /10^{10} bits	0 err/10^{12} bits	
2m long TP	0 err /10^{10} bits		
Test TP cable		0 err /10^{10} bits	0 err/10^{12} bits





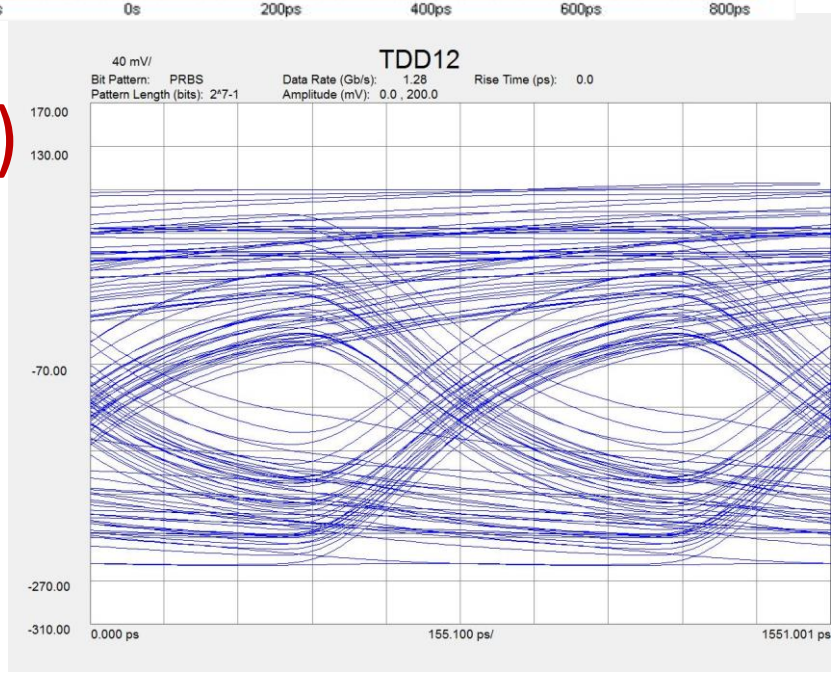
Eye Diagram

Chinese FFC (10 cm)



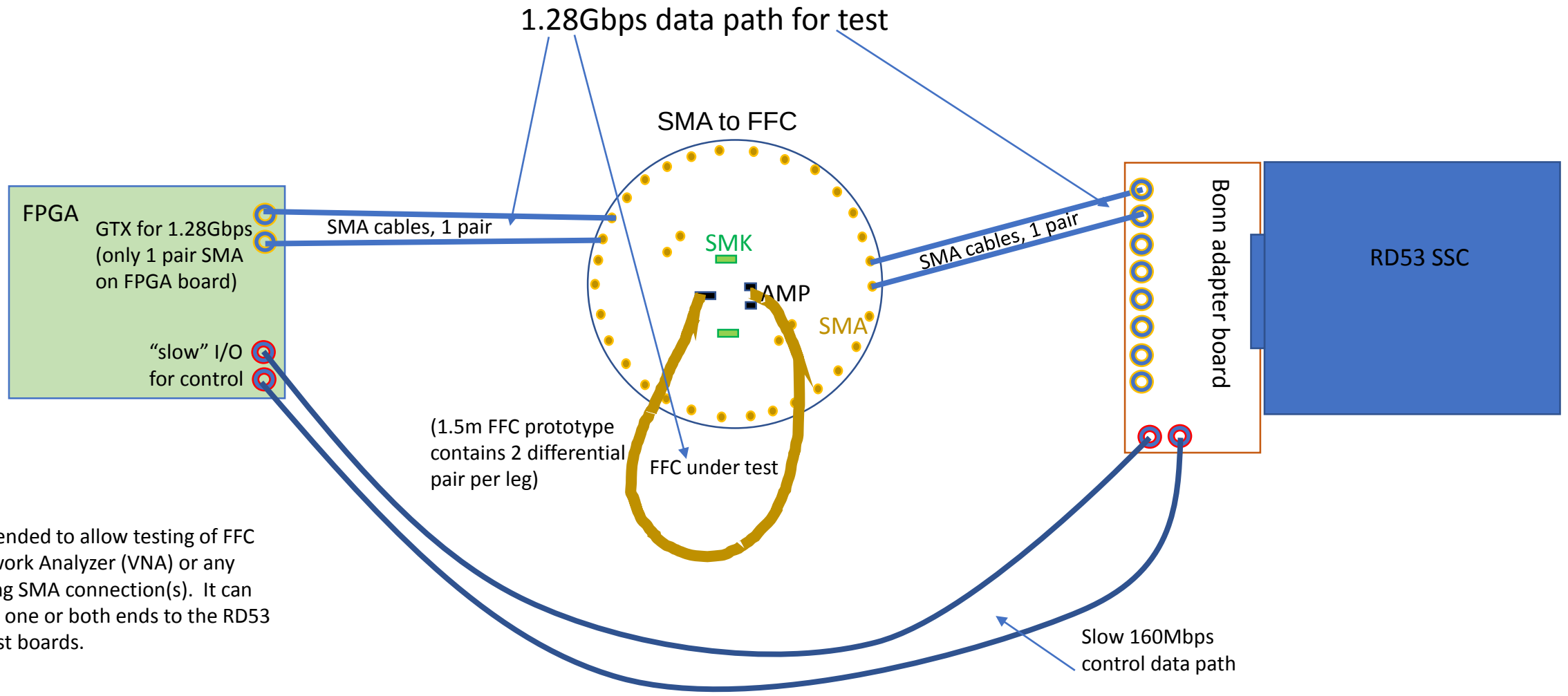
Preliminary first look, needs work

Al FFC (Phase-1) through VNA



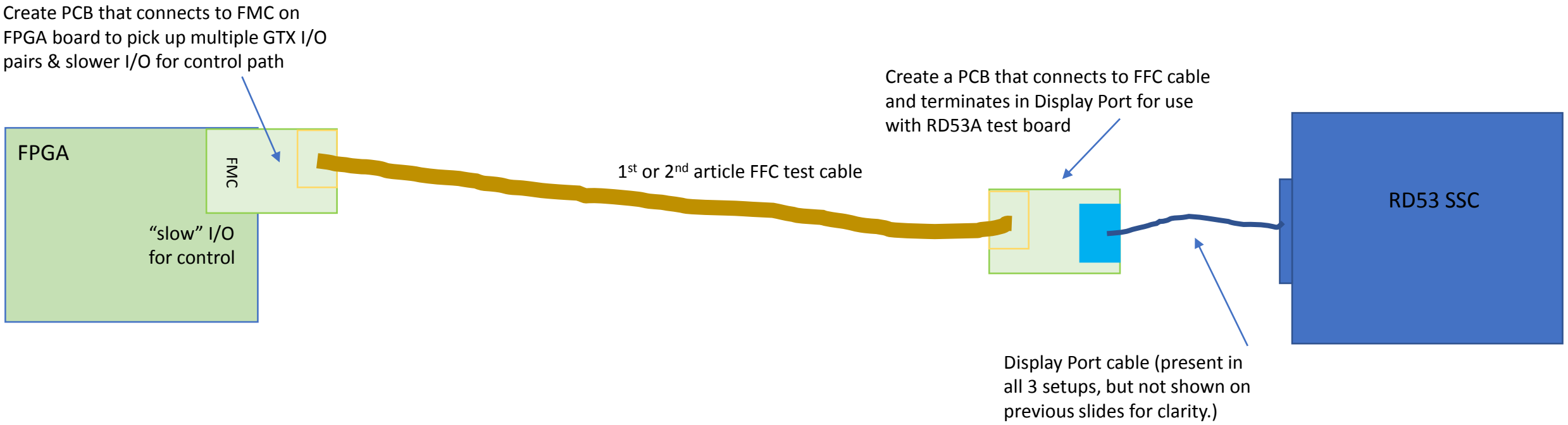
- Test setup for the Chinese manufactured FFC

Current Test setup with round board for RD53A



Round PCB is intended to allow testing of FFC on a Vector Network Analyzer (VNA) or any other device using SMA connection(s). It can be used to adapt one or both ends to the RD53 SSC and FPGA test boards.

Proposed test setup eliminating round board for RD53A



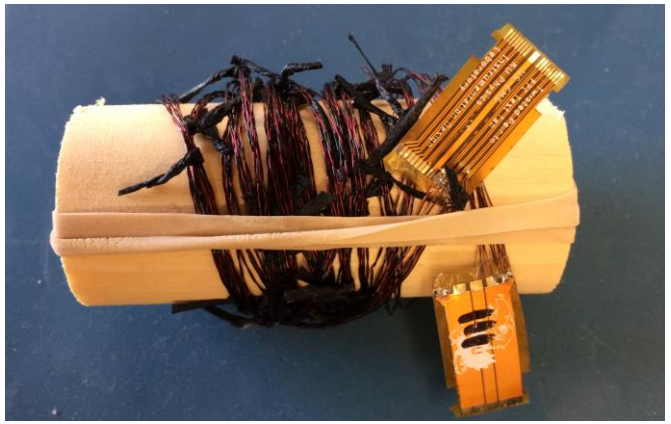
July Egamma Radiation Campaign

- We are in contact with Malte and has filled the document EDMS 1807333 from our side
- Dosage provided in this campaign will be 500Mrad (5MGy), where we require a cumulative dosage of 1.5Grad (15MGy)

List of samples and quantities

Materials	*Quantity*
Coupon board that houses 4 connectors	*2*
Hirose connectors of three families (in a bag)	*3+3+3=9*
Micro twisted pair cable of 1m length	*2*
Micro twisted pair cable of 2m length	*2*
FFC of 1.0m (long end) and 10cm(short end)	*3*
FFC of 1.5m (long end) and 10cm(short end)	*3*

Logistic of irradiation (Working with CERN Rad Camp contact)



Wrapped around 3'' long and 1.5'' diameter block

Backup

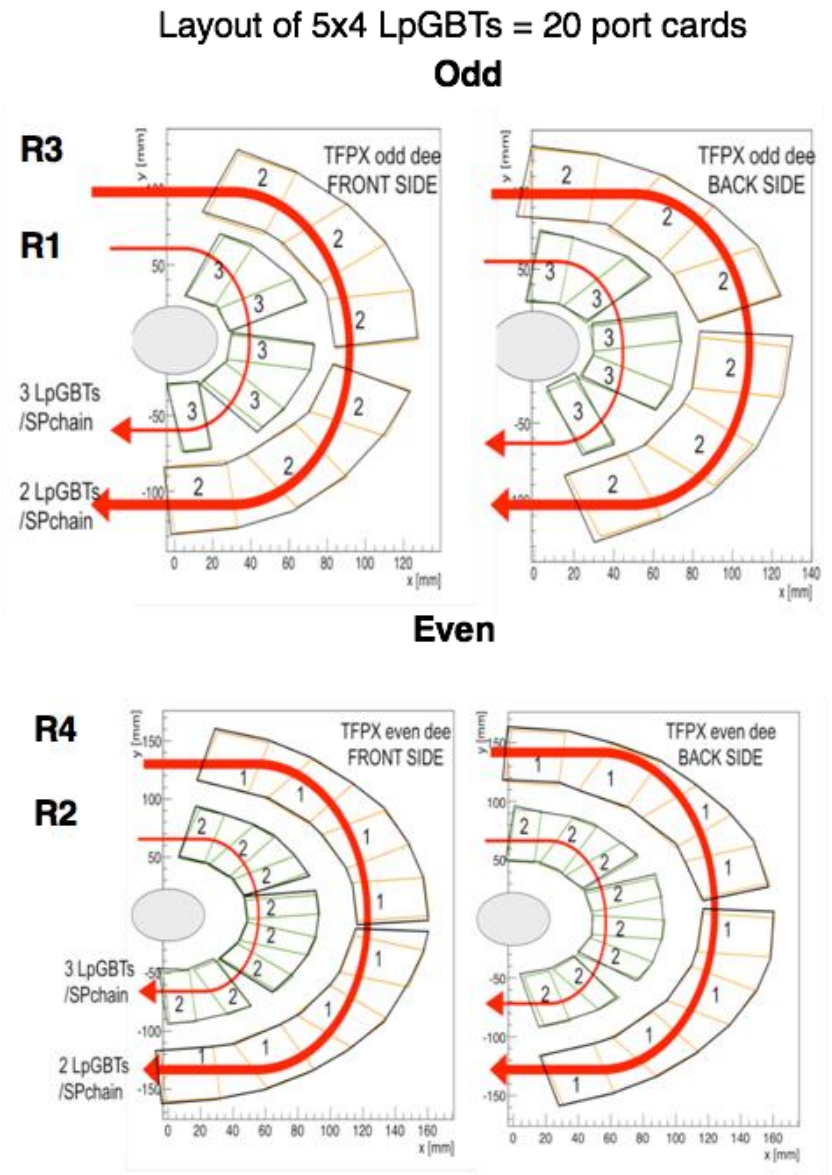
E-links: Flavor

- Elinks flavors are driven by the TEPX/TFPX power routing

A port card needs to max 6 uplinks and max 4 downlinks

Portcard	Ring	#mod	links/	tot link
1	R1	2	3	6
2	R1	2	3	6
3	R1	1	3	3
4	R3	3	2	6
5	R3	3	2	6
6	R1	2	3	6
7	R1	2	3	6
8	R1	1	3	3
9	R3	3	2	6
10	R3	3	2	6
11	R2	3	2	6
12	R2	3	2	6
13	R2	2	2	4
14	R4	4	1	4
15	R4	4	1	4
16	R2	3	2	6
17	R2	3	2	6
18	R2	2	2	4
19	R4	4	1	4
20	R4	4	1	4

TFPX



E-links: Flavor

- Elinks flavors are driven by the TEPX/TFPX power routing

A port card needs to max 7 uplinks and max 5 downlinks

Portcard	Ring	#mod	links/	tot link
1	R1	5	1	5
2	R1	5	1	5
3	R3+R5	7	1	7
4	R3+R5	7	1	7
5	R3+R5	7	1	7
6	R1	5	1	5
7	R1	5	1	5
8	R3+R5	7	1	7
9	R3+R5	7	1	7
10	R3+R5	7	1	7
11	R2	7	1	7
12	R2	7	1	7
13	R4	5	1	5
14	R4	5	1	5
15	R2	7	1	7
16	R2	7	1	7
17	R4	5	1	5
18	R4	5	1	5

TFPX

Layout of 5x2 + 2x2 + 2x2 LpGBTs = 18 port cards