Universität Zürich[UZH]
Physik-Institut
PAUL SCHERRER INSTITUT PSI

EPIX portcard

Lea Caminada

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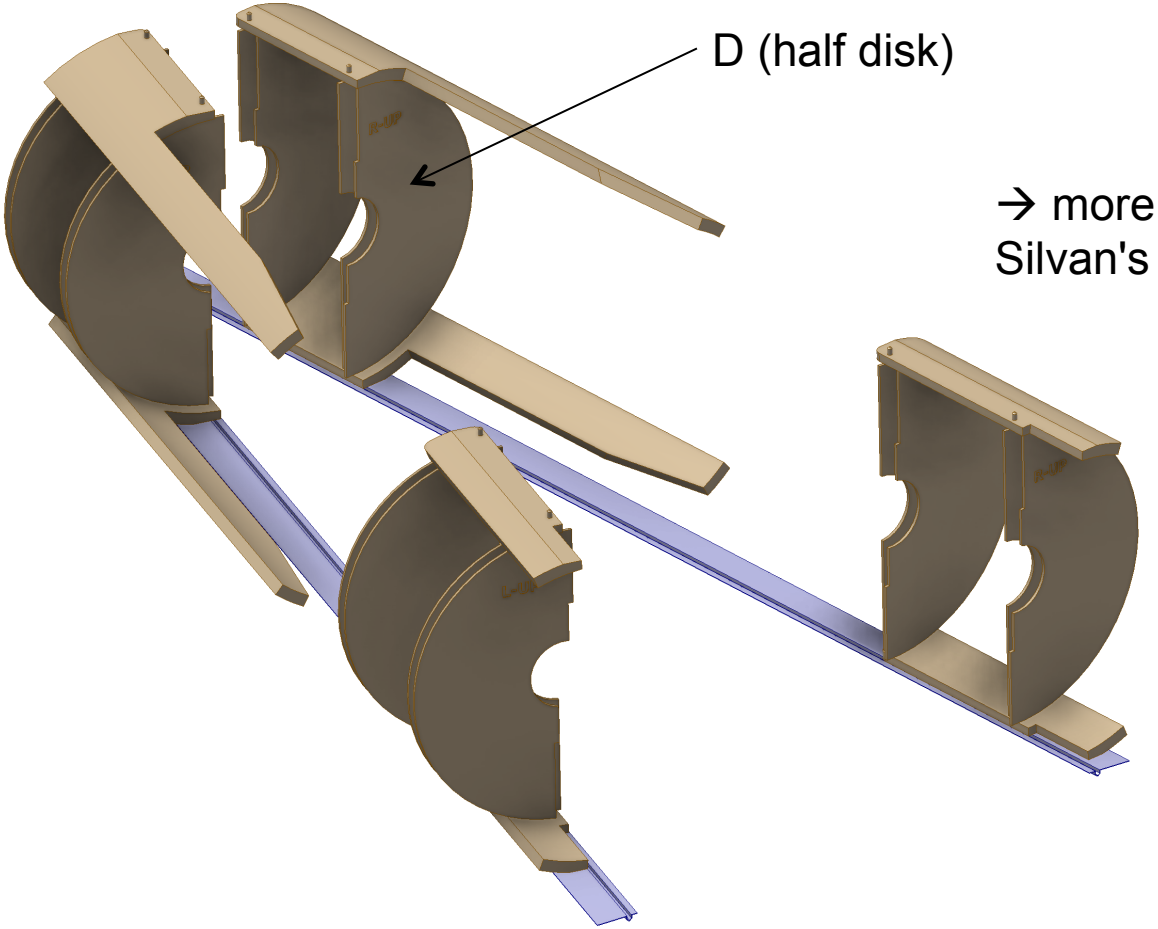
EPIX Services

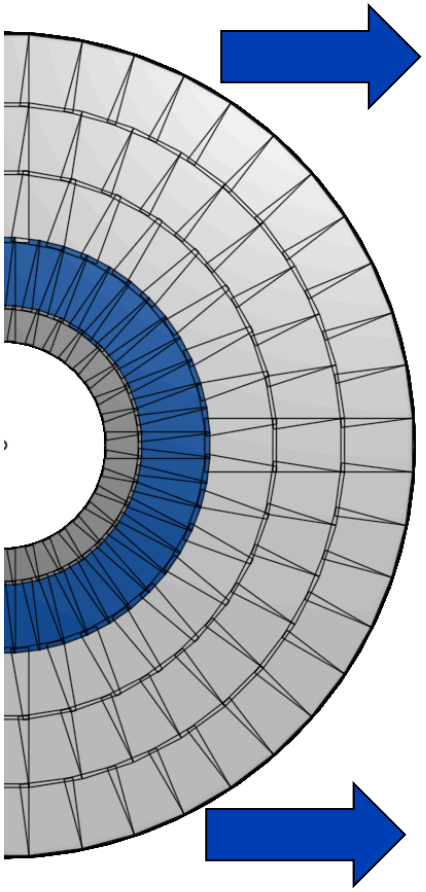
- Geometry of EPIX services different than FPIX services
  - phi segments vs half cylinder
- EPIX consists of 8 mechanical units with 2 Ds (half-disks) each
  - aim for common design of portcard for all Ds



→ more details in Silvan's talk

EPIX Services per D

- Based on module arrangement presented in Wolfram's talk
- Compared to TDR design
  - Fewer numbers of modules (and therefore elinks)
  - Same number of lpGBT (but less modules per lpGBT)
  - Larger bandwith for innermost ring (1 elink for 1 chip instead of 2)
- Services for each D in two slots (top and bottom)
  - 2 portcards per disk



	Ring 1	Ring 2	Ring 3	Ring 4	Ring 5	Total
#Modules	18	26	18	20	24	106
#ROCs	18	52	72	80	96	318
#elinks	18	26	18	20	24	106
#lpGBT	4	4	6*	4	*with Ring 3	18
#modules/ lpGBT	4.5	6.5	7	5		5.9

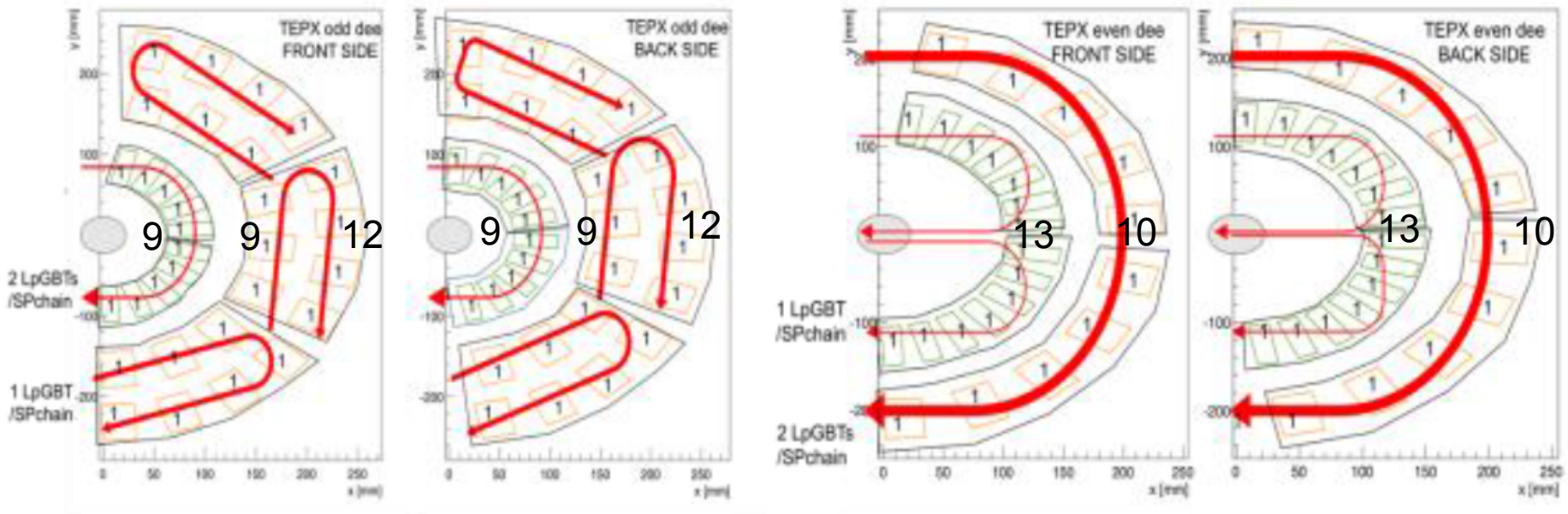
EPIX Services per D

- Connection scheme follows TDR layout

same lpGBT

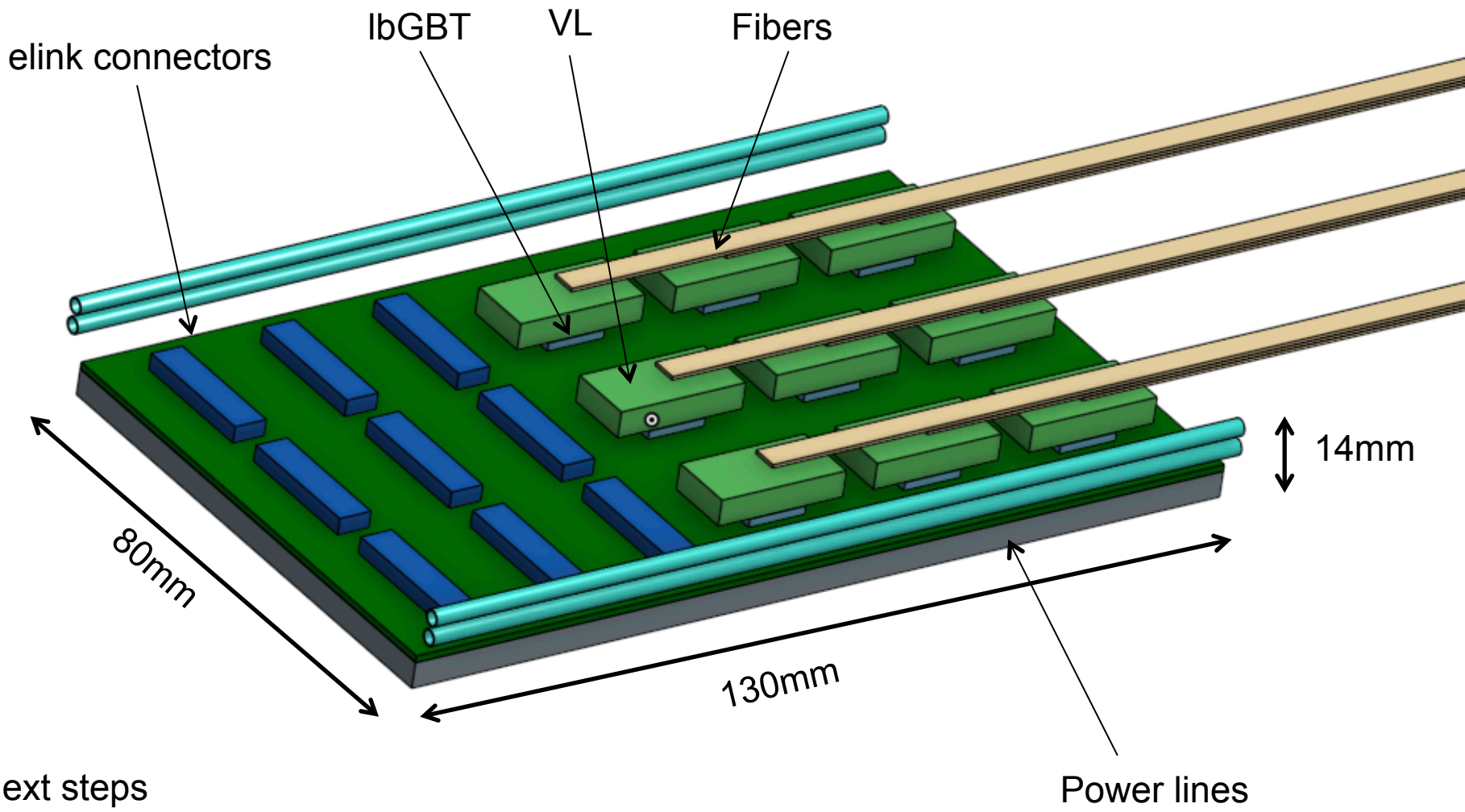
same serial powering group

Stella Orfanelli



- 2 portcards per D:
  - elink: 1 up/1 down link per module → 106 differential pairs per portcard
  - elink length up to 30-40cm
  - 9 lpGBT/VL per portcard
  - 1 elink connector per lpGBT → connecting to 4-7 modules

How the portcard could look like



Next steps

- Placement of module/lpGBT connectors: outside/inside?
- Placement of power lines, connectors?
- Elink design?

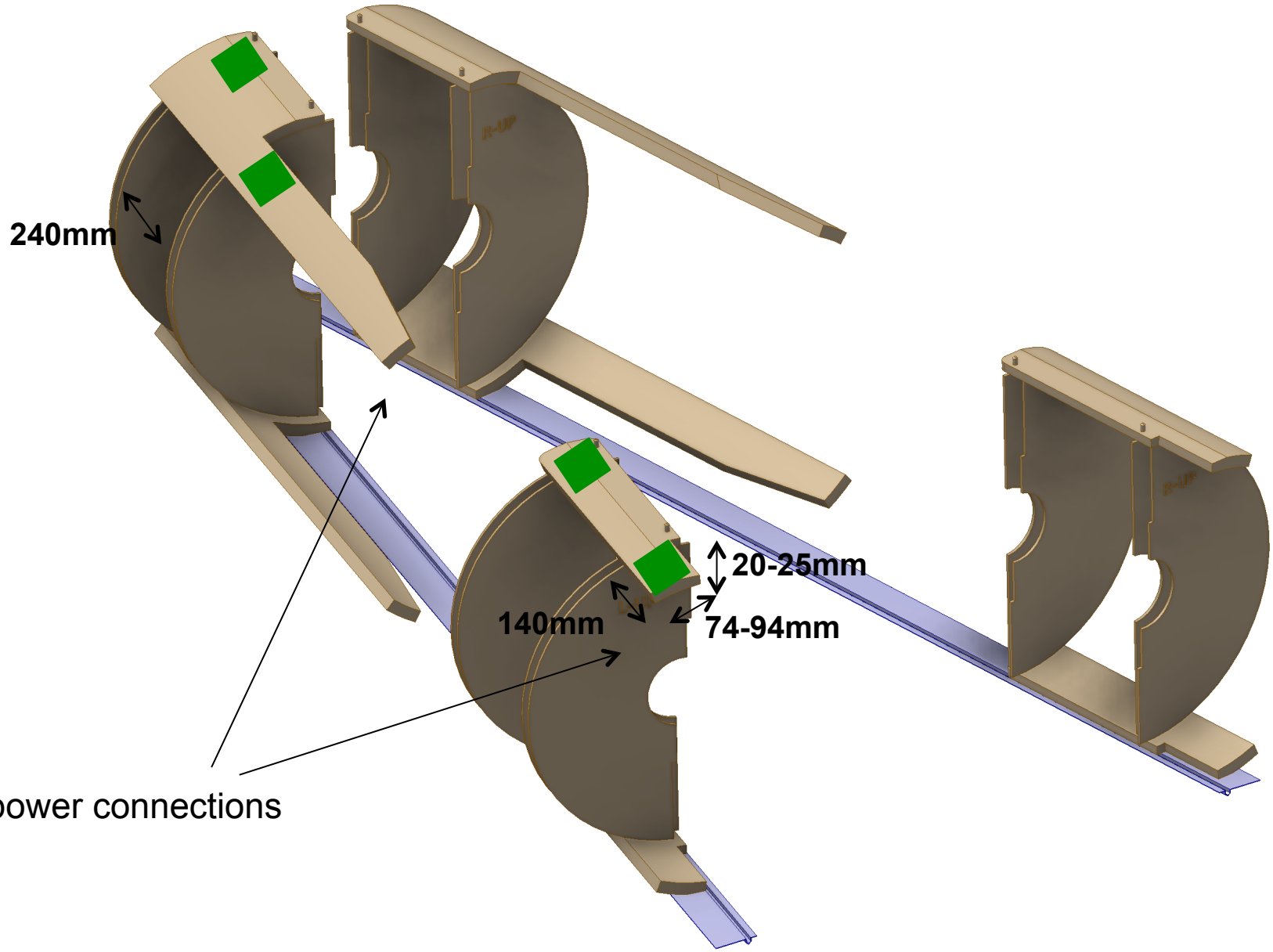
Powering of portcard

- TDR scheme based on 2 DCDC converters (11V→2.55V→1.25V)
- Is direct powering an option?
- Assuming one cable per portcard (powering 9 lpGBT/VL)

		Length [m]	xsec [mm^2]	I[A]	Vin[V]	Vout[V]	Power loss [W]
lpGBT	PS-PP1	85	3.5	5.4	8	3.6	24
	PP1-PP0	6	0.7	5.4	3.6	2.0	8
VL	PS-PP1	85	1.4	1.1	6	3.8	2.4
	PP1-PP0	6	0.7	1.1	3.8	3.5	0.3

- Power loss for one EPIX quadrant: 280 W (compared to 740W for detector power)
- Cable cross section for one EPIX quadrant:
  - 80mm^2 (compared to 670mm^2) for PS-PP1
  - 23mm^2 (compared to 280mm^2) for PP1-PP0
- Is there an option that fits within service constraints?

Where the portcard could be placed



Backup

1x1

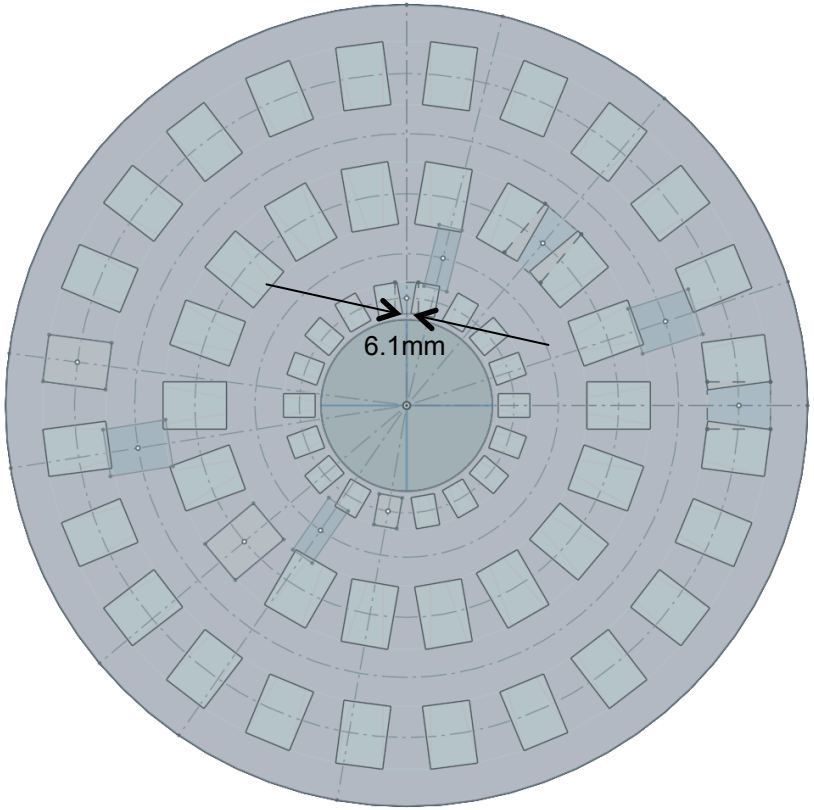
Advantages

- Smaller number of modules/ROCs per disk
- Reduced number of elinks per disk
- Increased elink bandwidth for innermost ring
- (Fewer number of modules per lpGBT)
- Increased minimal distance between modules on same disk → space for wire-bonding

At the cost of

- Additional module type

(Note however that 1x1 modules are already in the planning for sensor/module R&D)



from IT service document

EPIX	CHIP			MODULE			
	RO rate in Mbps for 750KHz	RO 1.28 Gbps Links per chip	Elink Occupancy per chip	#chips per module	Module Rate Mbps	RO 1.28 Gbps Links per module	Elink Occupancy per module
R1_lowCol	348	0.5	54%	1	881	1	69%
R1_highCol	533	0.5	83%	1			
R2_lowCol	206	0.5	32%	1	475	1	37%
R2_highCol	269	0.5	42%	1			
R3 lowCol	167	0.25	52%	2	688	1	54%
R3_highCol	177	0.25	55%	2			
R4 lowCol	121	0.25	38%	2	518	1	40%
R4_highCol	138	0.25	43%	2			
R5_lowCol	102	0.25	32%	2	442	1	
R5_highCol	119	0.25	37%	2			