Inner Tracker DTC requirements & specifications

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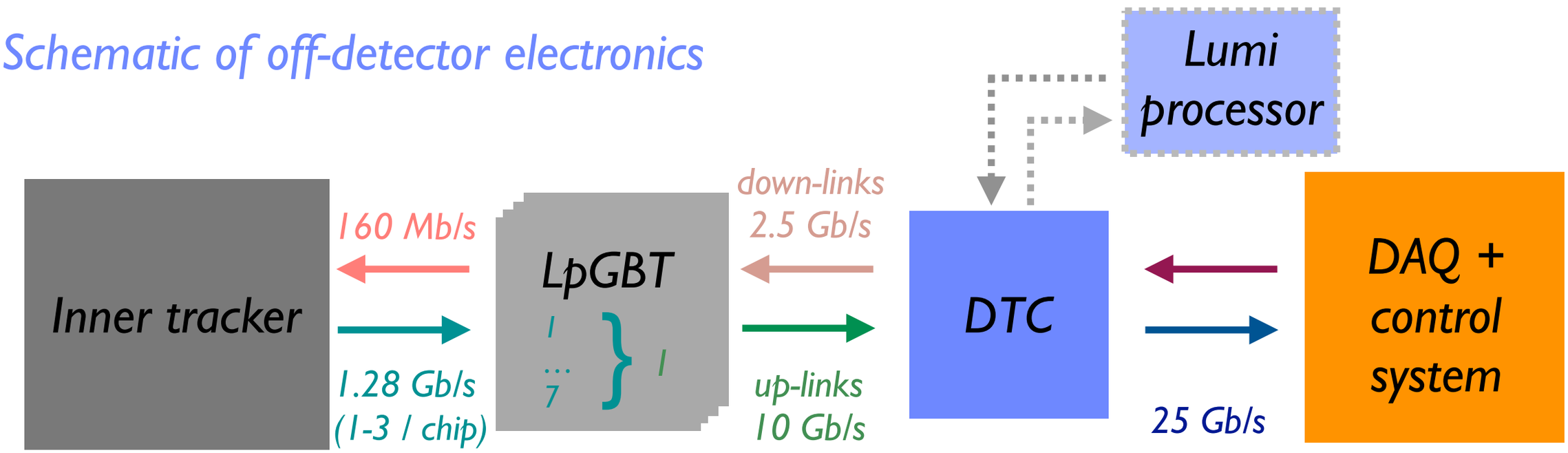
Data Trigger Control board introduction

- *Inner tracker off-detector electronics* consists of DAQ interface modules and power supplies for the on-detector electronics

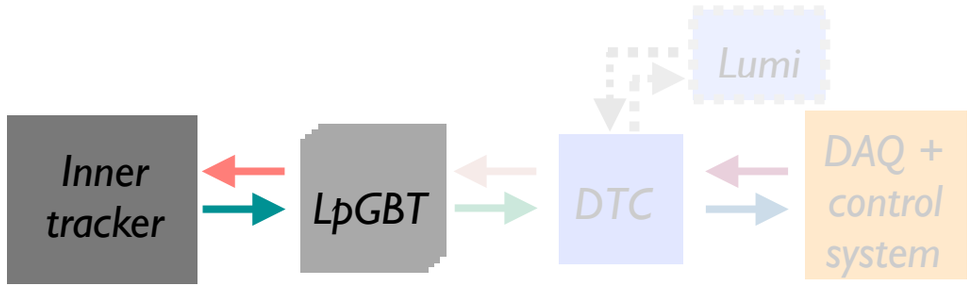
- *DAQ interface: Data Trigger Control (DTC) board*
  - only data from Level-1 triggered events are transmitted to the back-end system
  - communicates with on-detector electronics via low-power Gigabit Transceiver (LpGBT) optical links
    - *optical down-links* at 2.5 Gb/s used for clock, trigger, commands, and configuration data to the pixel modules
    - *optical up-links* at 10 Gb/s will carry readout data from L1 accept and monitoring info to the DAQ and control system

Schematic of off-detector electronics



Data compression and electrical links

- Data accepted by L1 trigger are collected by the end of column of the pixel chip
- Pixel data array are compressed by lossless algorithm within the chip
  - *up to a factor of 2 compression can be achieved (in simulation)* Y. Cheng talk



- Data are sent through differential electrical links (eLinks) at 1.28 Gb/s to LpGBT ASICs for optical transmission
- Each readout chip can transmit on 3 eLinks but actual number used depends on occupancy

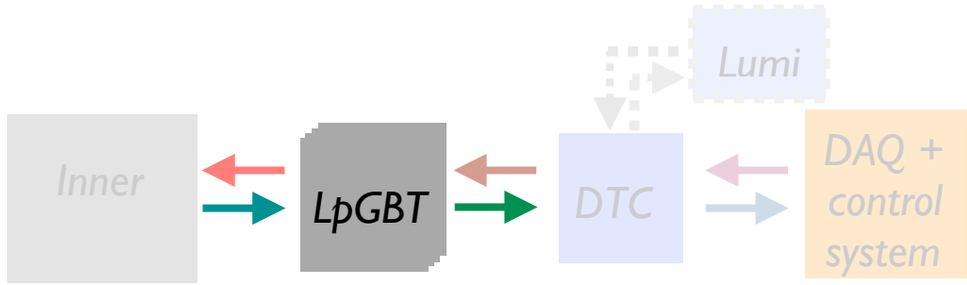
ELinks readout counting for full Pixel detector

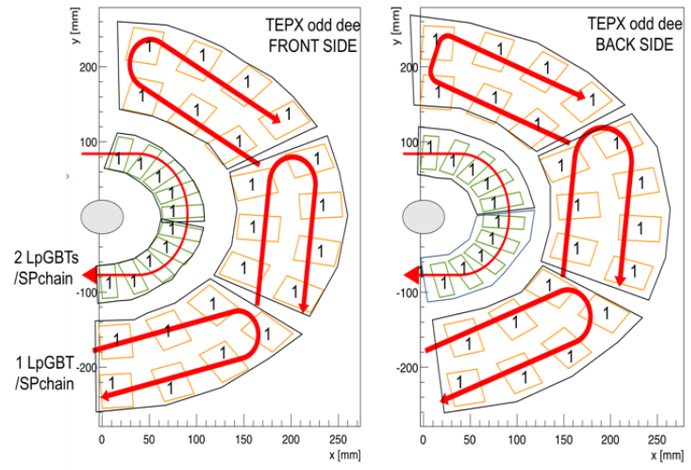
TBPX	(108 mod L1x6 eLinks) + (252 mod L2x2 eLinks) + (504 mod L3/L4x1 eLinks) = *1656 eLinks*
TFPX	(20 mod R1 x 3 eLinks) + (56 mod R2/R3 x 2 eLinks) + (32 mod R4 x 1 eLinks) = 204 eLinks / double-disk * 16 double-disks = *3264 eLinks*
TEPX	1760 mod x 1 eLinks = *1760 eLinks*

Pixel electrical and lpGBT links

- *Constraints for combining eLinks into optical links:*

  - Each LpGBT has 7 eLink inputs
  - All links from a module connects to the same LpGBT
  - Modules can connect to same LpGBT only if they belong to the same power chain





- ***Proposed*** mapping of eLinks into optical fibers from TDR

	TBPX	TFPX	TEPX	Total
E-links (readout)	1 656	3 264	1 760	6 680
E-links (control)	864	1 728	1 760	4 352
Optical links *(lpGBT links)*	332	640	288	1 260
Power chains	96	256	224	576
Front-end power [kW]	8	16	16	40

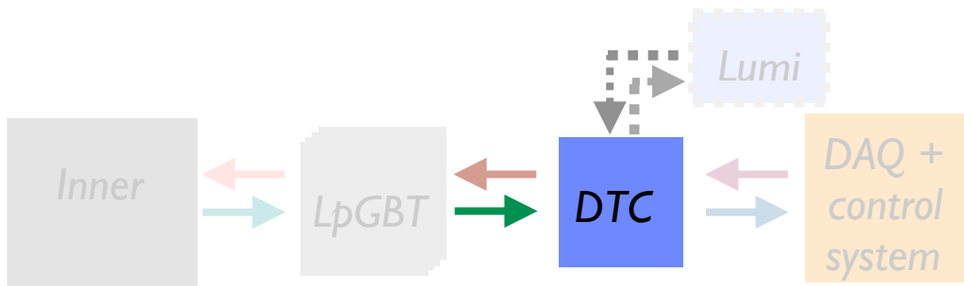
Can be changed if there are additional constraints

DTC boards count for Pixel system

Currently some mapping have been proposed based on structure and service constraints:

From DAQ TDR:

- 1/4 pixel detector can be readout with 6 DTC (1 crate)
- assumed a DAQ bandwidth / DTC of ~360 Gbs



From IT Services document:

- requirement that TEPX services are completely separated
- requirement of mixing fibers from the TBPX and TFPX to reduces effect of DTC failures

Slot #	Board description	RX #
8	DTC (TEPX 4 half-disks)	72
7	DTC (half BPIX L1 + 1 TFPX half-disk)	24 (30) + 20 = 44 (50)
6	DTC (half BPIX L2 + 1 TFPX half-disk)	28 + 20 = 48
5	DTC (half BPIX L3 + 2 TFPX half-disk)	12 + 40 = 52
4	DTC (half BPIX L4 + 2 TFPX half-disk)	16 + 40 = 56
3	DTC (2 TFPX half-disk)	40
2	DTH 1	-
1	DTH 2	-

- mapping proposal for the various subsystems in 1/4 of the Inner Tracker
- *to readout 1/4 of Inner Tracker with 6 DTC, 72 fibers RX / DTC maximum are needed*

Proposal to increase the total number of TEPX DTC from 4 to 8

Phase II inner tracker layout summary

- *DAQ interface for Inner Tracker: Data Trigger Control (DTC) board*
  - data from Level-1 triggered events are transmitted to the back-end system
  - communicates with on-detector electronics via low-power Gigabit Transceiver (LpGBT) optical links

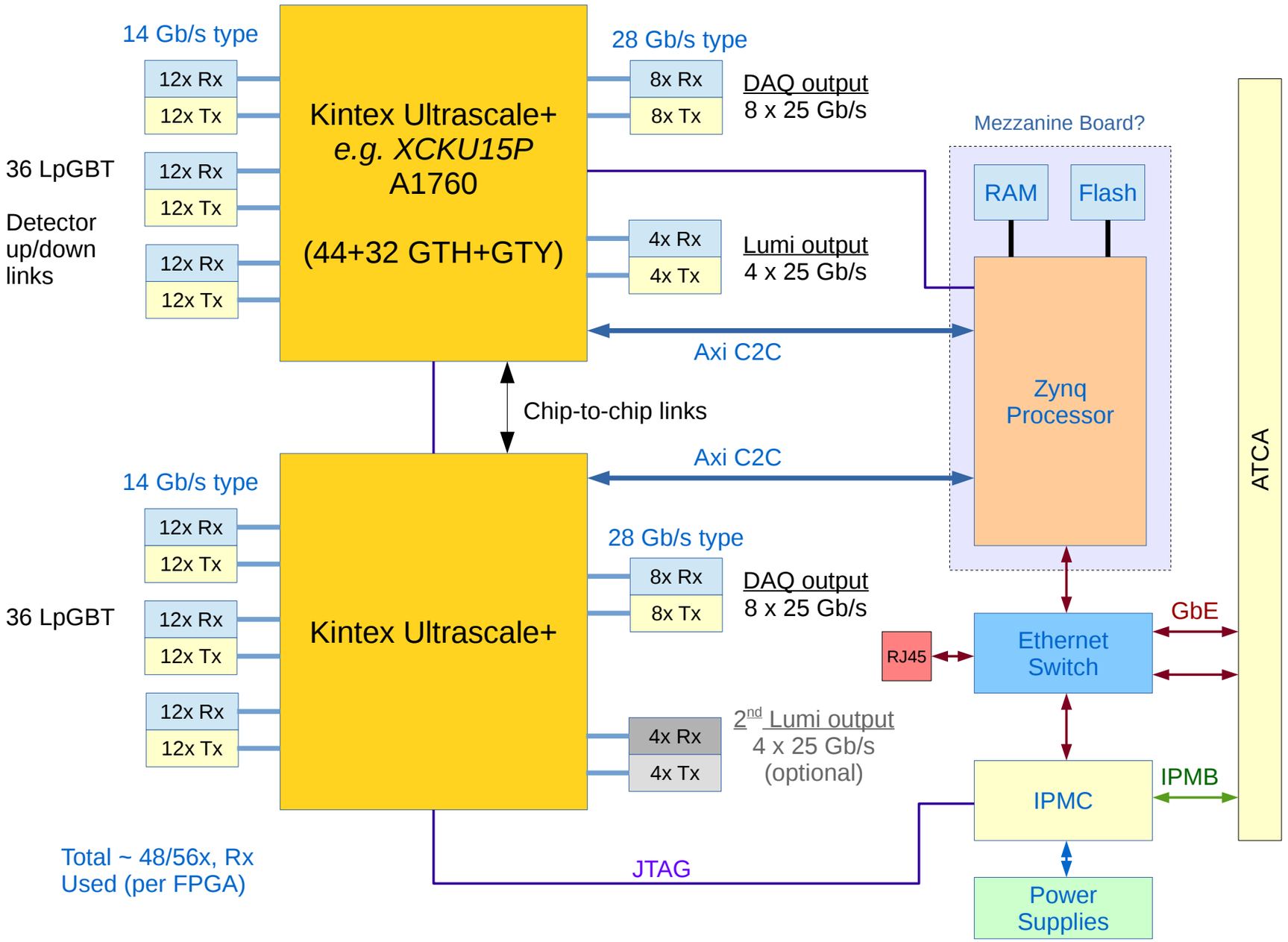
- *Inner tracker layout and fiber counting*
  - fiber mapping designs need to consider limitation coming from power chain and services of the detector
  - one of current proposal consists in 24 DTC boards to cover the entire Inner Tracker (based on 72 RO fibers / DTC)
  - final number of RO fibers per DTC needs to be decided

- *Proposal for lumi data processing* *(DTC requirements from Lumi in backup)*
  - have a separate lumi processor (perhaps a DTH board), to which the DTC would send the data over ~4x25Gb/s links

DTC: preliminary design

Pixel DTC: first conceptual design

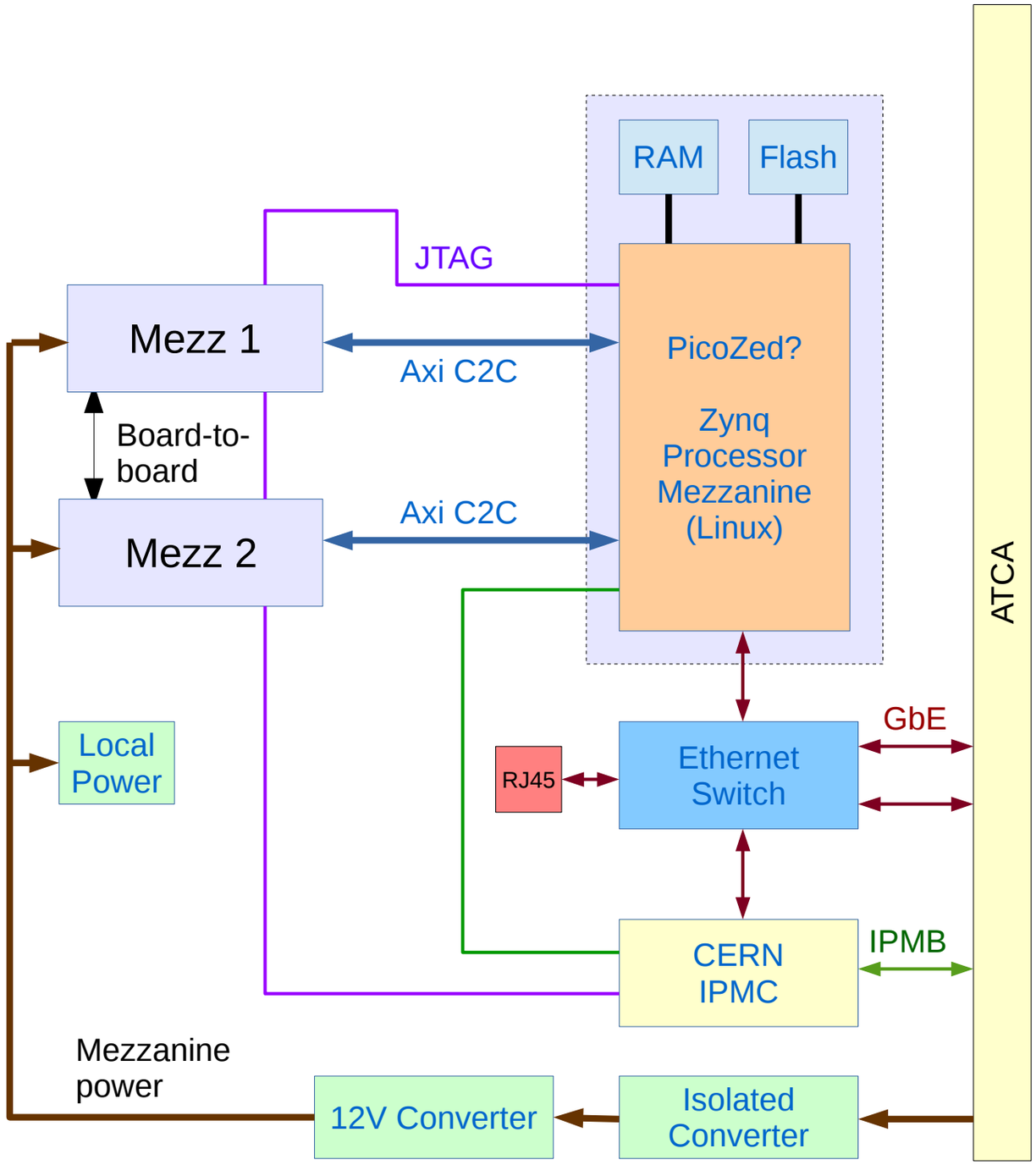
- *option with 25 Gb/s DAQ links*



- Follow OT/CMS (not identical hardware)
- Xilinx Zynq CPU
- CERN standard IPMC
- Ethernet: Front panel and ATCA
- Design decisions:
  - Unified blade or carrier/mezzanine?
  - What FPGA/family?

Pixel DTC: new conceptual design

- *Proposed carrier block diagram: option with 25 Gb/s DAQ links*



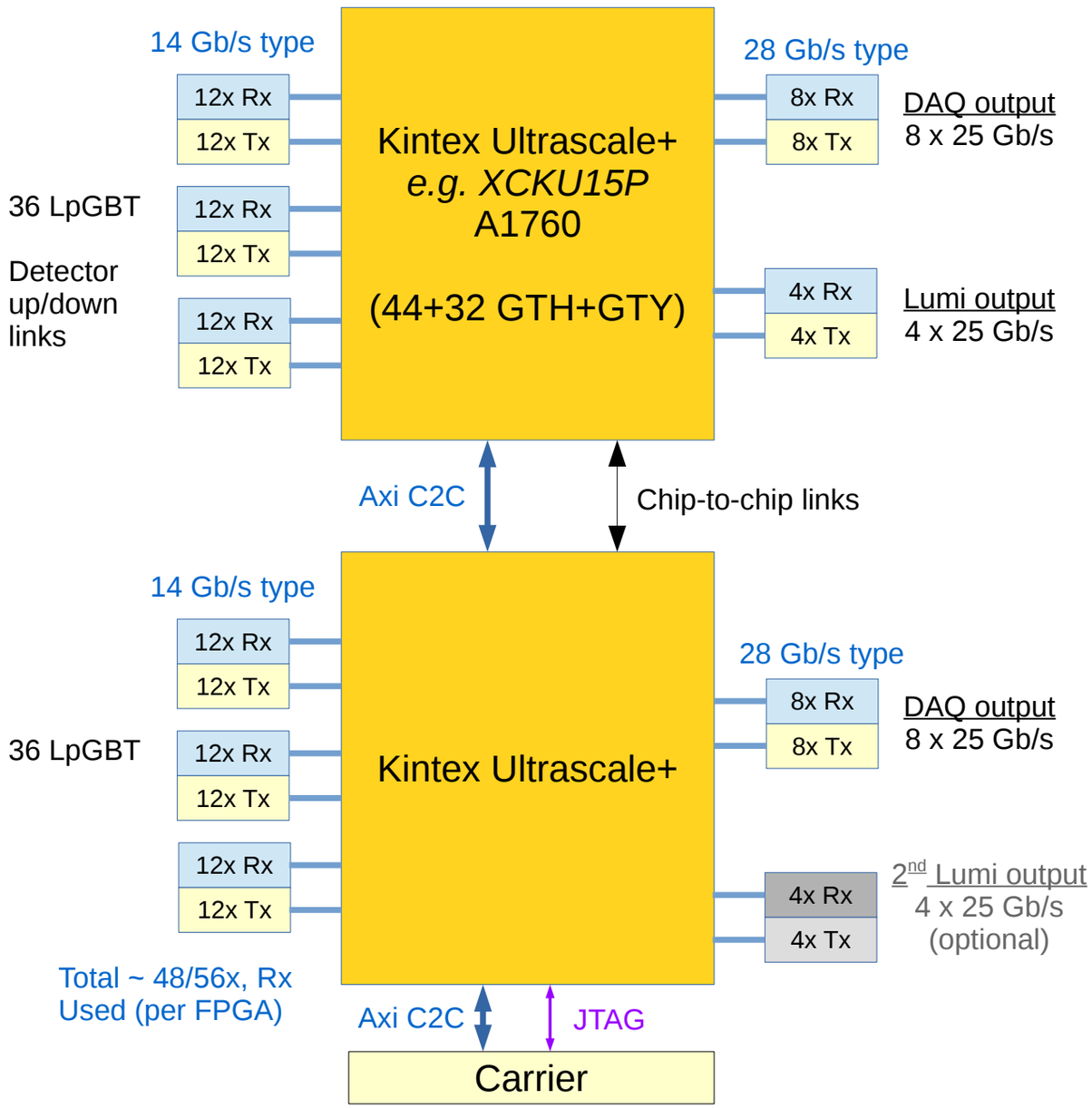
Preliminary plan:

simple/universal carrier blade design not tied to any particular FPGA/family

- Accommodates 2 smaller mezzanines or one large one
- Supplies JTAG, AXI chip-to-chip and 12V power
- Uses CERN IPMC, off-the-shelf Zynq board to save engineering

Pixel DTC: new conceptual design

- *Proposed mezzanine card: option with 25 Gb/s DAQ links*



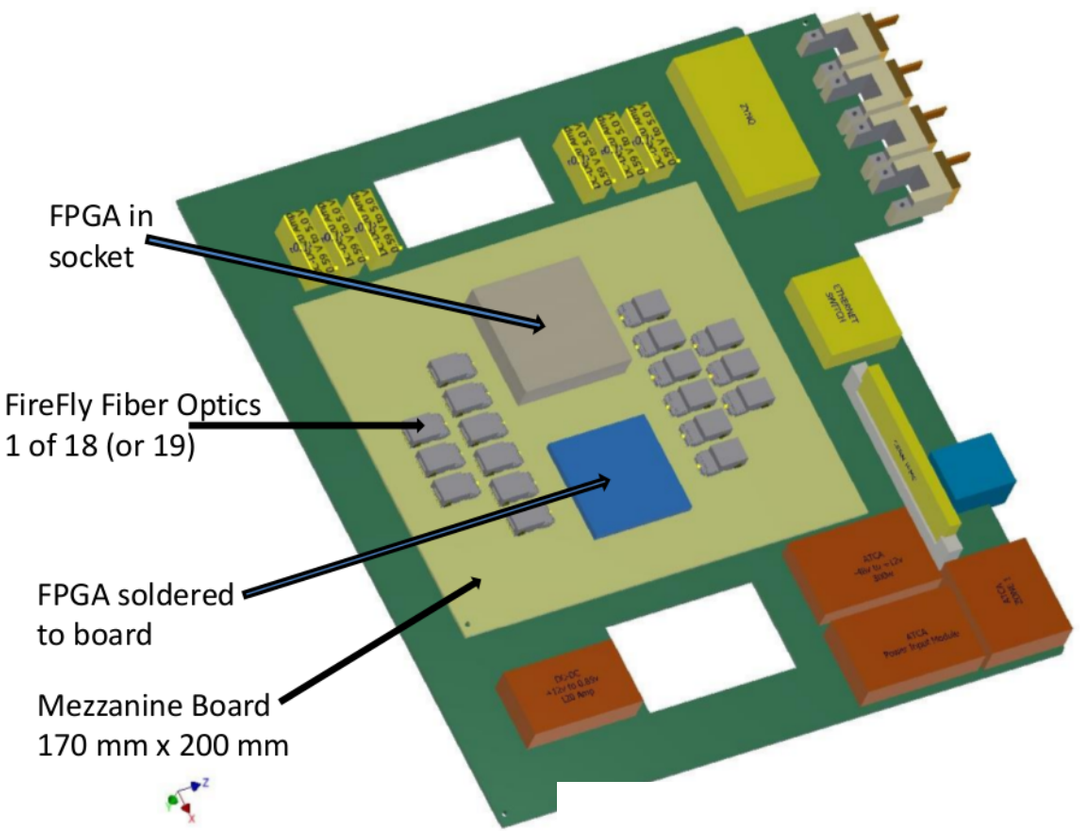
Preliminary plan:

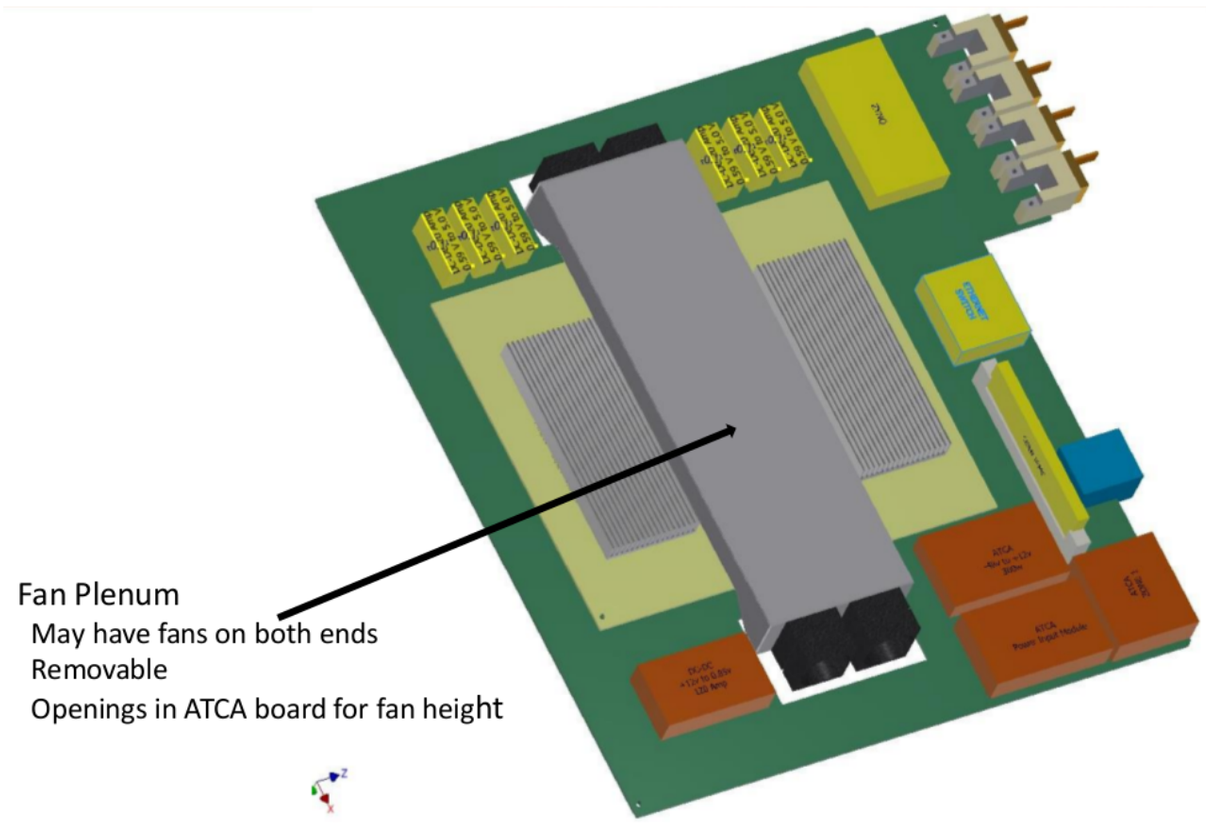
incorporate voltage regulators on mezzanine card allowing standalone tests

- FPGAs, Optics, Power on mezzanine
- Test connectors for operation sans blade

Pixel DTC: new conceptual design

- *Proposed mezzanine card: option with 25 Gb/s DAQ links*
  - *foreseen cooling scheme for FPGA and fiber optics*





Pixel DTC: development plans

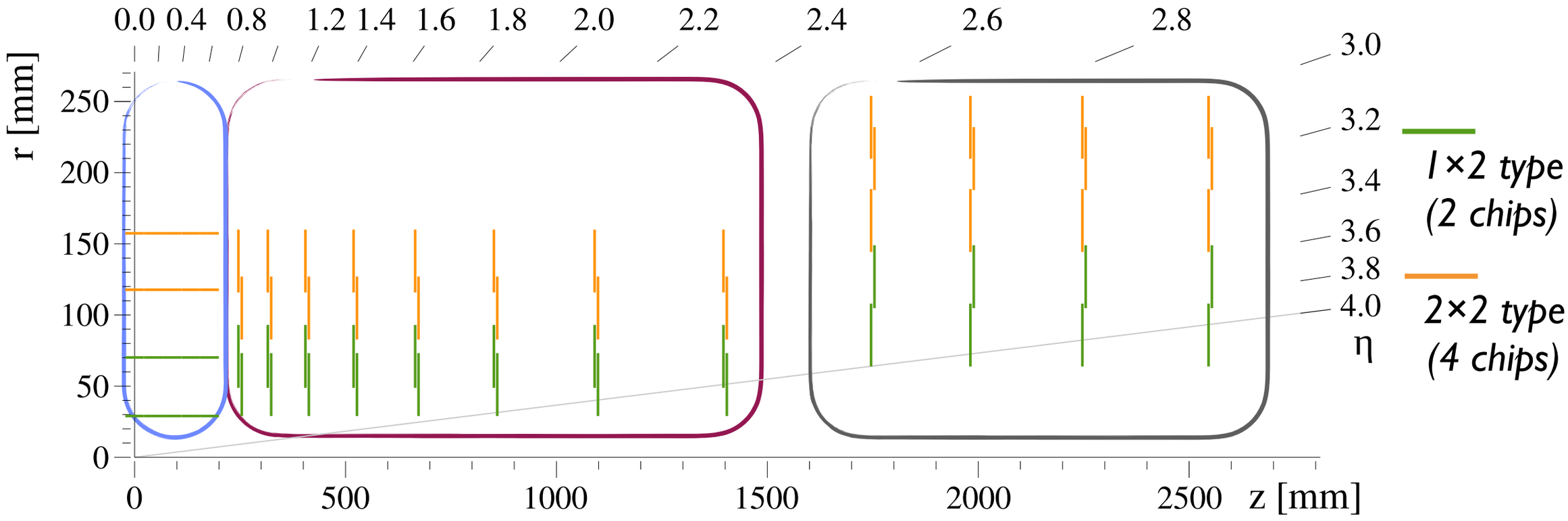
- ***Preliminary eLinks and lpGBT links calculation for DTC counting***
  - constraints from power chain and services in connecting modules to DTC for RO
  - *assumed a data compression up to a factor of 2*

- ***DTC considerations from Lumi***
  - maintain close contacts with Lumi group to understand better the DTC needs for lumi measurements
  - DTC could send data to lumi processor over 4x25 Gb/s (or 10x10Gb/s) links

- ***Next steps***
  - define DTC specifications in the next months *(collaboration with Cornell)*
    - *prototype to be manufactured early 2019*
  - discussions ongoing with DAQ, FE groups to take into account all needs for board design

Backup

Pixel layout from TDR



TBPX

Layer	modules
1	108
2	252
3	216
4	288
tot	*864*

TFPX

Disk	modules
1	108
2	108
3	108
4	108
5	108
6	108
7	108
8	108
tot	*1728*

TEPX

Disk	modules
1	220
2	220
3	220
4	220
tot	*1760*

Pixel layout from TDR: parameters

TBPX								
Layer	1	2	3	4				
Average radius [mm]	29.0	70.1	117.8	157.4				
z coverage [mm]	$\pm$199.7	$\pm$199.7	$\pm$199.7	$\pm$199.7				
N_{ladders}	12	28	24	32	**Total: 96**			
N_{modules}	108	252	216	288	**Total: 864**			
TFPX (one side)								
Double-disc	1	2	3	4	5	6	7	8
Average z position [mm]	250.0	319.8	409.0	523.1	669.1	855.8	1094.6	1400.0
N_{rings}	4	4	4	4	4	4	4	4
N_{modules}	108	108	108	108	108	108	108	108 **Total: 864**
Per TFPX double-disc								
Ring	1	2	3	4				
Inner radius [mm]	30.1	49.5	84.4	117.0				
Outer radius [mm]	73.2	93.0	127.0	160.0				
N_{modules}	20	32	24	32	**Total: 108**			
TEPX (one side)								
Double-disc	1	2	3	4				
Average z position	1750.0	1985.4	2250.8	2550.0				
N_{rings}	5	5	5	5				
N_{modules}	220	220	220	220	**Total: 880**			
Per TEPX double-disc								
Ring	1	2	3	4	5			
Inner radius [mm]	64.3	105.1	145.2	188.5	210.4			
Outer radius [mm]	108.0	149.0	188.5	232.0	254.0			
N_{modules}	40	56	36	40	48	**Total: 220**		

Pixel rates after compression and eLinks

From S. Orfanelli based on rates from Y. Cheng

TBPX

Delta_Column (PU200)	Bits per chip per event	Mbps per chip (750kHz)
	Mean	Rate
BARREL		
BPIXL1 (PR2x2)	3173.6	2380.2
BPIXL1 (PR1x4)	2910.85	2183.1375
BPIXL1 (PR4x1)	3529.39	2647.0425
BPIXL2	695.036	521.277
BPIXL3	308.774	231.5805
BPIXL4	202.568	151.926

BARREL	1.28 Gbps Links per chip	Chips/ Module	Links per module	Max Readout rate per module	Max Readout rate per chip	Occupancy
BPIXL1 (PR2x2)	3	2	6	7680	3840	62%
BPIXL1 (PR1x4)	3	2	6	7680	3840	57%
BPIXL1 (PR4x1)	3	2	6	7680	3840	69%
BPIXL2	1	2	2	2560	1280	41%
BPIXL3	1	4	1	1280	320	72%
BPIXL4	1	4	1	1280	320	47%

TFPX

Delta_Column (PU200)	Bits per chip per event	Mbps per chip(750kHz)
	Mean	Rate
FORWARD		
FPIXD1R1_lowCol	901.184	675.888
FPIXD1R2_lowCol	543.93	407.9475
FPIXD1R3_lowCol	309.292	231.969
FPIXD1R4_lowCol	205.549	154.16175

FORWARD	1.28 Gbps Links per chip	Chips/ Module	Links per module	Max Readout rate per module	Max Readout rate per chip	Avg Occupancy
FPIXD1R1	1(out)/ 2(inner)	2	3	2560	1280	55%
FPIXD1R2	1	2	2	1280	640	43%
FPIXD1R3	0.5	4	2	1280	320	43%
FPIXD1R4	0.25	4	1	1280	320	55%

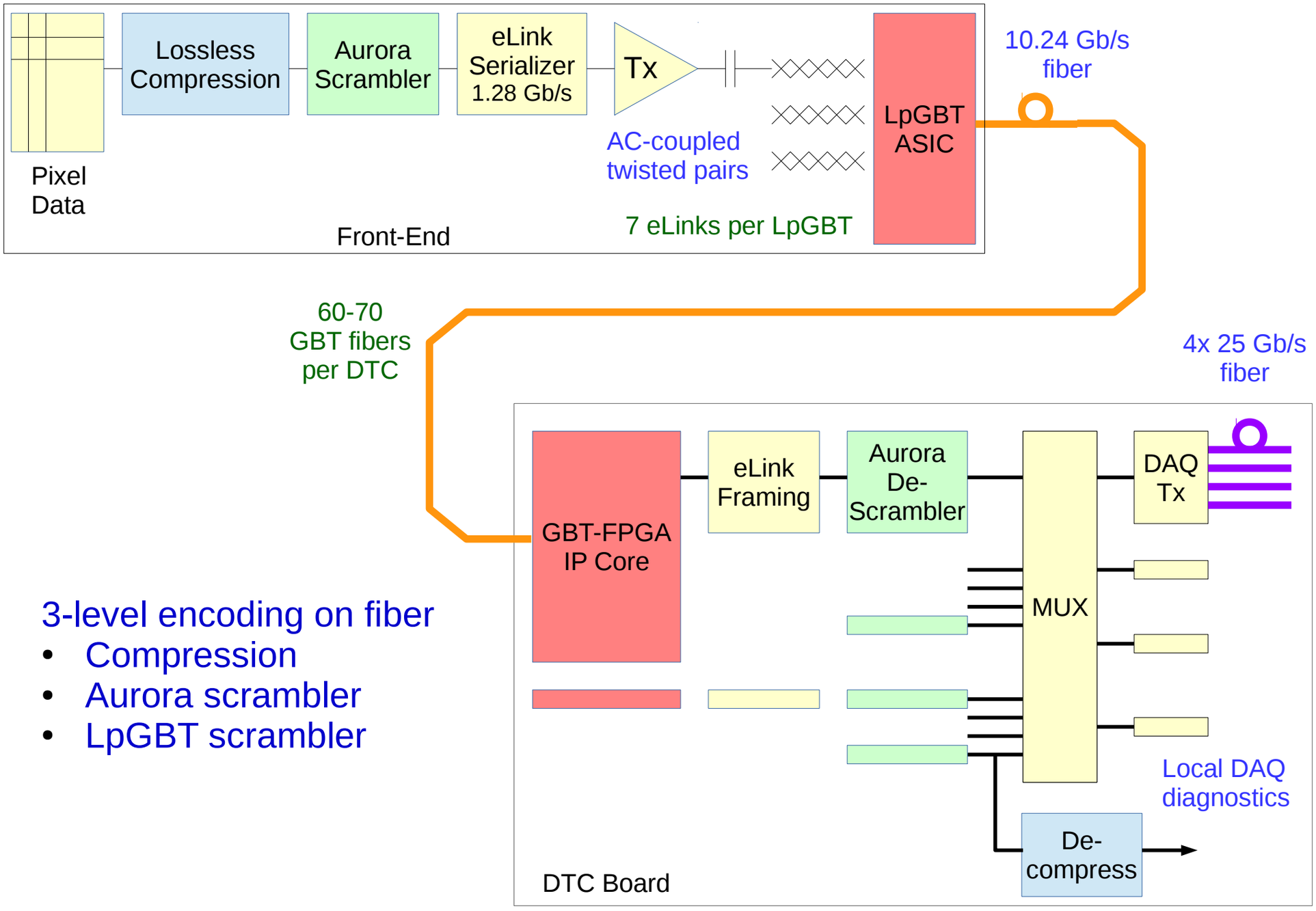
TEPX

Delta_Column (PU200)	Bits per chip per event	Mbps per chip(750kHz)
	Mean	Rate
EXTENSION		
FPIXD8R1_lowCol	463.59	347.6925
FPIXD8R2_lowCol	274.883	206.16225
FPIXD8R3_lowCol	222.738	167.0535
FPIXD8R4_lowCol	161.522	121.1415
FPIXD8R5_highCol	158.583	118.93725

EXTENSION	1.28 Gbps Links per chip	Chips/ Module	Links per module	Max Readout rate per module	Max Readout rate per chip	Occupancy
FPIXD8R1	0.5	2	1	1280	640	69%
FPIXD8R2	0.5	2	1	1280	640	37%
FPIXD8R3	0.25	4	1	1280	320	54%
FPIXD8R4	0.25	4	1	1280	320	40%
FPIXD8R5	0.25	4	1	1280	320	35%

Pixel readout encoding

- ***Pixel Readout: Logic chain showing encoding***



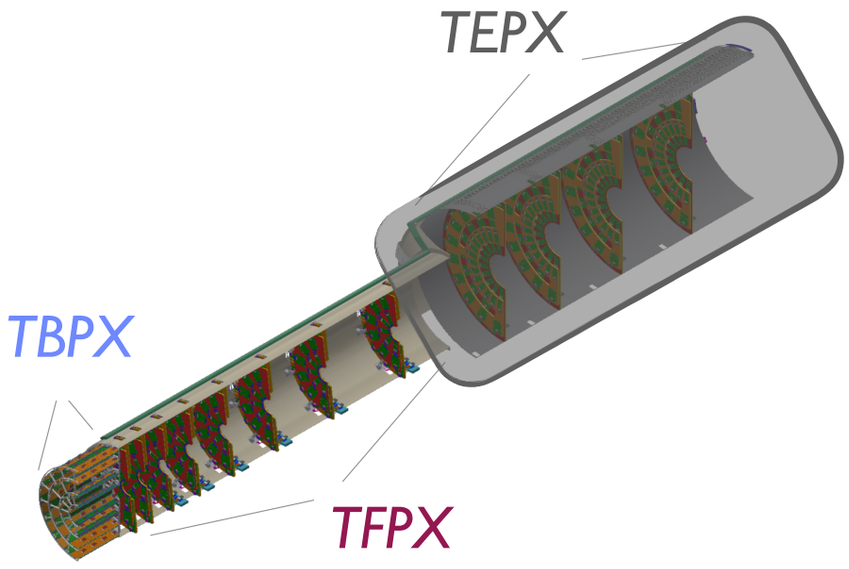
3-level encoding on fiber
- Compression
- Aurora scrambler
- LpGBT scrambler

The DTC understanding of Lumi

The DTC understanding of Lumi

Phase II: 3 luminosity measurement systems considered

- Calorimetric-type
- Minimum Ionizing Particle counting
- ***Low occupancy pixel based measurement*** using the data collected from TEPX



General plan

- *Have a separate lumi processor board, to which the DTC would send the data over ~4x 25Gb/s links*
  - *eg. lumi board could be a mezzanine card or a board on DTH*

The DTC understanding of Lumi

- ***Lumi measurement***

  - lumi measurements consists in *counting number of hits per unit of time* and fill in an histogram with this information / BX / geometric region
  - *must run whenever there is beam in the machine*, independent of state of global DAQ (TCDS must be running as lumi-nibble counter updates are sent)
  - data loss due to e.g. slow control intervention should be known by back-end board and passed on to lumi (orbit by orbit, pref.)
  - might need info of previous and later BXs
  - may want disk-to-disk coincidences where there is overlap
    - *coincidence could be done among front and back half disks*
  - back-pressure from DAQ should not affect lumi board

The DTC understanding of Lumi

- ***Lumi trigger***
  - process events marked with ~75kHz lumi triggers separately from main DAQ stream and pass to lumi DAQ. Bandwidth would be ~10% of 360Gb/s or 36Gb/s
  - during “unstable beams” no L1 triggers only lumi triggers
    - lumi trigger rate may be >> 75kHz but bandwidth similar to beam operation
    - bandwidth similar to beam operation employing only outer TEPX disks

- ***Compression***
  - compression performed on pixel chip using arbitrary regions that are not mapped to real clusters
  - data must be de-compressed and re-clustered for luminosity measurements
    - *the DTCs will send the compressed data to the lumi board (to limit bandwidth)*
    - *decompression will still be performed on the DTC (maybe only on a subset of events) for monitoring reasons*