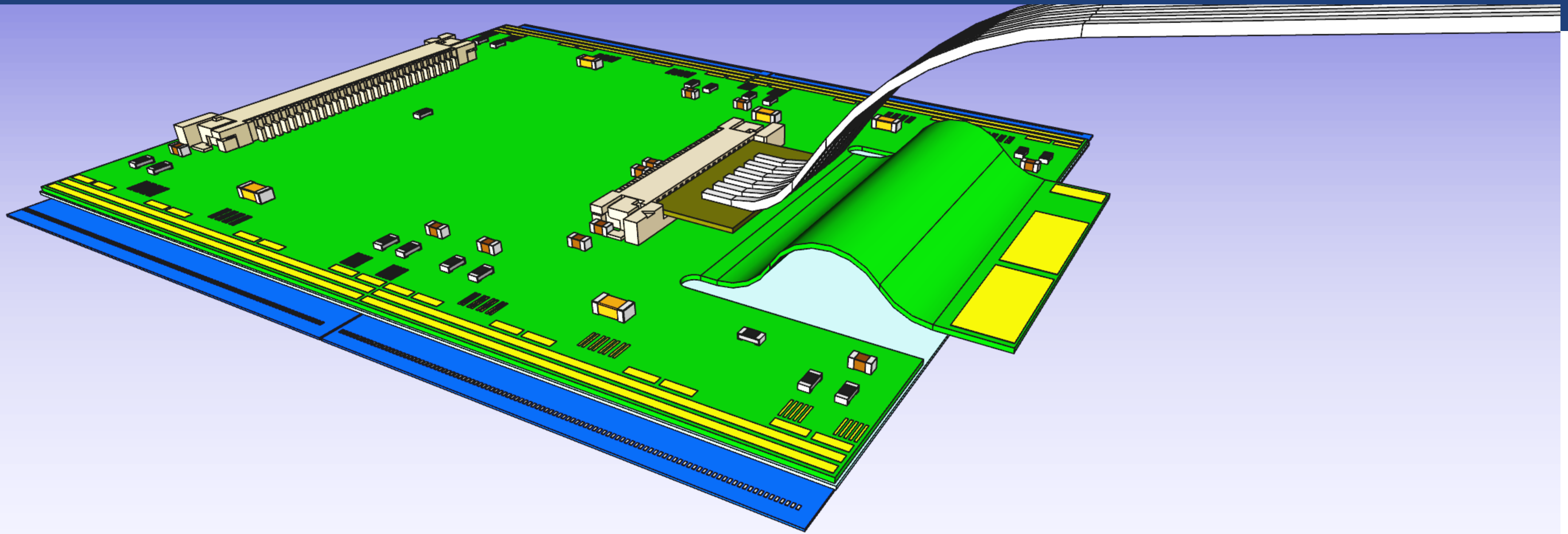
ETH zürich



Serial Powering in CMS pixel and at ETH

Malte Backhaus

(with a lot of material from S. Orfanellis talk at ACES 2018)

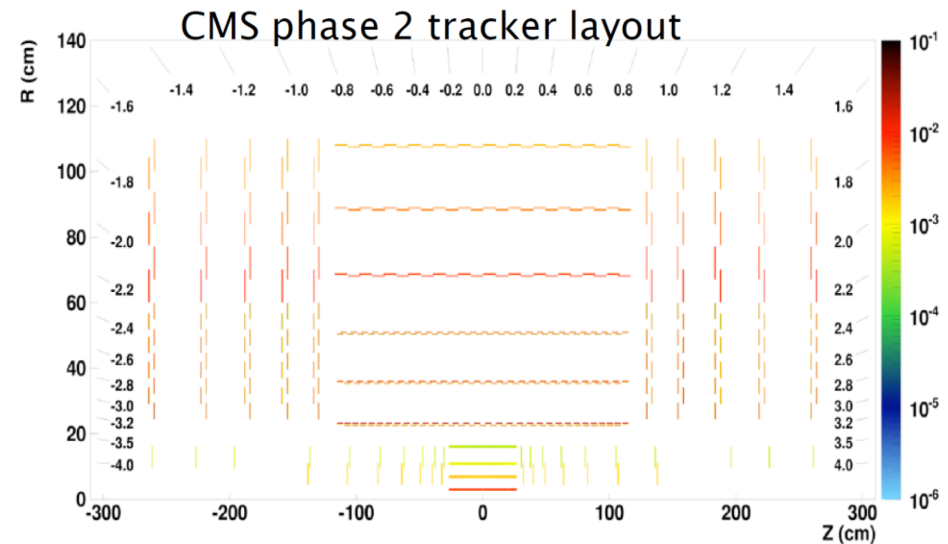
IPA

Outline

- Motivation for serial powering
- Constraints due to serial powering
- R&D status
- Further plans at ETH

Major challenges - Powering

- Larger detector ($2m^2$ → $4m^2$), smaller pixels ($50x50um^2$)
  → 800 million pixels
- 10x higher hit rate, 4-6x increase in latency, 10x trigger rate, 100x readout data rate (barrel inner layer), 10x radiation level (SEU, TID)
  → At least **one order of magnitude** increase in requirements
  → Digital speed and logic density increase
  (“challenging” with custom radiation hard libraries, large feature size)
  → Fast analog chain
- Lower feature size technology (**65nm**, 110nm) needed
  → Lower supply voltage,
  but **increase of supply current**
- **1-4x power density** in comparison with current pixel detector
- Challenging even for unrealistic case of similar power density:
  5-10x higher current (65nm)
  → **25-100x power loss** in “similar” cables



Power consumption estimation

- Lower feature size:
  → ~1V supply voltage
  → Increase in supply current, even for (unrealistic) similar power density compared to Phase-I ROCs

[Estimation by J. Christiansen]

Pixel chip power: 2cm x 2cm	Conservative	Optimistic
Analog power supply	1.2v	
Pixel analog current (50x50um²)	6uA per pixel	4uA per pixel
Pixel analog current (100x100um²)	10uA per pixel	6uA per pixel
Digital power supply	0.8 (1.0) v	
Digital power density, low rate	0.2W/cm²	0.1W/cm²
Digital power density, medium rate	0.25W/cm²	0.12W/cm²
Digital power density, high rate	0.5W/cm²	0.25W/cm²
High rate pixel chip (50x50):		
Analog (1.2v) current per chip	0.96A	0.64A
Digital (0.8v) current per chip	2.50A	1.25A
Total chip power (high rate 50x50)	**3.15W**	**1.77W**
Medium rate pixel chip (50x50):		
Analog (1.2v) current per chip	0.96A	0.64A
Digital (0.8v) current per chip	1.25A	0.60A
Total chip power (med rate 50x50)	2.15W	1.25W
Low rate pixel chip (100x100):		
Analog (1.2v) current per chip	0.40A	0.24A
Digital (0.8v) current per chip	1.00A	0.50A
Total chip power (low rate 100x100)	**1.28W**	**0.69W**

- Power consumption of full detector:
  16kW (9kW) → **16kA** (9kA) to be delivered to the modules

- A simple calculation of cable weight:

  Local services:
  $V_{drop} \leq 0.2V$, 2m (1m), Al → **48kg** (12kg)

  Global services:
  $V_{drop} \leq 1.0V$, 50m → **6100kg**
  → **66% power loss in cables**

Power Options

Direct parallel powering

- Power loss 66% in cables → excluded

One-stage on-chip DC/DC

- Interesting option, but only efficient enough if conversion factor g is about 6-10 (power loss ~1/g). Current on-chip converters allow only factor 2-4 (still very challenging, see FE-I4)
  → ATLAS decided for Serial Powering

One-stage external DC/DC

- No gain in local power cables and material budget of active volume. External converters mass needs to be included in the global cable mass calculation → excluded

Two-stage DC/DC

- Very interesting option, more studies needed. No experience with this option available. Cable mass reduction ~2.2, reducing to only ~1.5 if external DC/DC converters mass counted

Serial Powering

- Cable mass (or power loss) reduced by $1/n^2$ compared to direct powering, with n the number of readout chips powered in parallel. Very interesting options with implications on system level
  → see next slides

External DC/DC and Serial Powering

- Very complicated, combining drawbacks → excluded

Benefit of a Serial Powered System

The power efficiency of the full detector system needs to be increased. Calculate the power efficiency for a parallel and serially powered detector system.

Parallel powered system:

$$I_{par} = nI_0, \qquad U_{par} = U_0 + R_{cable} \cdot I_{par}$$

Module power consumption:

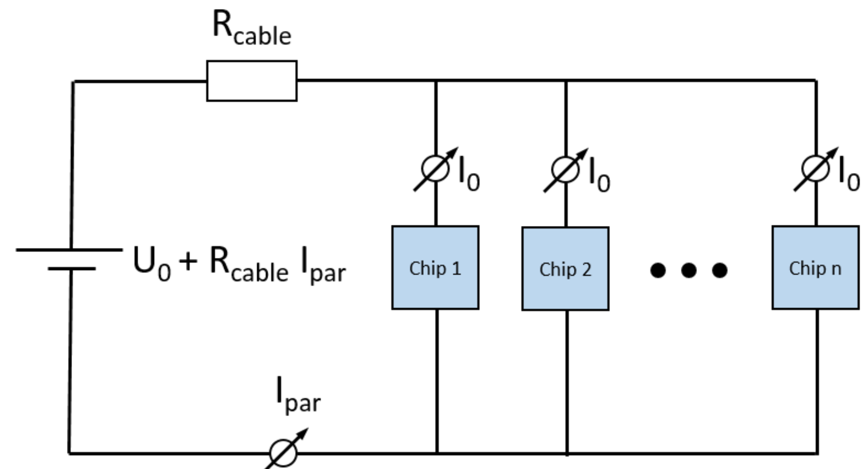
$$P_{par}^{mod} = U_0 \cdot nI_0$$

Power loss in cables:

$$P_{par}^{cable} = U_{drop} \cdot I_{par} = R_{cable} \cdot n^2 I_0^2$$

Power efficiency:

$$\epsilon = \frac{P_{par}^{mod}}{P_{par}^{mod} + P_{par}^{cable}} = \frac{U_0 \cdot nI_0}{U_0 \cdot nI_0 + R_{cable} \cdot n^2 I_0^2} = \frac{U_0}{U_0 + R_{cable} \cdot nI_0}$$



Benefit of a Serial Powered System

The power efficiency of the full detector system needs to be increased. Calculate the power efficiency for a parallel and serially powered detector system.

Serially powered system:

$$I_{ser} = I_0, \qquad U_{ser} = nU_0 + R_{cable} \cdot I_0$$

Module power consumption:

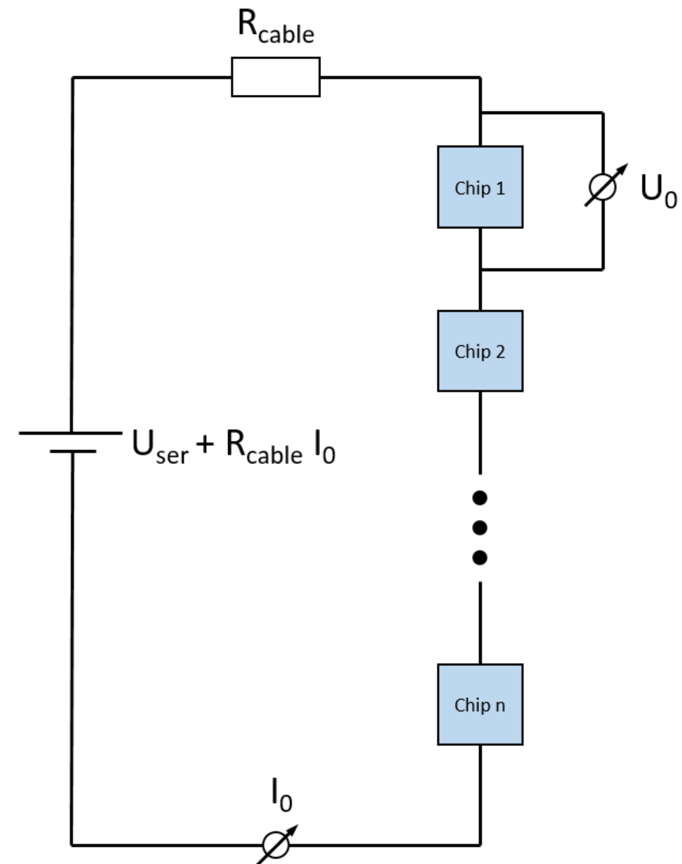
$$P_{ser}^{mod} = nU_0 \cdot I_0$$

Power loss in cables:

$$P_{ser}^{cable} = U_{drop} \cdot I_{ser} = R_{cable} \cdot I_0^2$$

Power efficiency:

$$\epsilon = \frac{P_{ser}^{mod}}{P_{ser}^{mod} + P_{ser}^{cable}} = \frac{nU_0 \cdot I_0}{nU_0 \cdot I_0 + R_{cable} \cdot I_0^2} = \frac{U_0}{U_0 + R_{cable} \cdot \frac{1}{n} I_0}$$



Implications

- As soon as voltage drop in supply cables becomes significantly larger than supply voltage of the ROCs (usually the case), a **serially powered system** has a **gain of $1/n^2$ in power efficiency**

- A serially powered system has a **constant current** consumption
→ **No** voltage **transients** in case of current loss
(letal for ROCs, limiting possible voltage drop in cables)
→ **Cable cross section** can be "freely" chosen within margin of heat dissipation and power supply output voltage
→ Trade-off power efficiency vs. system design constraints (dominated by voltage transient protection in parallel powered system)

- There is a **price to pay** for these benefits:
→ The system is more **complex** on stave/secor level or on module level (see next slides)

Needs to enable a serially powered system

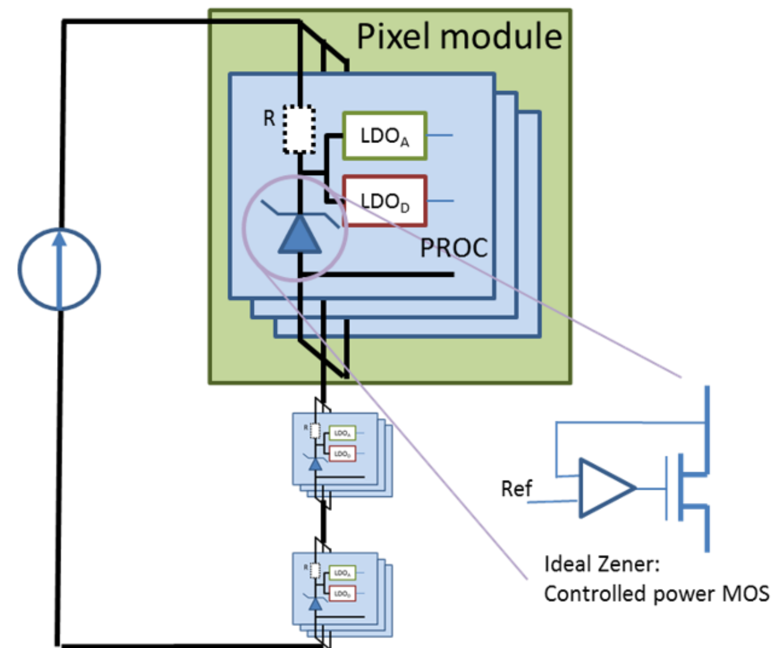
Only an on-chip converter of the **constant supply current** into a constant voltage is needed

- Stable output voltage and current consumption independent of the dynamic current consumption of the ROC itself (load current).

Typical solution:

- Normal LDO (as used for voltage regulation)
  +
  voltage clamp (zener diode) to translate the supply current into the input voltage of the LDO

- **Supply current splitting** needs to be well defined in our application (parallel chips, parallel LDOs for digital/analog)
  → change voltage clamp by "something resistive"



Needs to enable a serially powered system

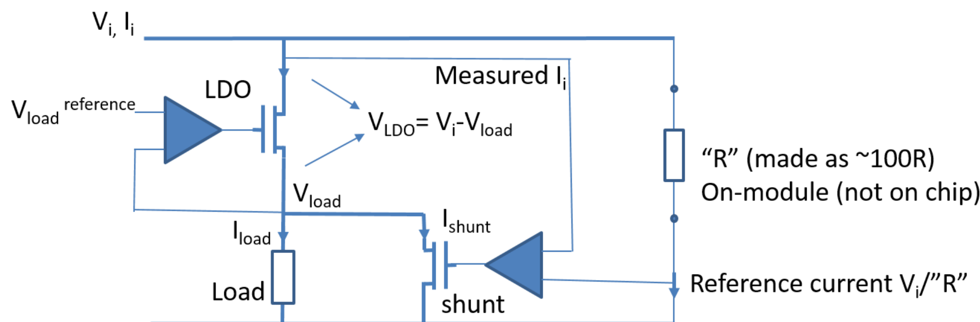
Only an on-chip converter of the **constant supply current** into a constant voltage is needed

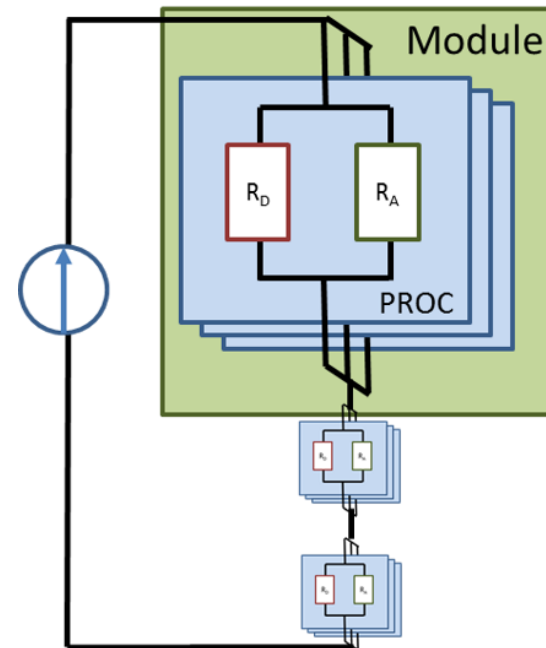
- Stable output voltage and current consumption independent of the dynamic current consumption of the ROC itself (load current).

Resistive Shunt-LDO [M. Karagounis]:

- Resistive behavior if “on”
- LDO adjusts V_{drop} in transistor if $V_{load} \neq V_{ref}$
- Shunt circuitry compares I_{in} to I_{ref} and adjusts I_{shunt} to achieve a stable $I_{in} = I_{load} + I_{shunt}$

→ I_{in} constant and $I_{in} \geq I_{load}$ max.





IPA

Needs to enable a serially powered system

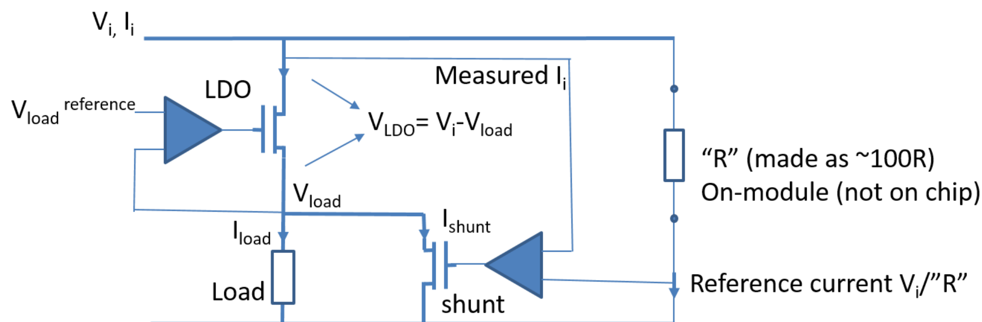
In case of load current loss the full power needs to be consumed in the shunt transistor
→ localized heat dissipation

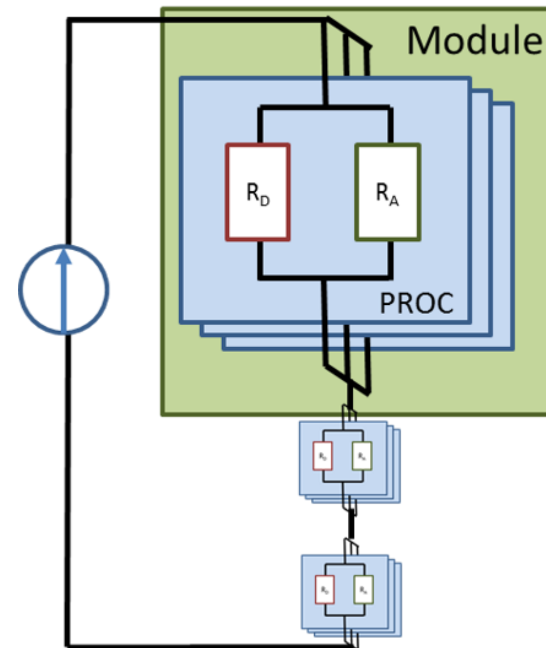
In case of parallel chips and chip failures
→ other chips need to “burn” the power of failing chips to avoid loss of full chain

Resistive Shunt-LDO [M. Karagounis]:

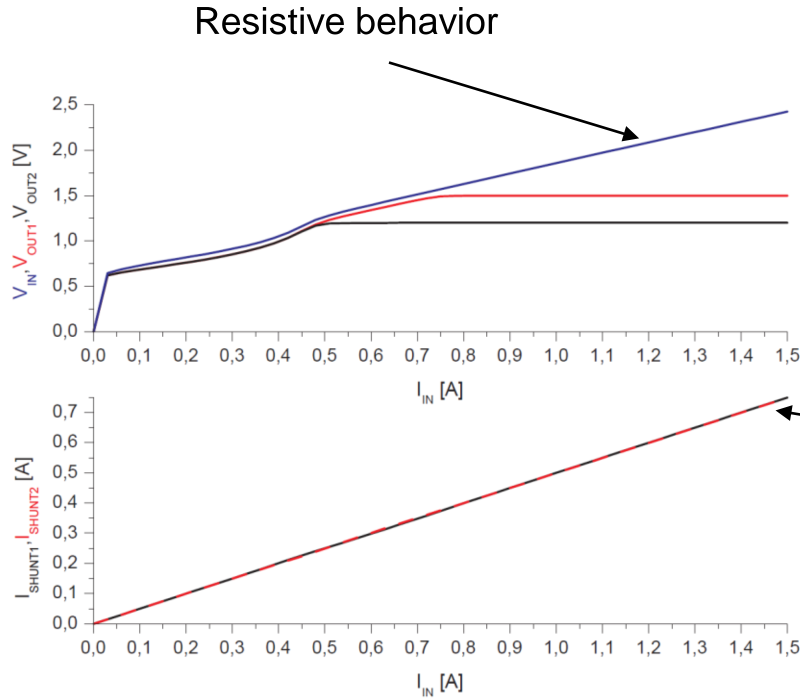
- Resistive behavior if “on”
- LDO adjusts V_{drop} in transistor if $V_{load} \neq V_{ref}$
- Shunt circuitry compares I_{in} to I_{ref} and adjusts Ishunt to achieve a stable $I_{in} = I_{load} + I_{shunt}$

→ I_{in} constant and $I_{in} \geq I_{load}$ max.

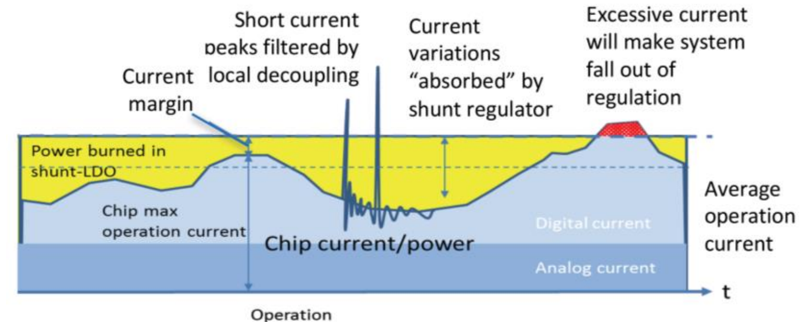




Needs to enable a serially powered system

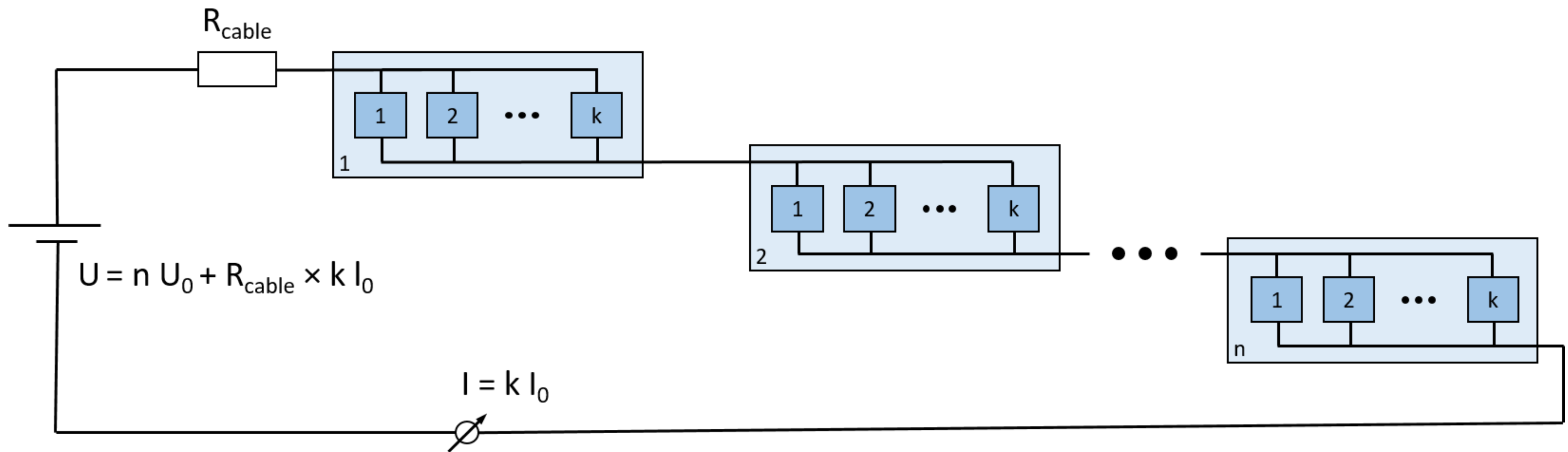


Supply the system with a **constant current** instead of a constant voltage!



IPA

Serial powering concepts: Chains of serially powered modules



Benefits

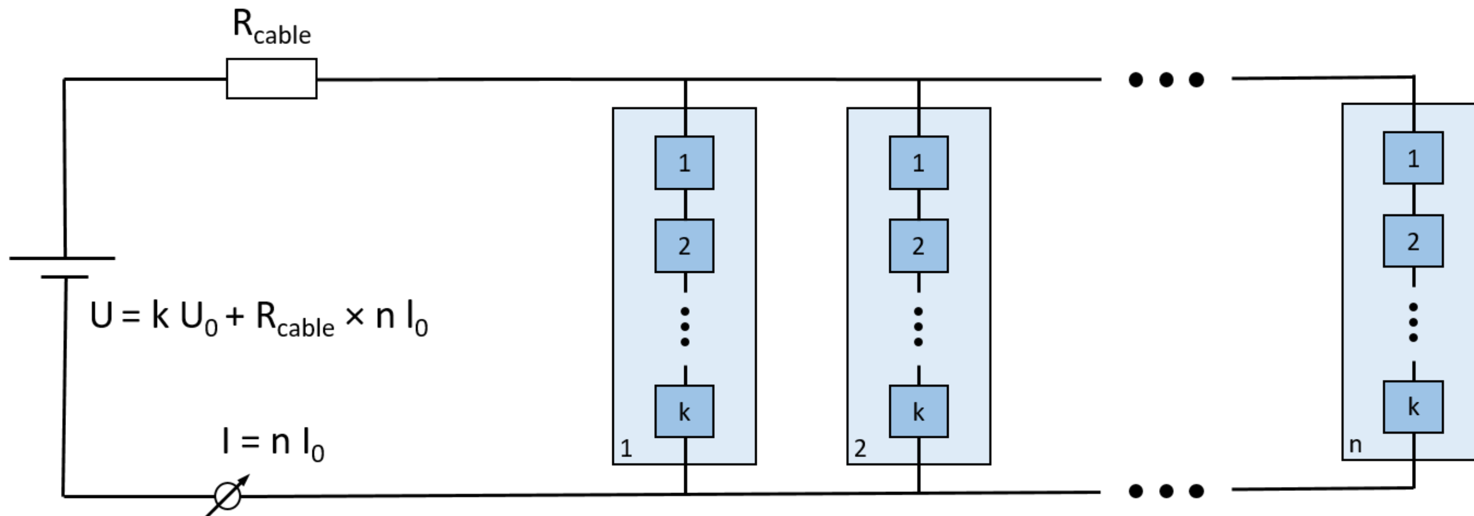
- "Free" choice of gain factor n (number of serial modules)
  → Very high gain in power efficiency possible

Drawbacks

- Chips on modules need to have high safety margin to dissipate power in case of chip failure
- Single module failure results in loss of the full chain
  → Bypass functionality needed
- Control granularity is the full chain unless bypass functionality is configurable (needs to be highly SEU tolerant!)
- Modules on different potential
  → complex high voltage connection
  → AC coupled data transmission mandatory

→ High gain factor, but very complex/fragile system

Serial powering concepts: On-module serial powering



Drawbacks

- Gain factor limited due to module size
- Loss of chip → loss of module, unless on-module protection implemented
- Chips on module on different potential
  → AC coupled data transmission on module
  → Sensor choice limited? AC coupled sensor needed? We started a study with Daniele…

Benefits

- Full granularity (module level) could be conserved
- No loss of full chain in case of module failure
- No AC-coupled data transmission to opto-conversion needed

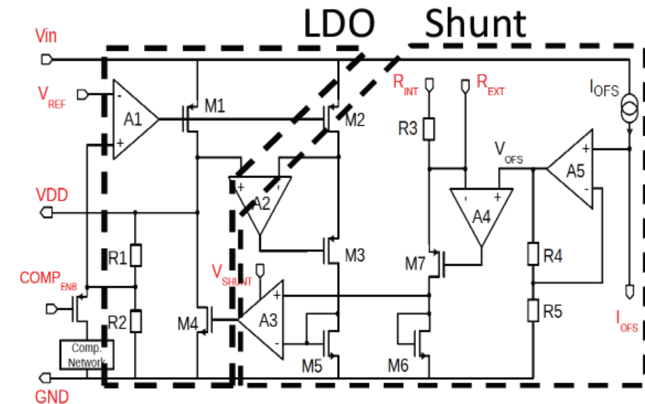
→ Limited gain factor, but significantly less complex/fragile system

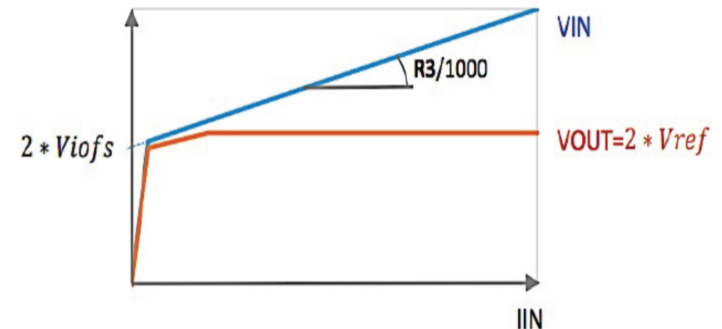
System level constraints

- Modules **not** connected to power individually
  → need a „module to module“ current routing
  → especially challenging in barrel in combination with „ladder mechanics“ (no access to ladder backside)
  → separation of data and power cables
- All modules on different potential
  → no GND!
  → modules on different potential
    → AC-coupled data transmission → DC balanced data formats
    → sensor bias voltage position dependent (with single HV line per chain)
      → need sensors with large overdepletion before irradiation
- Localized heat generation in shunt transistors
- Module power consumption **increase** in failure modes (see later slides)
  → thermo-mechanical interface design for failure modes needed
  → SLDO design failure mode compatible

RD53A SLDO regulator [M. Karagounis]

- **65 nm for Iin= 2A, Vin =2A** (FE-I4 version was 0.5A).
- **Configurable Resistive behavior** allows for well-defined current sharing, determined by their effective resistance.
- **Configurable Offset voltage**, allows for an optimization of the power consumption.
- Improved control loop to assure stability with **capacitive loads (from increased logic)**.
- **Off-chip decoupling capacitors** (uF) needed for LDO stability at the input and the output of the circuit.
- The reference and offset voltages are provided by **on-chip integrated BANDGAPs** (2/Shunt-LDO)
  - Vref value can be trimmed using trimbits.





$$VIN = 2 * Viofs + \frac{\boldsymbol{R3}}{1000} * IIN$$

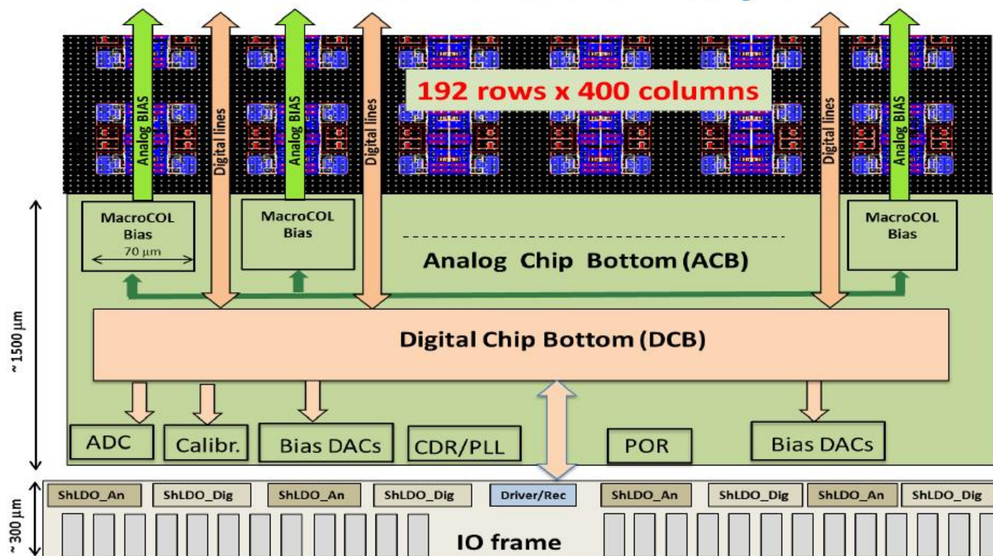
$$Viofs = 2\mu A * \boldsymbol{Riofs}$$

For an introduction to the Shunt-LDO circuitry see M.Karagounis paper:
https://indico.cern.ch/event/72160/attachments/1036621/1477145/Shunt-LDO_Regulator.pdf

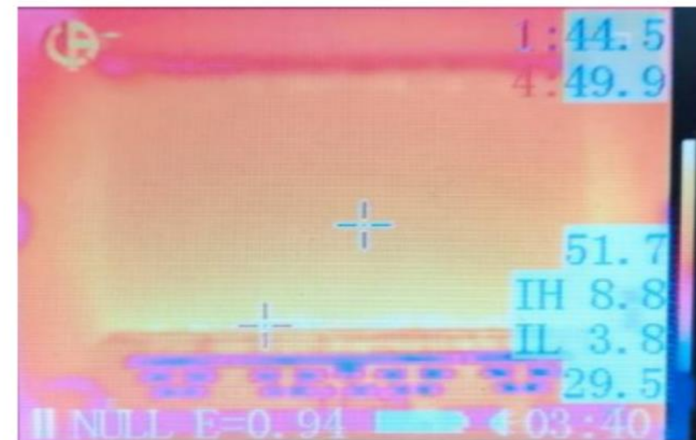
SLDO integration in RD53A

- Two SLDOs with 2A max. current integrated in RD53A
  - → Conservative ≤100% current margin
  - → Seperate analog and digital supply voltage generation
  - → Max. 4W per SLDO, final chip: 1W/cm²
- Shunt transistors seperated in four 0.5A transistors, distributed along wire bond pads

RD53A functional floorplan



Picture with thermal camera for Iin=2.0A, Vin =1.45V (2.9W)

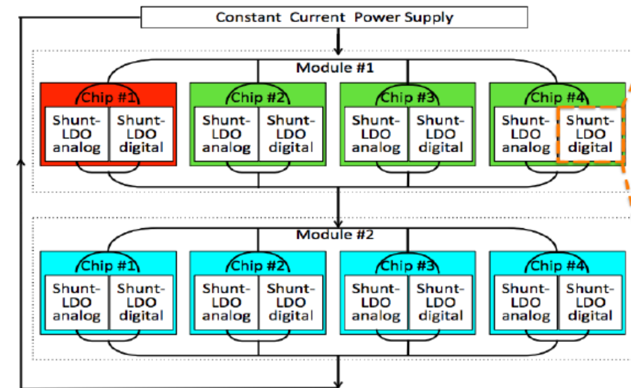


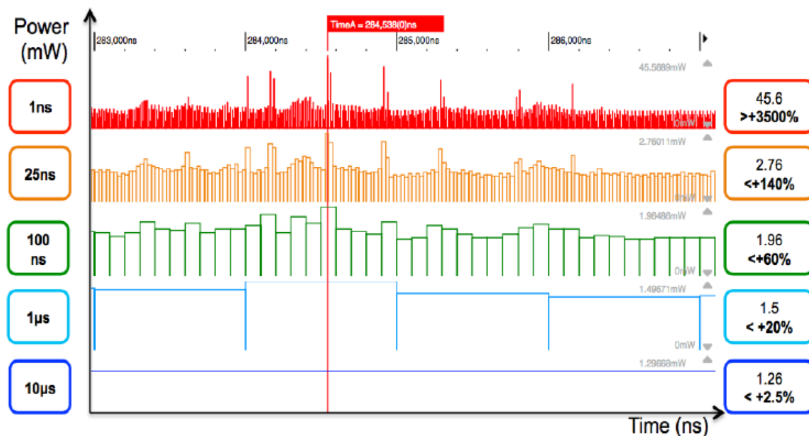
System simulations with power profiles

System simulations (Cadence Virtuoso) with Shunt-LDO detailed design, serially powered pixel modules and parasitic elements.

Dynamic profiling of both digital and analog power

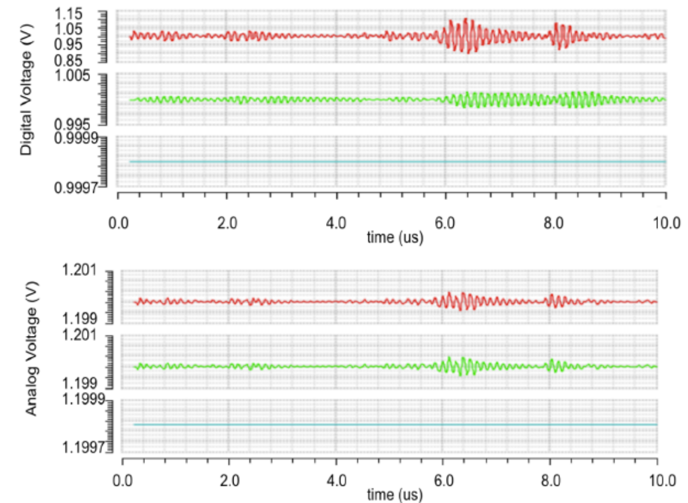
Noise coupling has been found to been within acceptable limits (Vout ripple 100mV for digital, <10mV for analog).





Power profiles at different time-scales with Monte Carlo hits (3GHz/cm²), triggers (1MHz) from detailed gate level simulations after place and route and with circuit parasitics for 64x4 pixels

S.Marconi (CERN)



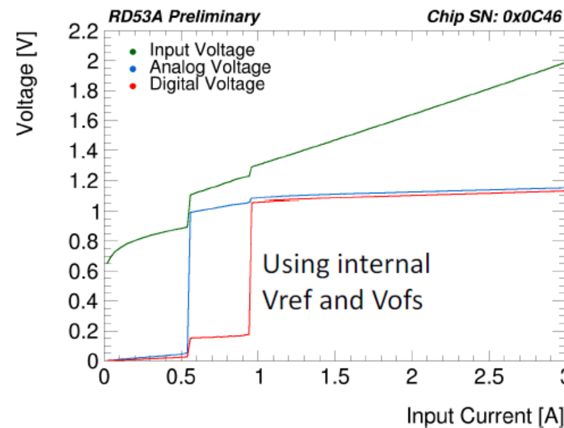
More details: http://iopscience.iop.org/article/10.1088/1748-0221/12/02/C02017/pdf

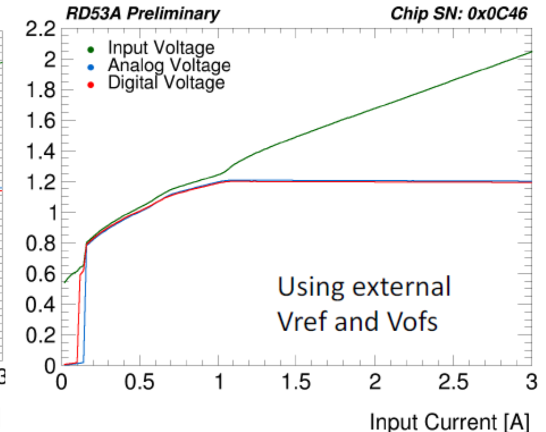
SLDO tests on RD53A

Line regulation:

Bandgaps need a minimum V to start:

- **New bandgap design (mini-asic)**
- Difference in analog and digital bandgaps under study.



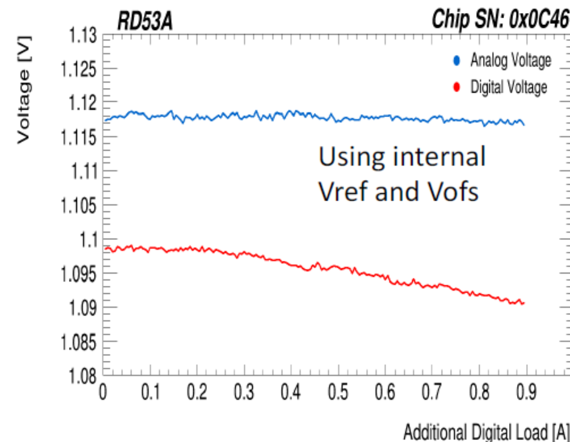


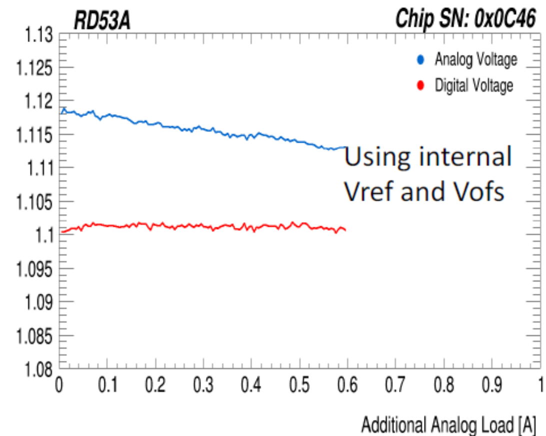
Impedance analysis:

- Slope is higher than expected ≈0.37Ω instead of 0.3Ω, **parasitics under investigation**
- Offset is lower than expected ≈0.9V instead of 1.0V, **understood by simulation**

Load regulation

- After power-up 100mA digital load (no clk) and 400 mA analog load (matching simulations).
- The digital voltage (VDDD) decreases over the additional load ~8mV/0.9A
- The analog voltage (VDDA) decreases over the additional load ~5mV/0.6A

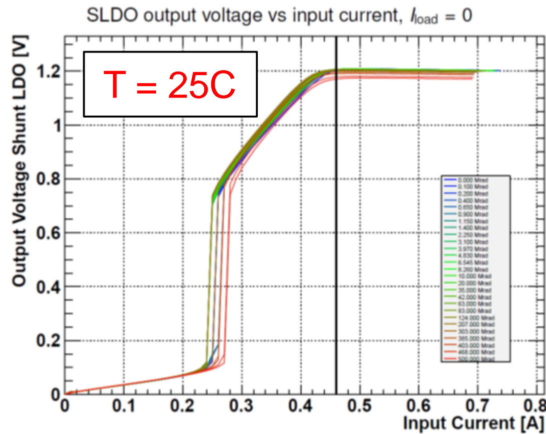


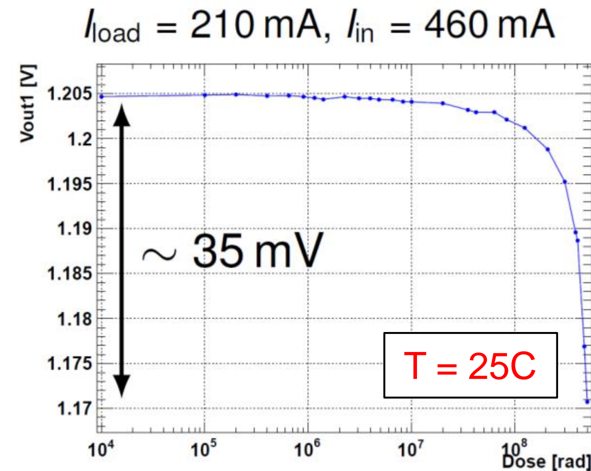


D. Koukola, CERN

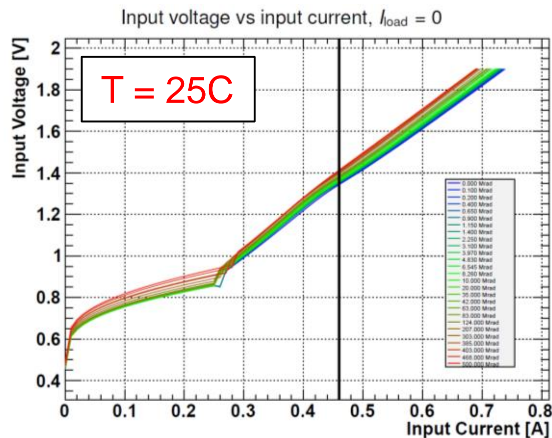
SLDO radiation hardness: 1st prototype

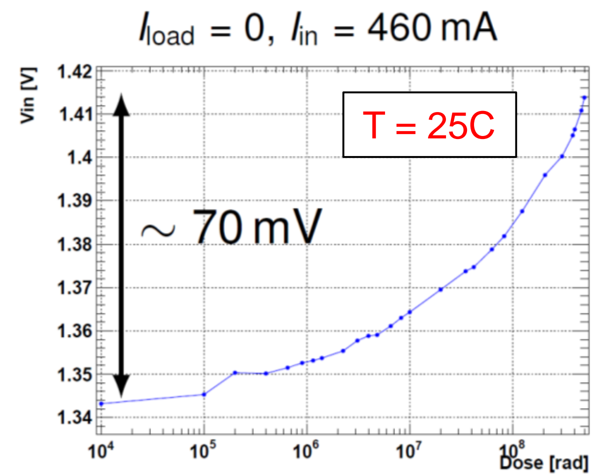
M. Backhaus (ETH), M. Hamer (Uni Bonn), F. Hinterkeuser (Uni Bonn), M. Karagounis (FH Dortmund), S. Orfanelli (CERN), D. Ruini (ETH), G. Sguazzoni (INFN)





→ V_{out} adjustable, can compensate





→ Not adjustable, can Not compensate

SLDO radiation hardness: 1st prototype

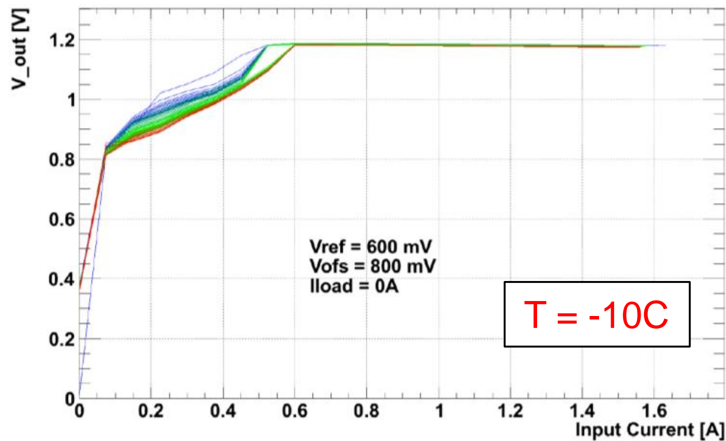
M. Backhaus (ETH), M. Hamer (Uni Bonn), F. Hinterkeuser (Uni Bonn), M. Karagounis (FH Dortmund),
S. Orfanelli (CERN), D. Ruini (ETH), G. Sguazzoni (INFN)

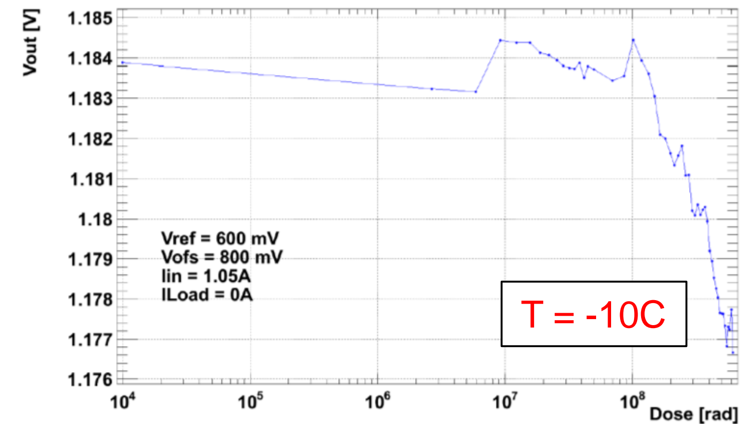
- Gate-drain connected transistor M6 defines I_{ref} for I_{in} adjustment
- Radiation induced threshold shift in M6 changes I_{in} setting and thus V_{in} as a function of I_{in}
  → larger V_{in} at same I_{in}

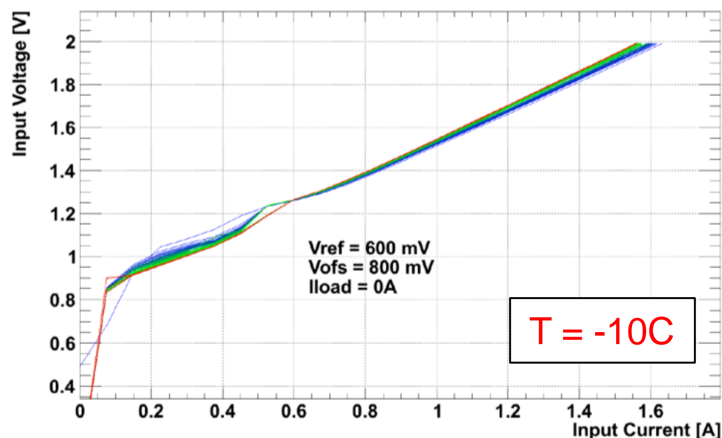
→ Adjusted I_{ref} generation in 2nd prototype incl. adjustable offset
→ can compensate by offset adjustment

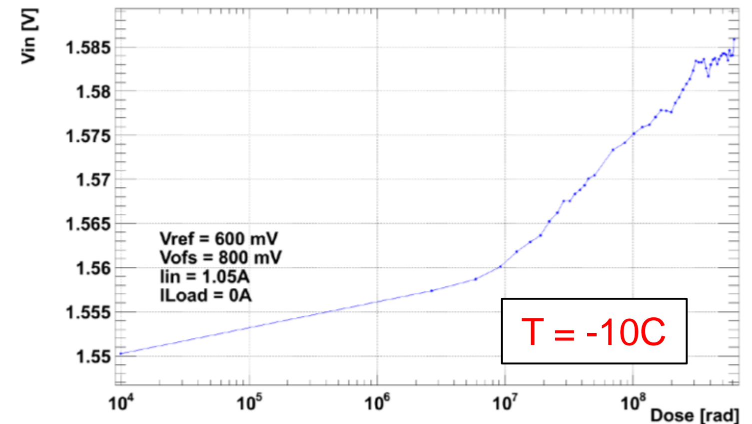
SLDO radiation hardness: 2nd prototype

M. Backhaus (ETH), M. Hamer (Uni Bonn), F. Hinterkeuser (Uni Bonn), M. Karagounis (FH Dortmund), S. Orfanelli (CERN), D. Ruini (ETH), G. Sguazzoni (INFN)









Failure modes and protection

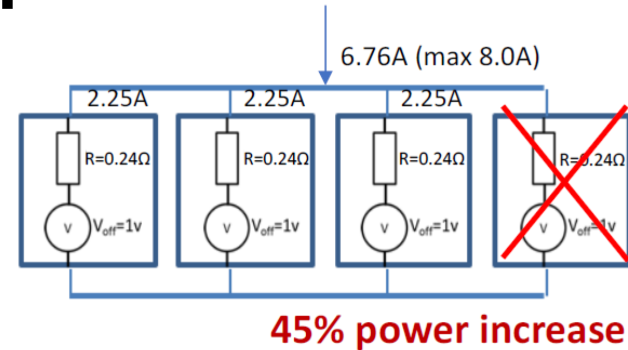
Open circuit:

Collapse due to load or fast start-up

⇒ current transients & power increase for remaining chips

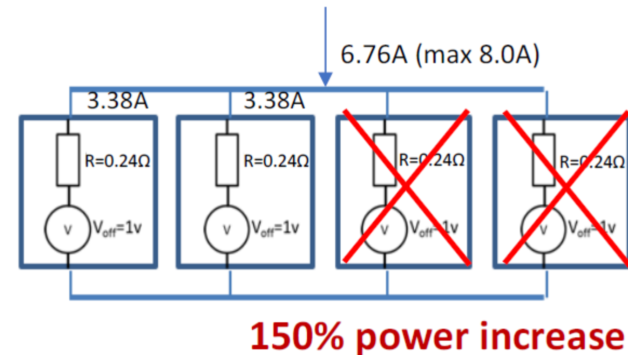
⇒ over-voltage transients at Vin

⇒ power increase for the remaining



Potential protection mechanisms:

- Voltage clamp to limit the input voltage for increased Iin (under study)
- Operation with high offset voltage and low value of Req
- Connect double-chip modules in parallel (if geometry permits)
- Use of PSPP chip in ATLAS to bypass modules



Overload / Short circuit:

Physical short or over consumption due to failure/misconfiguration:

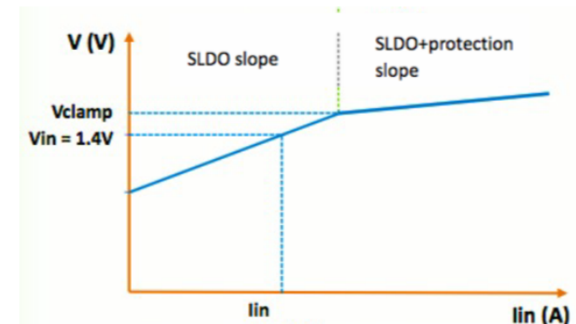
=>shorted Shunt-LDO takes most of the module current

=>input voltage decreases (1.1V) but not collapsing fully

=>rest of the chips underpowered

Potential protection mechanisms:

- Passive or active fuse
- Overcurrent protection (under study)
- Use of PSPP chip in ATLAS to bypass modules

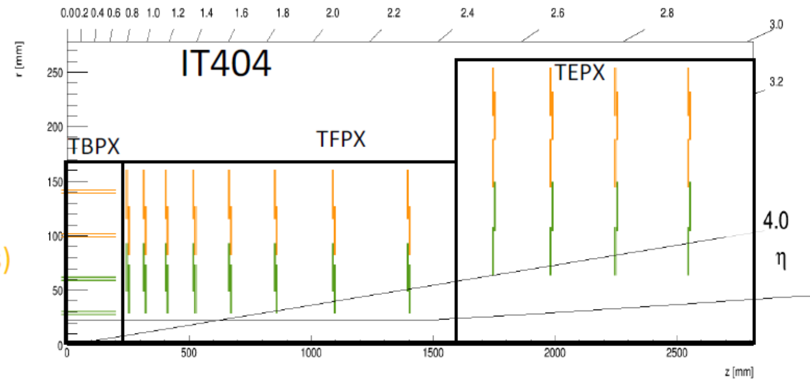


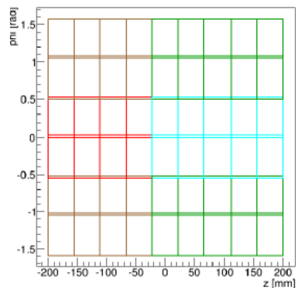
The planned SP system in CMS

CMS Inner Tracker (pixel) detector layout:

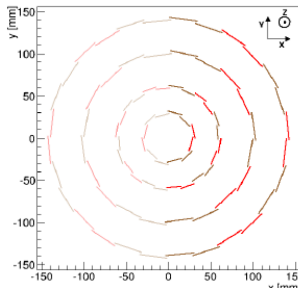
- 3 subsystems
- Accessible & replaceable system
- Serial powering chains built
  - In z for barrel sections & in ϕ for rings
- Powering unit: Modules always in series
  - 2-chip modules TBPX L1, L2 & R1, R2 (4A chains)
  - 4-chip modules TBPX L3, L4 & R3, R4, R5 (8A chains)

- in total, ~ 564 SP chains for ~4244 modules
- Planar sensors. 3D are considered for inner layers/rings.

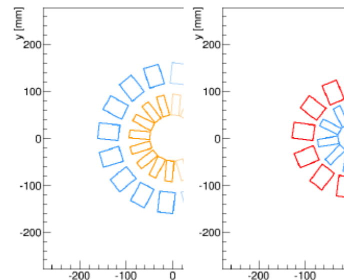




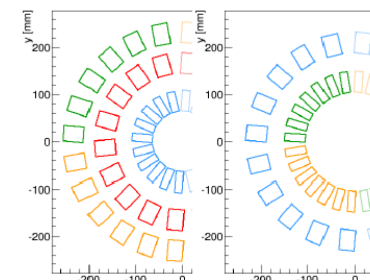
TBPX L1



TBPX



TFPX R1,R3 TFPX R2,R4



TEPX R1,R3,R5 TEPX R2,R4

Serial power chains in TBPX:

- 1 serial power chain for 2 consecutive rods in φ.
- Modules at Z=0: all modules connected to the same (Z) end (alternation by layer)

Serial power chains in TFPX/TEPX:

- Up to 4 chains per (X) side /(Z) side of a ring.
- Chains do not connect front/back side for easiness of mechanics.

The planned SP system in CMS

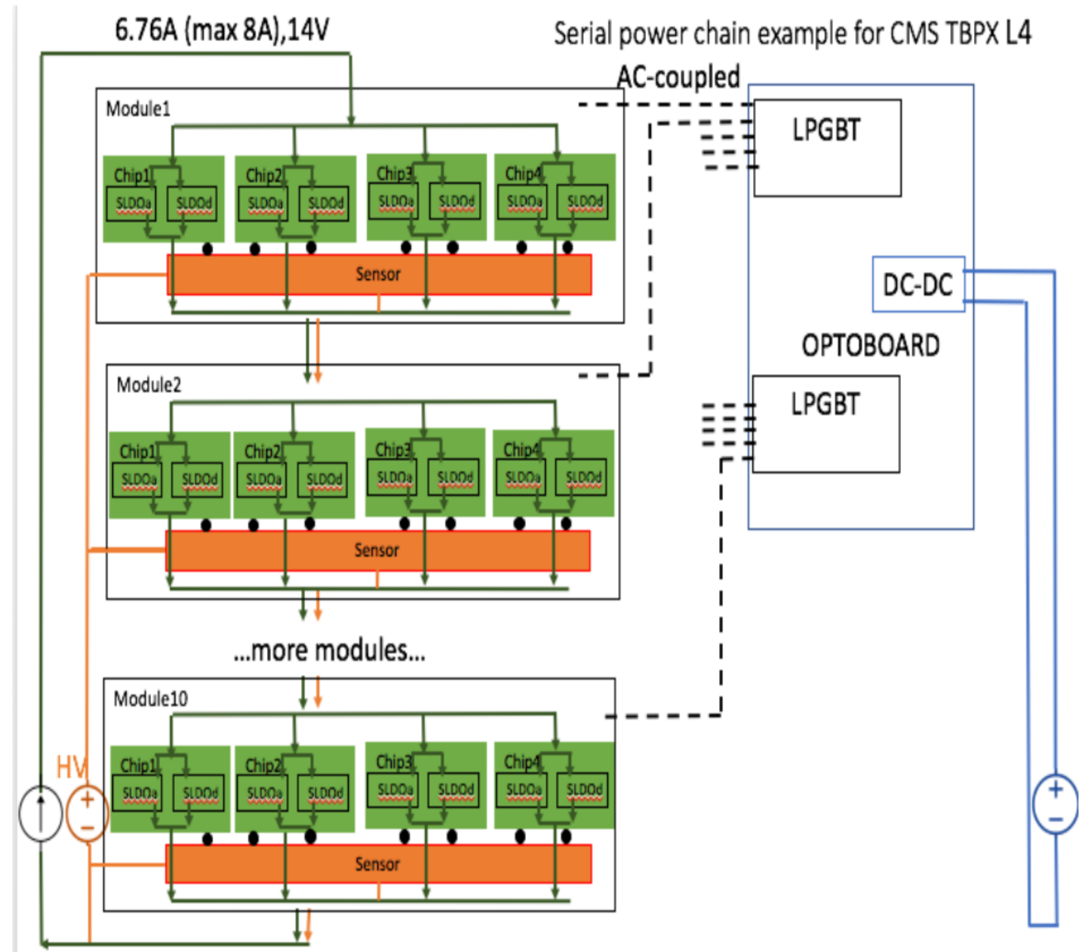
Serial power chains in CMS:
- Up to 10 modules per chain
- 1 serial power chain for 2 consecutive rods in φ.
- No parallel modules. Only in series modules and chips in parallel.

Under study “simple” on-chip integrated protection mechanisms such as voltage clamps and over-load current limitation.

Always reading/controlling with an optoboard modules that belong to the same chain.

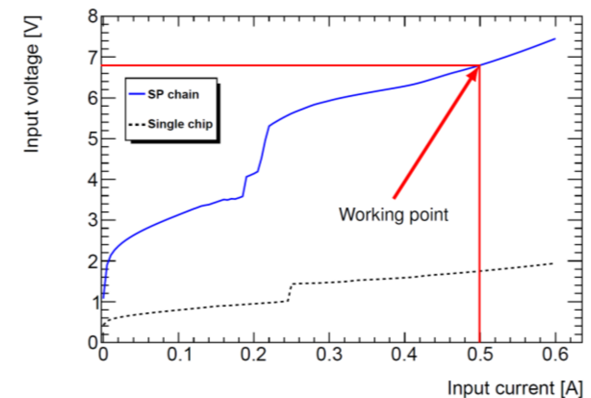
One NTC/SP chain hardwired interlock system

HV modularity (>1 HV line per SP HV modularity (>1 HV line per SP chain) follows serial power chains.
Extra return lines for HV under discussion



Steps towards a SP system validation at ETH: RD53A in serial powering

- Study RD53A single chips in serial powering mode (constant current supply)
- Build and operate chain of ~4 RD53A chips on PCBs
  - actively involved:
    - Bonn (ATLAS)
    - CERN (CMS)
    - ETH (CMS)
  - Connect all chains together
    → operate first chain of realistic lengths
  - Connect two/four chips in parallel, rest in series
    → study current sharing etc.
- Planned for summer this year in a common effort at CERN



Steps towards a SP system validation at ETH: Modules in a realistic system

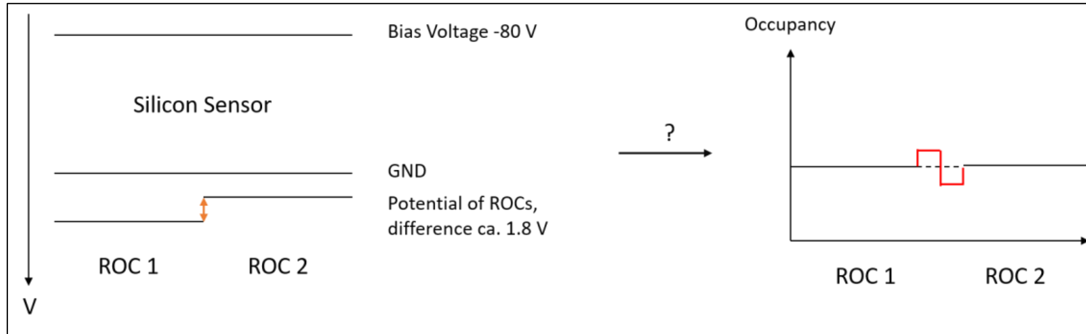
- To validate the serial powering scheme for detector operation, a realistic chain of modules on CO2-cooled mechanics is needed.

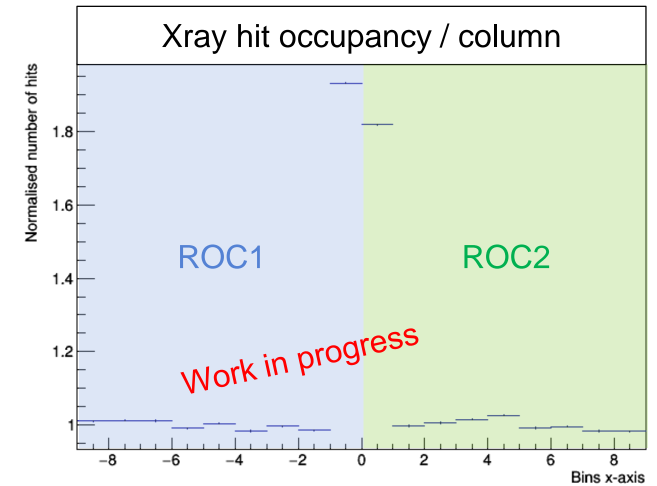
- Will build a realistic „barrel“ thermo-mechanical setup (final dimensions)
  → Design and build carbon support structure, piping, etc. for one SP chain
  → Build test box/freezer for environmental control
  → Install „cooling lab“ in clean room vicinity, piping to clean room

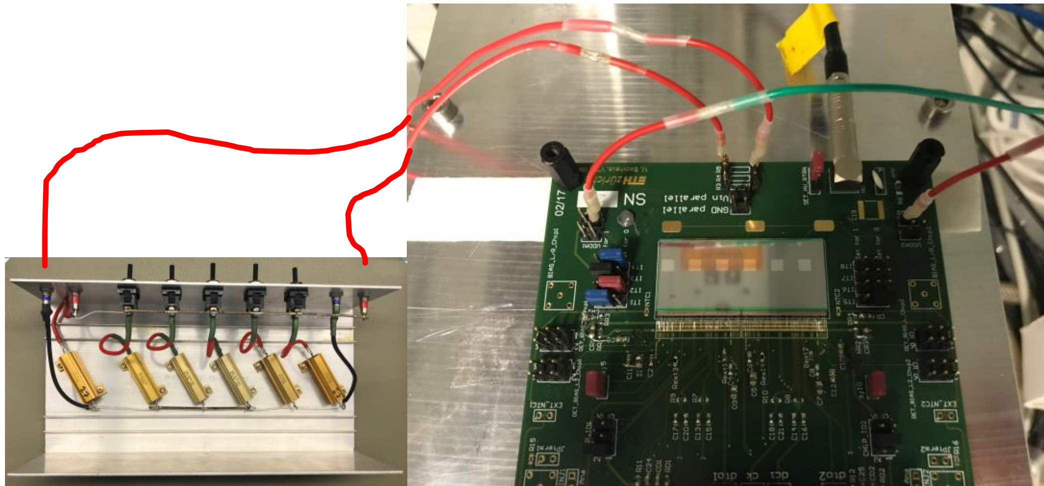
- Design and build RD53A 2x2 modules
  → Produce prototype HDI and test current routing
  → Build digital module (unprocessed chiops, no sensor)
  → test HDI, compare chip performance
  → Build number of RD53A 2x2 modulesIntegrate on mechanics support
  → Test and (hopefully) validate serial powering

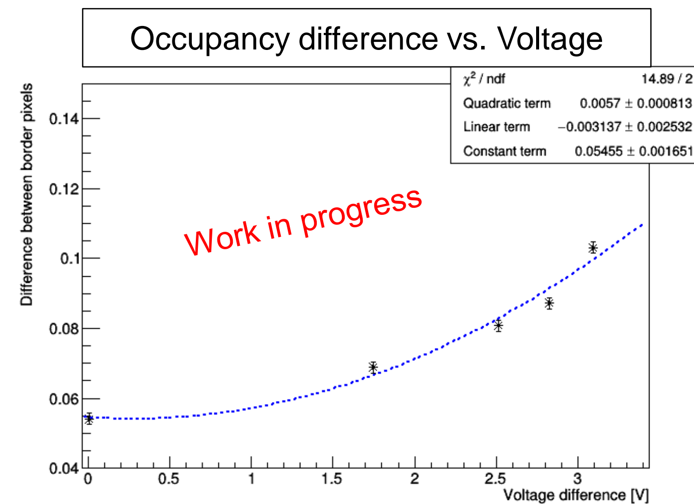
A view to the side…
First on-module SP demonstrator at ETH

[S. Tschui, D. Ruini]









Summary

- A lot of progress in serial powering R&D
- CMS started years after ATLAS, but now head to head
- Serial powering proved to be more robust than expected in all test systems
- Realistic large system never build to date
  → ATLAS focusses on FE-I4 modules on phase 2 like mechanics
  → CMS will build systems with RD53A modules ~next year
- Serial powering impacts details in about all detector components:
  AC coupled data, data format, connector specs, **voltage rating** of filter capacitances, …