

Semestral Project     Master Project     Thesis     Other

## **Buried channel in a dummy CMOS device**

### **Description of the fabrication project**

The goal is to demonstrate the integration of a microfluidic circuitry in a dummy 100  $\mu\text{m}$  thick CMOS device. Some dummy chips are prepared to train in handling 100  $\mu\text{m}$  chips and to define a process flow in order to obtain buried channels embedded in them.

<b>Technologies used</b>			
Positive resist, dry etching, grinding, gas etching, parylene depo, SEM			
<b>Laser direct write data</b>			
<b>Mask #</b>	<b>Critical Dimension</b>	<b>Critical Alignment</b>	<b>Remarks</b>
1	<b>3 <math>\mu\text{m}</math></b>	First mask	
2	<b>100 <math>\mu\text{m}</math></b>	10 $\mu\text{m}$	
<b>Substrate Type</b>			
Silicon <100>, $\varnothing$ 100mm, 525 $\mu\text{m}$ thick, SS polished + 1 $\mu\text{m}$ SiO <sub>2</sub>			

### **Interconnections and packaging of final device**

Thinning/grinding/polishing of the samples is required at some stage of the process.

No     Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.






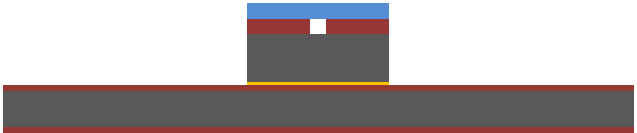


No     Yes => confirm dicing layout with CMi staff





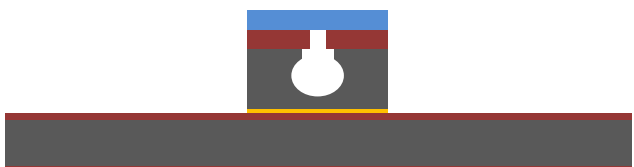
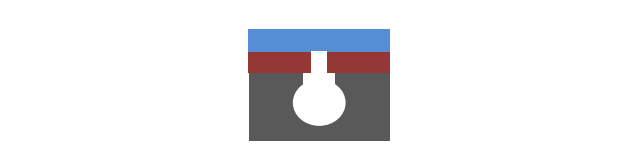


Wire-bonding of dies, with glob-top protection, is required at the end of the process.

No     Yes => confirm pads design (size, pitch) and involved materials with CMi staff

## Step-by-step process outline



Step	Process description	Cross-section after process
01	Coating Machine: ACS 200/Z1 Resist: AZ ECI 3007 Thickness: 1 $\mu\text{m}$ Recipe: 0123	
02	Exposure & development Machine: MLA150 Layout: Trenches HQ, dose 130mJ/cm2, defoc 0 Machine: ACS200 Recipe: 0923	
03	SiO2 etching Machine: SPTS/Z2 Recipe: SiO2 PR 3:1 soft Time: 5 min	
04	PR stripping Machine: Tepla gigabatch/Z2 Recipe: High_strip Time: 5 min	
05	Coating Machine: ACS 200/Z1 Resist: AZ ECI 3027 Thickness: 4 $\mu\text{m}$ Recipe: 0128	
06	Exposure & development Machine: MLA150 Layout: Grid HQ, dose 400 mJ/cm2, defoc -2 Machine: ACS200 Recipe: 0928	
07	SiO2 etching Machine: SPTS/Z2 Recipe: SiO2 PR 3:1 soft Time: 5 min	

<p><b>08</b></p>	<p>Si etching          Machine: AMS/Z2          Recipe: SOI.acc +++++          Time : 20 min</p>	
<p><b>09</b></p>	<p>PR stripping          Machine : Tepla gigabatch/Z2          Recipe: Strip_high          Time: 10 min</p>	
<p><b>10</b></p>	<p>SiO2 stripping (backside)          Machine: SPTS/Z2          Recipe: SiO2 PR 2:1          Time: 5 min</p>	
<p><b>11</b></p>	<p>Backside grinding          Desired thickness: 100 µm</p>	
<p><b>12</b></p>	<p>Frontside protection          UV tape</p>	
<p><b>13</b></p>	<p>Chip on carrier wafer          Machine: Suss RC-8 THP/Z6          Quickstick</p>	
<p><b>14</b></p>	<p>Protection removal          UV light/Z11</p>	
<p><b>15</b></p>	<p>Trenches etching          Machine: AMS/Z2          Recipe: SOI.acc 5-          Time: 8 min          Target: 30 um</p>	

16	Parylene depo Thickness: 200nm	
17	Parylene etching Machine: SPTS/Z2 Recipe: PI_vertical Time: 22 sec	
18	Channel etching XeF2 etching 45-50 pulses (30 sec each) at 2700 mTorr Target: 40 um (diameter)	
19	Parylene stripping Machine: Tepla gigabatch/Z2 Recipe: Strip_high Time: 3'	
20	Frontside protection UV tape	
21	Chip detachment and cleaning Acetone	
22	Protection removal	
23	Backside protection	

Lab : CERN  
Operator Name : Riccardo Callegari  
Supervisor Name : Alessandro Mapelli

Phone : +41227675013  
Office : 21/1-049  
E-mail : riccardo.callegari@cern.ch

<b>24</b>	Trench filling Machine: Parylene depo Thickness: 3 um	
<b>25</b>	Protection removal	
<b>26</b>	Thermal cycle Machine: Heraeus T6060 oven N=2, r=0, P0=50 deg, T1=30', P1=300 deg, T2=2h, P2=300	