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CMi EPFL Center of MicroNanoTechnology

☐ Semestral Project ☐ Master Project ☐ Thesis ☑ Other

Buried channel in a dummy CMOS device

Description of the fabrication project

The goal is to demonstrate the integration of a microfluidic circuitry in a dummy 100 µm thick CMOS device. Some dummy chips are prepared to train in handling 100 µm chips and to define a process flow in order to obtain buried channels embedded in them.

Technologies used
Positive resist, dry etching, grinding, gas etching, parylene depo, SEM

Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**3 µm**	First mask	
2	**100 µm**	10 µm	

Substrate Type
Silicon <100>, Ø100mm, 525um thick, SS polished + 1 um SiO2

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.
☐ No ☑ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.
☑ No ☐ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.
☑ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

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Step-by-step process outline

Step	Process description	Cross-section after process
01	Coating Machine: ACS 200/Z1 Resist: AZ ECI 3007 Thickness: 1 µm Recipe: 0123	
02	Exposure & development Machine: MLA150 Layout: Trenches HQ, dose 130mJ/cm2, defoc 0 Machine: ACS200 Recipe: 0923	3 µm
03	SiO2 etching Machine: SPTS/Z2 Recipe: SiO2 PR 3:1 soft Time: 5 min	
04	PR stripping Machine: Tepla gigabatch/Z2 Recipe: High_strip Time: 5 min	
05	Coating Machine: ACS 200/Z1 Resist: AZ ECI 3027 Thickness: 4 µm Recipe: 0128	
06	Exposure & development Machine:MLA150 Layout: Grid HQ,dose 400 mJ/cm2, defoc -2 Machine: ACS200 Recipe: 0928	100 µm
07	SiO2 etching Machine: SPTS/Z2 Recipe: SiO2 PR 3:1 soft Time: 5 min	

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08	Si etching Machine: AMS/Z2 Recipe: SOI.acc ++++ Time : 20 min	120 µm
09	PR stripping Machine : Tepla gigabatch/Z2 Recipe: Strip_high Time: 10 min	
10	SiO2 stripping (backside) Machine: SPTS/Z2 Recipe: SiO2 PR 2:1 Time: 5 min	
11	Backside grinding Desired thickness: 100 µm	
12	Frontside protection UV tape	
13	Chip on carrier wafer Machine: Suss RC-8 THP/Z6 Quickstick	
14	Protection removal UV light/Z11	
15	Trenches etching Machine: AMS/Z2 Recipe: SOI.acc 5- Time: 8 min Target: 30 um	

16	Parylene depo Thickness: 200nm	
17	Parylene etching Machine: SPTS/Z2 Recipe: PI_vertical Time: 22 sec	
18	Channel etching XeF2 etching 45-50 pulses (30 sec each) at 2700 mTorr Target: 40 um (diameter)	
19	Parylene stripping Machine: Tepla gigabatch/Z2 Recipe: Strip_high Time: 3’	
20	Frontside protection UV tape	
21	Chip detachment and cleaning Acetone	
22	Protection removal	
23	Backside protection	

24	Trench filling Machine: Parylene depo Thickness: 3 um	
25	Protection removal	
26	Thermal cycle Machine: Heraeus T6060 oven N=2, r=0, P0=50 deg, T1=30’, P1=300 deg, T2=2h, P2=300	