Development of next-generation timing system for the Japan Proton Accelerator Research Complex

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J-PARC Center

October 2020
1. Introduction

2. Original timing system

3. Next-generation timing system

4. Conclusion
Japan Proton Accelerator Research Complex (J-PARC)

- Accelerators: 400 MeV linac, 3 GeV RCS, 30 GeV Main Ring (MR)
- Experimental facilities: MLF \((n, \mu)\), Hadron hall, Neutrino
- Beam operation started in 2006

- High intensity: 1 MW (RCS), 750 kW (MR)
- A precise and stable timing system is necessary to avoid beam losses and residual activation
  - jitter below 1 ns
MR magnet pattern

- MR accelerates protons from 3 GeV to 30 GeV at repetition period of 2.48 s (FX) or 5.2 s (SX)
- J-PARC machine cycle defined by MR cycle
Linac, RCS running at 25 Hz rep rate: Tick of J-PARC timing
Four RCS beams injected to MR, others (FX: 58, SX: 126) delivered to MLF
Beam parameters (intensity, macro pulse width, chopping width, injection painting) different for destinations
Role of timing system: to give appropriate instructions to the accelerator devices for various operating conditions

Continuous user operation / single shot for commissioning / etc...

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Categories of J-PARC timing signal

Scheduled timing:
- Defined by the programmed delay from the 25 Hz reference trigger sent from the central control building (CCB)
- Most devices use scheduled timing

Synchronization timing:
- Generated by the accelerator devices for synchronization to the beams
- Linac chopper gate, RCS extraction kicker, MR injection kicker, etc.

We focus on the scheduled timing in this presentation.
1. Introduction

2. Original timing system

3. Next-generation timing system

4. Conclusion
25 Hz reference trigger, 12 MHz clock, and Type are sent from CCB to facilities.

Star configuration: same signal delivered

Type represents the operation of next 25 Hz cycle.
Operating principle of scheduled timing

According to type, receivers work as follows:

- Output pulse with programmed delay
- No output
- Continue counting for longer delay beyond reference trigger
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Operating principle of scheduled timing

Type sequence:

- A type sequence represents operation in a MR cycle
- End code or jump code indicates the end of cycle
- Changing type sequence, accelerator operation is switched
- Special word “S” sent additionally at the beginning of type sequence
High-precision synthesizer and clock generator generate 12 MHz master clock.

Reference trigger generated by counting clocks.

Timing transmitter module sends serialized 32-bit type code prior to reference trigger:
- MSB: special flag
- Each 8-bit for linac, RCS, MR. 7-bit reserved.

Three signals sent to facilities via fanout and E/O.


Timing receiver station in the facilities

- Three delivered optical signals are input to the timing receiver module via O/E
- Receiver module picks up control word from LUT by taking specified 8-bit from the 32-bit type code
- Behaves as the operating principle in previous slide
- 96 MHz delay counter clock from 12 MHz clock by PLL
- Output level converted NIM modules
- Daisy chain possible
Original timing system works nicely

The original timing system working without major problems since 2006.
The stable / precise timing system serving the high intensity beam operation.

RCS 1 MW continuous operation demo:

MR beam power reached 510 kW:

[Graphs and diagrams showing beam power history and timing system operation]
Why next-generation system?

Optical component (Finisar v23826) was discontinued, no successors:

O/E, E/O modules are no longer in production and the original system cannot be maintained for longer period, while we have enough spare modules.

We started development of the next-generation system from 2016.
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Design considerations

- Impossible to replace whole system at once. Compatibility to the original system is most important

  → Popular timing system solutions (MRF, WR) not considered

- Three cables per station is infrastructure burden
- Metal cable between O/E and receiver may pick up noises from pulsed PS or high intensity beam. Receiver hang ups experienced

  → High speed serial communication containing three signals on single optical cable

- A set of VME and NIM crates requires space and cost. MR control rooms have limited space (and budget)

  → Small form factor (PLC) receiver also developed
- Yellow: newly developed modules
- New transmitter outputs serialized optical signal containing ref trig, clk, type
  - SFP as optical device
  - All connections are optical
- Optical fanout
- New receiver: VME and PLC. Works same as original
- Also outputs same three signals so that original receivers can be used as is
Configuration

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- New receiver: VME and PLC. Works same as original
- Also outputs same three signals so that original receivers can be used as is
New transmitter function: shift-jump

- In original system, switching of type sequence is allowed only at the end of the type sequence
- "Beam-on" trigger for measurement is stopped when interlock by modifying LUT by fast reflective memory network
- "Shift-jump" function: according to the jump table for the interlock types, the type sequence is switched so that beam-on trigger is suppressed

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High speed serial communication: transmitter

- At each reference trigger, type picked up from type memory
- New transmitter module generates an event every 12 MHz clock
  - Payload of high speed serial communication
- GTP on Xilinx Spartan-6 used
- Serial stream converted to optical signal by SFP module
Protocol

- A sequence: 12 consecutive 8 bit words
  - Repetition at 12 MHz
  - K28.5 (comma), event (E), 10 bytes data
  - 8B/10B encoded, 1.44 Gbps
  - All events are used for generation of 12 MHz clock at receiver

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
</table>
## Protocol

(1) Null event: sent when idle

```
<table>
<thead>
<tr>
<th>Null</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>K28.5</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
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<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
</tr>
</tbody>
</table>
```

$E(null) = D0.0$ (0x00)

(2) Trigger event

```
<table>
<thead>
<tr>
<th>Trig</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>K28.5</td>
<td>E(trig)</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
</tr>
</tbody>
</table>
```

$E(trig) = D1.0$ (0x01)

(3) Type event: before trigger

```
<table>
<thead>
<tr>
<th>Type</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>K28.5</td>
<td>E(type)</td>
<td>type1</td>
<td>type2</td>
<td>type3</td>
<td>type4</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
</tr>
</tbody>
</table>
```

$E(type) = D2.0$ (0x02)

(4) S event: at beginning of type sequence

```
<table>
<thead>
<tr>
<th>S</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
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<td></td>
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<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
</tr>
</tbody>
</table>
```

$E(S) = D3.0$ (0x03)

(5) S count event

```
<table>
<thead>
<tr>
<th>Scnt</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>K28.5</td>
<td>E(Scnt)</td>
<td>Scnt1</td>
<td>Scnt2</td>
<td>Scnt3</td>
<td>Scnt4</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
</tr>
</tbody>
</table>
```

$E(Scnt) = D4.0$ (0x04)

(6) trig count event

```
<table>
<thead>
<tr>
<th>Tcnt</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
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<td>D0.0</td>
<td>D0.0</td>
<td>D0.0</td>
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</tbody>
</table>
```

$E(Tcnt) = D5.0$ (0x05)

- Many reserved events
High speed serial communication: receiver

- On the receiver GTP, Clock and Data Recovery (CDR) is used to decode the 144 MHz clock and data
- 12 MHz clock is generated looking at commas
- Event analyzer extracts trigger, type, and other information
- Clock, trigger, and type are fed into the same circuit as original modules
- As a whole, the new receiver behaves in the same way as the original system
Pitfall: latency of pure GTP is not deterministic at power-up

- Phase of recovered 144 MHz clock different at each power-ups
  - Normal applications for data transfer do not care
- Critical issue for timing system
- Any solutions?

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Yes, solution found!

The solution is found in R. Giordano's TNS articles:

- We appreciate their good work

We implemented fixed-latency logic according to the reference.
Fixed-latency logic implementation (receiver side)

Overview:
- **GTP**
- **GTPCLKOUT**
- **RXUSRCLK_IN**
- **RXUSRCLK2_IN**
- **RXDATA_OUT[9..0]**
- **GTPRESET_IN**
- **RXSLIDE_IN**

10B/8B Decorder
Comma Detector and Aligner

Comma detector and aligner (CDA):
- Comma found
- Phase offset

• 10B/8B decoder and CDA are implemented in FPGA fabric, outside of GTP
• Phase offset is measured and fed to aligner
• If offset is even number of UI, RXSLIDE asserted necessary times to adjust phase
• In case of odd number, GTP is reset until the offset becomes even number

With the logic, deterministic latency is realized.
Fixed-latency logic implementation (receiver side)

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10B/8B Decoder
Comma Detector and Aligner

Comma detector and aligner (CDA):

- Comma Detector
- Comma found
- Phase Detector
- Phase offset
- Aligner
- State Machine

FPGA fabric

- Serial stream
- DATA[7..0]
- Is_K
- Recovered clock

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Comma

Detector

and

Aligner

Comma detector and aligner (CDA):

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Comma Detector and Phase Detector

Aligner

State Machine

GTPRESET

RXSLIDE

RXDATA[9..0]

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With the logic, deterministic latency is realized.
12 MHz clock jitter measurement by Tek DPOJET

- pk-pk 194ps
- RMS 22ps

- 12 MHz clock used for reference of 96 MHz counter clock and accelerator digital clocks (LLRF, etc)
- RMS 22 ps and pk-pk 200 ps, sufficiently low
- Trigger jitter similar (not measured by DPOJET)

Next-generation system performance confirmed.
Current status

- Original transmitter module was replaced with new transmitter in January 2020
- Until now, 12 receiver stations with 36 new receiver modules completed at linac and RCS
- Another 12 receiver stations to be done in this FY
- PLC receiver modules will be installed at new power supply buildings in MR
Conclusion

- J-PARC timing system is designed to fit the operation of the accelerator complex, which has multiple beam destinations.
- Original system has been working nicely, while key optical component is obsolete. Next-generation timing system has been developed with emphasis on compatibility.
- Next-generation system utilizes high speed serial communication technology. Fixed latency logic is implemented.
- Successfully deployed in 2020.

Note:
The serial communication framework is based on common technologies. It can be implemented with newer FPGAs. Next-generation system expected to be sustainable.