FELIX: commissioning the new detector interface for the ATLAS trigger and readout system

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Overview

ATLAS TDAQ evolution for Run 3

FELIX* readout system

Performance & commissioning

Conclusions

*FELIX : Front-End LInk eXchange → (custom) PCIe cards hosted in COTS servers
ATLAS TDAQ in Run 2

~ 2 MB events, ~ 50 GB/s network bandwidth, 
~ 1.5 GB/s recording throughput

Custom point-to-point links

Point-to-point S-LINKs*

VME (detector-specific)

Custom elx components

PCs (COTS)

*S-LINK: CERN Simple Link
ATLAS TDAQ in Run 2

• Custom HW/protocols for Front-End (FE) readout

• Data buffered in FE elx waiting for L1 trigger (max latency ~2.5 μs)

• Trigger and LHC clock sent to both FE elx and (detector specific) ReadOut Drivers (RODs)

• RODs send data to ReadOut System (ROS) which buffers them for High-Level Trigger (HLT) requests

• HLT finalises event selection in two steps

Readout system:
~1 k ROD boards
~150 ROS servers
Upgrade for Run 3

LHC Phase-I Upgrade → ATLAS trigger & detector upgrade

1) new muon detectors in both forward and transition regions
   → additional readout channels more than full present muon spectrometer

2) new trigger elx in calorimeter system
   → upgraded readout architecture
Upgrade for Run 3

Same requirements as Run 2

GBT* or FULL mode links

25-100 Gb/s Ethernet

*GBT: GigaBit Transceiver with Versatile Link
Upgrade for Run 3

Same requirements as Run 2 but reduced custom components

- GBT* or FULL mode links
- 25-100 Gb/s Ethernet
- PCIe Gen3 (TDAQ specific)
- VME (detector-specific)

*GBT: GigaBit Transceiver with Versatile Link

Custom elx component including FELIX cards

PCs (COTS)
New Readout Architecture

ROD + ROS legacy system

FELIX + SW ROD

DCS + TTC via FELIX
New Readout Architecture

FELIX :
- data/signal/message routing from/to FE elx
- detector state agnostic
- pushes detector fragments to SW ROD servers

SW ROD :
- data collecting and processing
- supporting configuration, calibration, control, and monitoring
- interface to HLT

Run 3 FELIX system:
- ~100 FLX boards / 60 servers
- ~30 SW ROD servers
FELIX system

FLX-712 : ATLAS production board for Run 3
FELIX functionality

• Router between FE serial links and commercial network

• Data transport decoupled from data processing

• Get and distribute TTC (Timing, Trigger and Control) signals

• GBT-mode configurable e-links*

• Detector independent

*e-link: data mux/demux protocol (more physical electrical links packed over one single GBT link)
FELIX block diagram

PC hosting up to two PCIe FELIX cards + network card
FLX-712 card features

- Kintex UltraScale FPGA
- 8 MiniPODs
- 16-lane PCIe Gen3
- Flash and μ-controller for FW update
- On-board jitter cleaner
- Timing mezzanine to interface TTC system

- 24 x 4.8 Gb/s links @ PCIe limit
- 12 x 9.6 Gb/s links @ PCIe limit
- 48 links as TTC dispatcher
Run 3 parameters for FELIX readout (worst cases)

<table>
<thead>
<tr>
<th>Name</th>
<th>&lt;chunksize&gt;</th>
<th>Rate per channel</th>
<th>Channels per FELIX</th>
<th>Chunkrate per FELIX</th>
<th>Datarate per FELIX</th>
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</thead>
<tbody>
<tr>
<td>GBT Mode</td>
<td>40</td>
<td>100</td>
<td>384</td>
<td>38.4</td>
<td>12</td>
</tr>
<tr>
<td>FULL Mode</td>
<td>4800</td>
<td>100</td>
<td>12</td>
<td>1.2</td>
<td>46</td>
</tr>
</tbody>
</table>

GBT Mode → FPGA-resource limited

FULL Mode → PCIe-bandwidth limited
## Firmware flavours

<table>
<thead>
<tr>
<th>FLX-712 # chans</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GBT dynamic</td>
<td>4+4</td>
</tr>
<tr>
<td></td>
<td>- all combinations of e-links (2,4,8) and modes (8b/10b, HDLC)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>GBT semi-static</td>
<td>12+12</td>
</tr>
<tr>
<td></td>
<td>- static &amp; configurable links</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FULL</td>
<td>12+12</td>
</tr>
<tr>
<td></td>
<td>- 6+6 channel matches max PCIe bw</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- 12+12 channel @ lower bw</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LTDB* mode</td>
<td>24+24</td>
</tr>
<tr>
<td></td>
<td>- only clock distribution, trigger, slow control and monitor</td>
<td>(LTDB)</td>
</tr>
</tbody>
</table>

*LTDB: Liquid Argon Digitizer Board*
Software

low level sw → basic configuration/monitoring (e-link conf., felix monitoring)

higher level sw → data rate and channel monitoring

felix-star

• single-threaded event loop, any operation is one event

• networking based on new communication library: NetIO-next

• data transfer uses RDMA i.e. kernel not involved

• higher performance
Performance, integration and commissioning

GBT mode

- stable multi-hour operation (longer than average LHC fill)
- reliable parallel communication with test board featuring DCS components

~ 12.5 Gbps network throughput
Performance, integration and commissioning

GBT mode

• BUSY signal propagation correctly handled

• Emulator rump-up demonstrated rates 50% above expectation (150 kHz)
Performance, integration and commissioning

FULL mode

• stable multi-hour operation (longer than average LHC fill)
Performance, integration and commissioning

Stress test

• backpressure shows up at ~ 200 kHz
• achieved ~ 300 kHz
User support & integration

- Active user support → crucial:
  user issues more and more difficult to reproduce in TDAQ testbed
- Further push toward integration
Summary & Outlook

ATLAS TDAQ evolution for Run 3:
FELIX + SW ROD replace (part of) ROD + ROS system
→ more flexibility, reduced custom design
→ architecture for Run 4 and beyond

HW commissioning and deployment ongoing
(~/ 200 FELIX cards already delivered)

SW development in progress

Performance tests consistently exceed Run 3 requirements

User feedback more and more relevant

Please, see also talk by Serguei Kolos on SW ROD
Thanks!
Extras
ATLAS Readout in Run 3

New Muon detectors: New Small Wheels, small “BIS7/8” RPCs
New L1 Calo trigger system
→ exploit commodity and/or common hw as soon as possible

FELIX
• Connects directly to detector FEE
• Receives and routes data from detector directly to clients
• Routes L1 trigger, clock and control signals to detector FEE
• Able to interface both with GBT protocol and directly to remote FPGA via high bandwidth ‘FULL mode’ protocol

SW ROD
• Software process running on servers connected to FELIX via high bandwidth network
• Common platform for data aggregation and processing - enables detectors to insert their own processing into data path
• Previously performed in ROD hardware
• Buffers and - on request - serves data to HLT
• Interface indistinguishable from legacy readout (ROS)

• Control and monitoring applications now distributed among servers connected to data network
Upgrade for HL-LHC (Phase-II)

~ 5 MB events, ~ 5 TB/s network bandwidth, ~ 50 GB/s recording throughput

GBT, LpGBT* or FULL mode links

COTS network technology

Custom elx component including FELIX cards

*LpGBT: Low-power GBT
FELIX firmware design

Central router block handles e-links
   e-link: data mux/demux protocol designed for ATLAS

Fixed latency transmission to FE

DMA for PCIe throughput to host memory (2 × 64 Gbps)

Optical Link Transceiver using GBT protocol
   Two link modes:
      GBT-frame mode, Full mode

Decoding TTC information and LHC clock recovering

Data routing using E-Link

Legend:
   Main data path
   Slow control and monitor

PCIe DMA engine
Performance & integration (Phase-II)

FELIX testbed:

- $32 \times 260$ Mb/s links
- 1 MHz random L1A for NSW Phase II
- stable transfer rate with felix-star, no errors
- actual test to be performed with NSW vertical slice
Integration in FELIX testbed

Integration with new trigger system (ALTI)
- ALTI installed and update
- learning how to operate it

Integration with swROD
- several test runs with felix sw emulator
- rerunning test with new sw

Integration with OPC-UA
- DCS sw depends on NetIO library
- preparing joint set-up as common reference frame
Software transition

**felixcore**
- multiple-threaded, pipeline architecture
- networking based on “NetIO” library
- functional, minimal performance margin
- supported until all users migrated to felix-star

**felix-star**
- single-threaded event loop, any operation is one event
- networking based on “NetIO-next” library
- uses RDMA i.e. kernel not involved in data transfer
- higher performance
- transition in progress ...
NetIO-next performance tests

GBT test configuration:

**pc-tbed-felix-06**

*swrod_netio_next_publisher*
- 192..1152 e-links
- 1..12 publishing threads
- 40 bytes packets

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**netio-next**

*over*

100 Gbps Ethernet

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**pc-tbed-swrod-01**

*swrod_test application*
- 1..6 ROBs with 192 e-links per ROB
- 1..2 reading/assembling threads per ROB
- 6 HLT processing threads
- No custom processing

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**pc-tbed-net-03**

*swrod_hlt_requester*
- 50% EB requests
- Request rate is dynamically adjusted to the reply rate

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**asyncmsg**

*over*

40 Gbps Ethernet
NetIO-next performance tests

GBT test results:

No HLT

50% EB requests
**NetIO-next performance tests**

**FULL-mode test configuration:**

- **pc-tbed-felix-06**
  - swrod_netio_next_publisher
  - 24 e-links
  - 6 publishing threads
  - 5000 bytes packets

- **pc-tbed-swrod-01**
  - swrod_test application
  - 1..24 ROBs with 24..1 e-links per ROB
  - 6 total reading/assembling threads
  - 12 HLT processing threads
  - No custom processing

- **pc-tbed-net-03**
  - swrod_hlt_requester
  - 50% EB requests
  - Request rate is dynamically adjusted to the reply rate

- **netio-next**
  - over 100 Gbps Ethernet

- **asyncmsg**
  - over 40 Gbps Ethernet
NetIO-next performance tests

FULL-mode test results:

- investigating scaling problem