The WaveDAQ integrated Trigger and Data Acquisition System for the MEG II experiment

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Outlook at MEG Physics in one slide

MEG Collaboration aims to observe a $\mu^+ \rightarrow e^+ \gamma$ decay
• Impossible to observe in the SM (BR~$10^{-52}$)
• Very sensitive to Beyond SM physics.
MEG II sensitivity goal: $BR = 6 \times 10^{-14}$

Complementary measurement to $\mu^- \rightarrow e^-$ conversion (Comet/Mu2e), $\mu^+ \rightarrow e^+e^-e^+$ (Mu3e) and muon g-2

Irreducible Background
 Photon from: RMD, AIF, Bremsstrahlung

<table>
<thead>
<tr>
<th>Signal</th>
<th>Irreducible Background</th>
<th>Accidental Background</th>
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<tbody>
<tr>
<td>$e^+$</td>
<td>$e^+$</td>
<td>$e^+$</td>
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<tr>
<td>$\mu^+$</td>
<td>$\mu^+$</td>
<td>$\mu^+$</td>
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<tr>
<td>$\rightarrow \gamma$</td>
<td>$\rightarrow \gamma$</td>
<td>$\rightarrow \gamma$</td>
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</tbody>
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| $E_\gamma = 52.8$ MeV | $E_\gamma < 52.8$ MeV$^1$ | $E_\gamma < 52.8$ MeV$^1$ |
| $E_{e^+} = 52.8$ MeV | $E_{e^+} < 52.8$ MeV$^1$ | $E_{e^+} < 52.8$ MeV$^1$ |
| $\Theta_{e\gamma} = 180^\circ$ | $\Theta_{e\gamma} < 180^\circ$ | $\Theta_{e\gamma} < 180^\circ$ |
| $T_{e\gamma} = 0$ s | $T_{e\gamma} = 0$ s | $T_{e\gamma} \Rightarrow$ flat |
MEG II detectors

LXe
Scintillation Detector
4092 MPPCs + 668 PMTs

Measure:
\[ E_\gamma \sim (1\%) \]
\[ \Theta_\gamma \sim (2 \text{ cm}) \]
\[ T_\gamma \sim (70 \text{ ps}) \]

@ \( r = 68 \text{ cm} \)

Timing Counter

1024 plastic scintillator tiles with SiPM double-readout. Measure: \( T_e \sim (30 \text{ ps}) \)

Drift Chamber

1728 square drift cells
Measure electron track with 
\[ \sim 110 \text{um resolution:} \]
\[ E_e \sim (130 \text{ KeV}), \]
\[ \Theta_e \sim (5 \text{ mrad}) \]

Very good charge and time measurement on heterogeneous detector technologies while handling an high pileup environment:
How much a 8000 channel oscilloscope?
DRS 4 Digitiser

Analog switched capacitor array: analog memory with a depth of 1024 sampling cells
Developed at PSI for the MEG experiment, perform a “sliding window” sampling

500MSPS ↔ 5GSPS sampling speed with 11.5 bit signal-noise ratio
8 analog channels + 1 clock-dedicated channel for sub 50ps time alignment

- Pileup rejection
- Time measurement ~10ps
- Charge measurement ~0.1%

External trigger needed before data in signal cell is overwritten
→ 512ns maximum trigger latency at 2GSPS
Former MEG TDAQ

MEG DAQ and Trigger systems: active splitter for parallel trigger sampling @100MSPS
3000 DRS4 chn + 1000 Trigger chn fully independent from each-other
VME readout
5 Racks

Old Trigger + DAQ Systems
The new WaveDAQ

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- active splitter for parallel trigger sampling @100MSPS
- 3000 DRS4 chn + 1000 Trigger chn
- fully independent from each-other
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- 5 Racks

Fully integrated Trigger and DRS sampling:
- WaveDAQ system
  - fit MEG II in the same rack space
  - no more signal splitting
  - SiPM biasing by the frontend card
  - scale up to 16384 channels
  - GbE Readout

Old Trigger + DAQ Systems

New WaveDAQ System
WaveDREAM board

WaveDREAM: 16 ch Drs4 REAdout Module
Waveform digitiser with two DRS4 each with 80MSPS ADC for fast readout and parallel trigger sampling

Selectable frontend gain and PZC intensity

Additional fast analog comparator for online pulse timing

Piggy-back HV module up to 240V for SiPM arrays with integrated current readout

Can work in crate or standalone for 16ch tabletop DAQ with Gb Ethernet readout
Single board TDAQ

Single board **DAQ** software developed by PSI.
**HTML5-Ajax web interface** working at 60 fps with online Histogramming

Server software using Mongoose C/C++ Framework
- Easy low level calls for fast DAQ operations:
- Single executable with no need of dedicated http server

Wide use within and outside MEG II collaboration for small scale **prototype tests** and fast **signal checks**

Fully working demo: [http://elog.psi.ch/scope](http://elog.psi.ch/scope)
Programmable trigger

trigger based on discrimination on input waveform sum in preparation
Medium size system

Up to 16 WaveDREAMs fit in a custom designed **3U crate** (256 channels) with hardware compensated **Clock distribution** and shared LVDS **Trigger signal**. Crate management board with **MIDAS Slow Control Bus** node and **SPI interface** to boards.

Trigger combination by means of Kintex 7 **Trigger Concentrator FPGA Board** using low latency **serial links**, up to 64 trigger lines involving **charge** and **time** algorithms.

Shared **readout** through **1/10Gb** interfaces on Zynq 7 SoC in the **Data Concentrator Board (DCB)**
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Bigger systems

Bigger systems?

- Additional aggregation layers by TCBs using High Speed LVDS cables
- Reuse existing hardware when possible

- 16:1 inside crate
- 4:1 through trigger cables
- (FCI Densishield)
- 16:1 inside trigger crate

The Ancillary system distributes trigger and clock signals through the system with <10ps jitter on clock up to 16384 channels

Re-use existing hardware when possible

Online PCs... Up to 64 crates...
MEG II system: installation ongoing...

- 8 WDB crates
- ~100 boards, 1600 channels
- Trigger crate
  - 3 TCB slaves + Master
- Trigger and CLK distribution crate
MEG II Timing Counter Test Beam

Tested with final detector and full MEG II beam intensity (8 \times 10^8 \mu/s):
- 256 scintillating tiles, 512 readout chn. (two crate system)
- 2 Auxiliary Laser chn. for monitoring
- Trigger on single tile (coincidence of two tile channels) select positron tracks

Offline DRS4 analysis: Time resolution scales as square root of hit multiplicity with electronic contribution on the order of 10ps/chn

\[ \chi^2 / \text{ndf} = 8.537 / 3 \]
\[ \text{single} = 92.62 \pm 0.6224 \]
\[ \text{const} = 0 \pm 3.032 \]

Electronic contribution not relevant
Online time resolution

Each discriminator input digitised @640MHz by ISERDES primitive

8 sample bit “waveform” each clock cycle then encoded in the FPGA

Theoretical resolution
1.56ns / sqrt(12) rms resolution each channel -> 320ps

In TC Test Run:
single tile resolution ~415 ps
MEG II LXe detector Test Beam

Subset of channels (4 crates) tested with photons from muon beam and calibration sources

Complete trigger **sum, calibration, threshold** and **veto** implemented with overall latency of 700ns

→ will be soon improved by ~200ns

DRS MPPC channel

Trigger latency

Signal digitised

Trigger stops

DRS

“-1” calibration value to have positive waveforms
Getting 1Gb/s line speed

Distributed network load (to avoid packet drops by network switch)
dedicated parameters to handle WDB data generation
- inter packet delay
- first packet delay

*Layer of CISCO 110 switches to collect packets to online machine

Multi threaded DAQ SW
Any of the thread can be parallelised
- data collection
- event building
- DRS waveform calibration
- data write to disk

Data [MB/s] 110.114
Learned tips to go beyond 1Gb/s

**Initial:** 155kpackets/s max
- Lock on CPU #0
- 180kpackets/s max
- Read multiple packets at once
- 460kpackets/s max
- "Jumbo" frames

**Current:** “only” 352kpackets/s, (5.4 Gbps) at full throttle

Switch
CISCO Catalyst 3850

DAQ pc
other pc
Beam monitor application

- Two layers of relatively orthogonal scintillation squared 500µm fibres
- Signal discrimination of WDBs and coincidences of any respective fibre on TCB
  - Beam profile and intensity requires 10sec of DAQ (other std methods: 1-2hours)

WaveDAQ used “just” as programmable scaler

preliminary: pure rates coincidences + accidentals
Application outside MEG II

Measuring ion fragmentation cross sections for proton therapy simulation improvement

Single crate WaveDAQ has been selected to readout TOF Wall detector (good time and charge resolutions needed)

40 Plastic Scintillator bars 2x0.3x44 mm with SiPM readout at both edges

+ Start counter: thin plastic detector read by 8 SiPM

+ BGO calorimeter: 320 projective crystal read by SiPM

Prototype bars tested on beam at CNAO (IT) with standalone WaveDREAM board
Conclusions

A new TDAQ system “WaveDAQ” has been designed by PSI and INFN accounting for the needs of MEG II upgrade:

- DRS4 digitizers
- 10-ps timing with full waveform digitization
- Full FPGA trigger processing with online amplitude and time algorithms
- SiPM power supply and onboard amplification
- Ethernet readout

System performances tested with MEG II detector, final 8000 chn. system will be ready in 2021.

Already application to other particle experiments (FOOT) and lab tests, simple and easy to deploy digitisation for everyone needing charge and time measurement with high pileup rejection.
Backup
The crate

**Crate Management Board (CMB):**
- power supply 24/300W
- fan and temperature control
- Power cycle each slot
- FPGA FW upload
- ethernet remote control
Trigger Links

Low latency serial connection are mandatory to keep a low latency trigger

Serial links have been implemented using ISerdes/Oserdes primitive by Xilinx

MultiGigabit GTX transceiver have been discarded due to the high intrinsic latency

8 links each with a serialisation ratio of $8 = 64$ bit/clock
The crate: CLK distribution

CLK distribution with skew kept below 5 ps within each slot