Intermodular Configuration Scrubbing of On-detector FPGAs for the ARICH at Belle II

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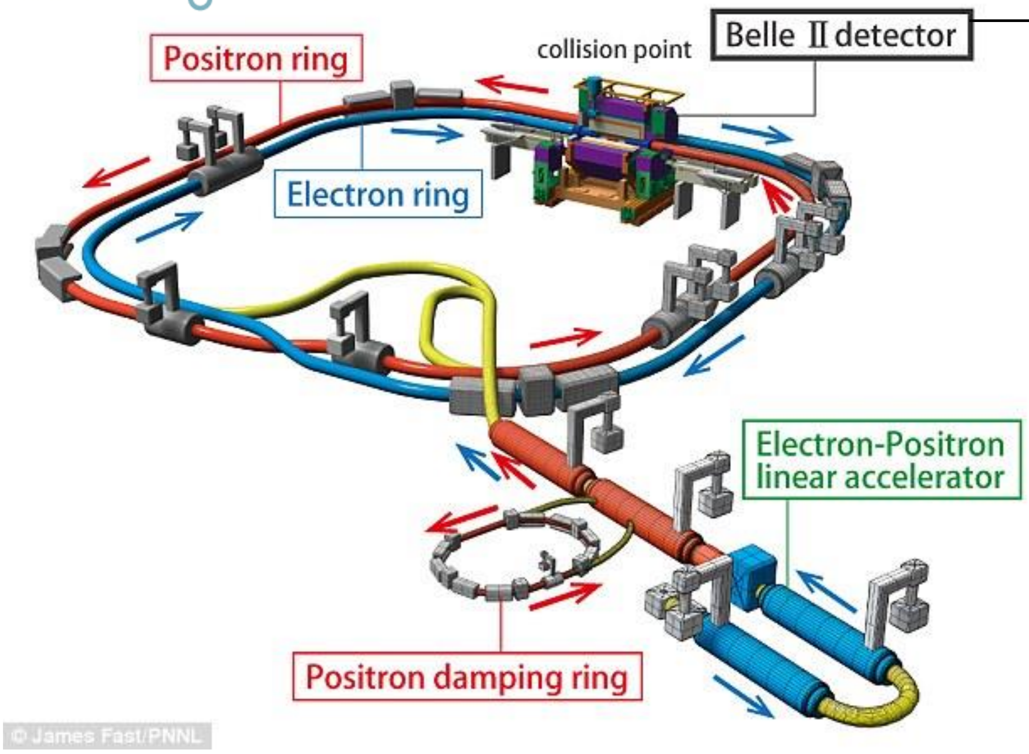
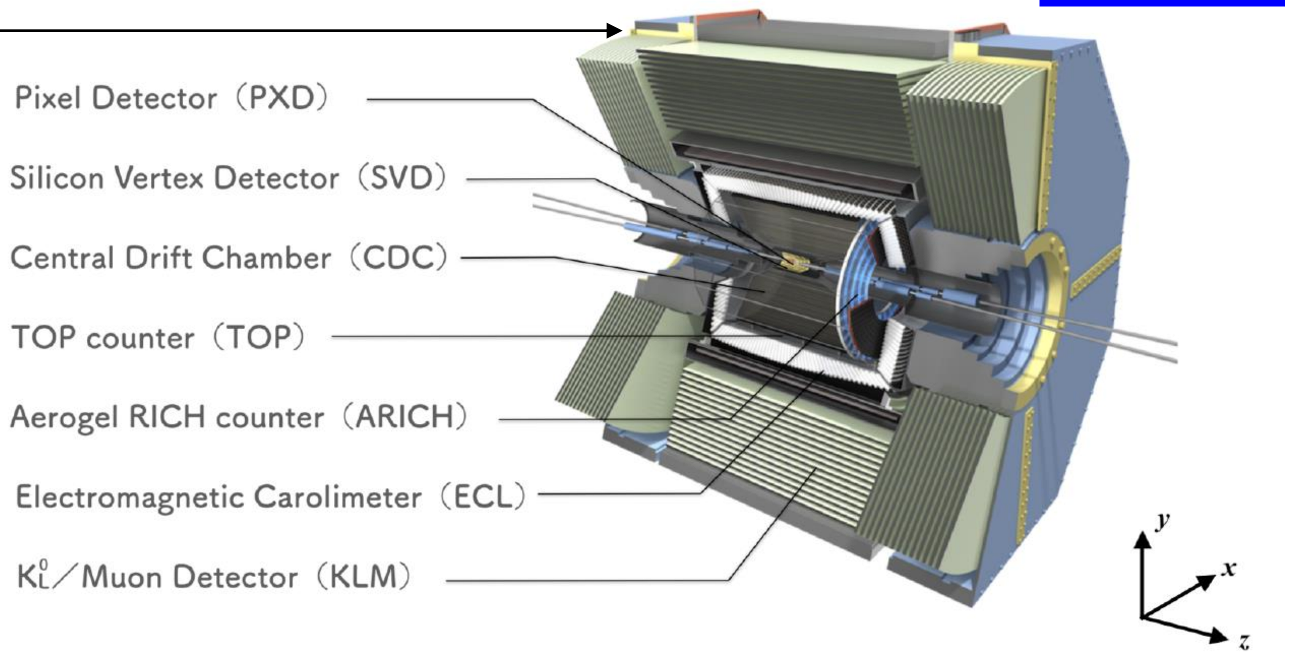
Outline

- SuperKEKB, Belle II and ARICH
- Single event upsets in ARICH front-end boards
- The Configuration Consistency Corrector
- Irradiation test results
- Conclusions

SuperKEKB and Belle II





2013/July/29	LER	HER	unit
E	4.000	7.007	GeV
I	3.6	2.6	A
Number of bunches	2,500		
Bunch Current	1.44	1.04	mA
Circumference	3,016.315		m

SuperKEKB e^+e^- B factory @ KEK (Tsukuba, Japan)

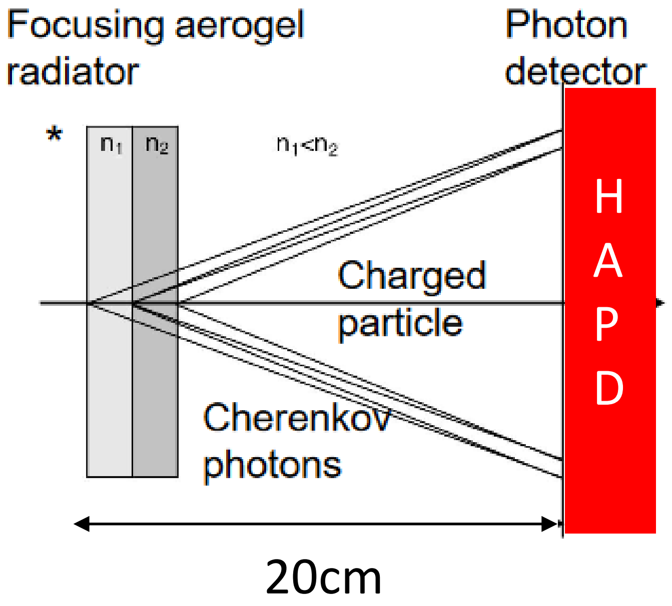
Design parameters

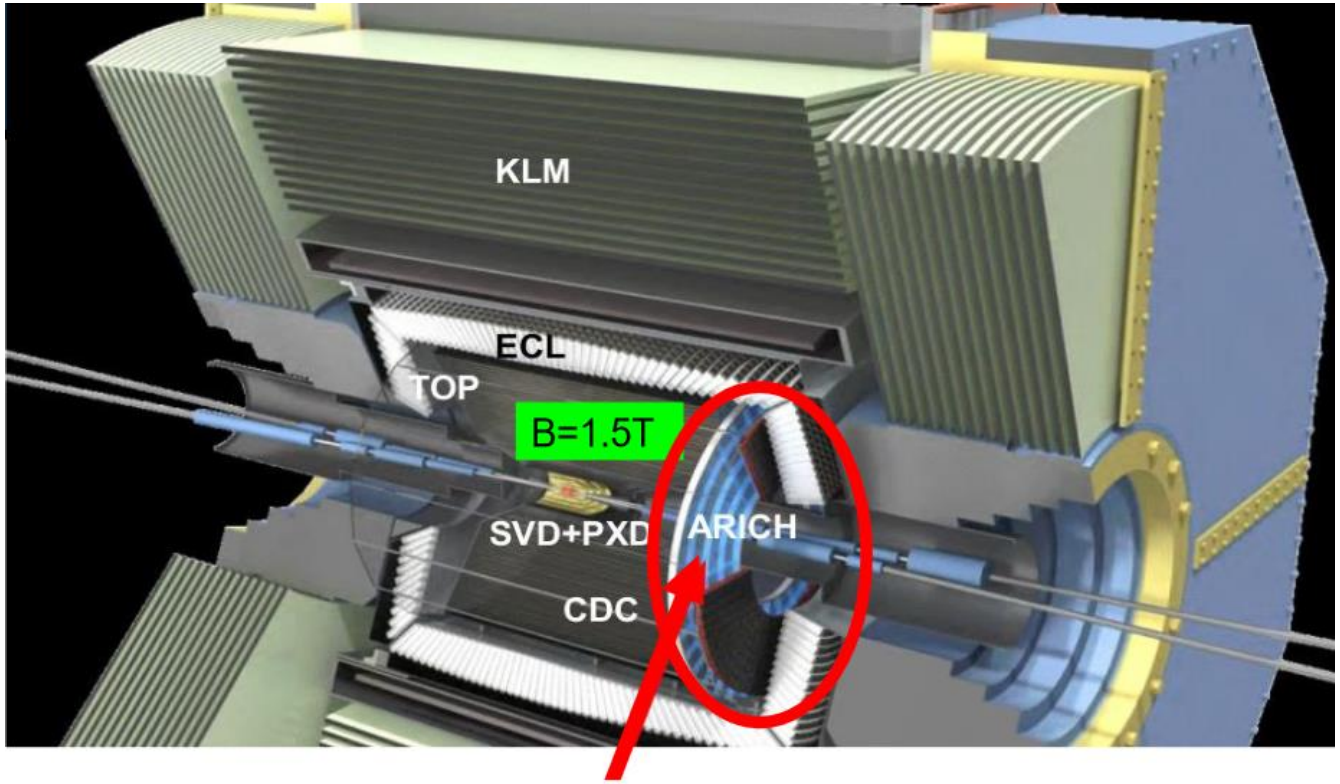
- Target L= 8×10^{35} cm^{-2} s^{-1}
- LER 4 GeV (e^+), HER 7 GeV (e^-)

- Belle2 detector at beam collision point
- Physics beyond the Standard Model at the intensity frontier
  - CKM matrix elements, CPV studies, rare B,D, τ decays and more

Aerogel Ring Imaging CHerenkov Counter

- Goals
  - Particle Identification in end cap
  - K/π separation > 4σ in momentum range 1-3.5 GeV/c
- Requirements
  - operation in 1.5T magnetic field
  - limited available space ~280 mm
  - radiation hardness
    - 1MeV eq. neutron fluence: 10^{12} n/cm^2
    - Total ionizing dose: 1 kGy

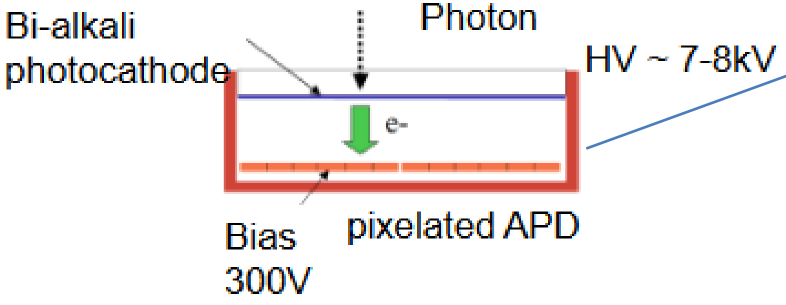




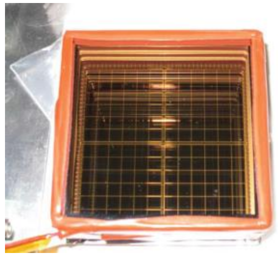
- Proximity focusing aerogel RICH
  - <n> ≈ 1.05
  - θc(π) ≈ 307 mrad@ 3.5 GeV/c
  - θc(π) –θc(K) = 30 mrad@ 3.5 GeV/c
  - pion threshold 0.44 GeV/c, kaon threshold 1.54 GeV/c

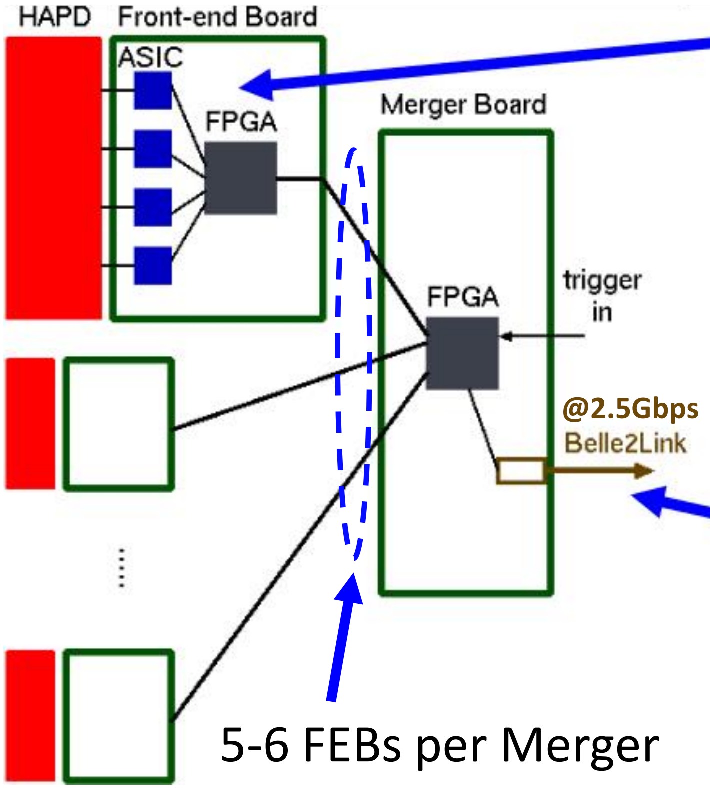
Photon Detector & Readout Electronics

- 420 x 144-channel Hybrid APDs
  - Custom design with Hamamatsu



Specifications	
Package	73×73mm2
sensitive area	64%
# of pixels	144(36×4chips)
capacitance	80pF
weight	220g
peak QE	28%
bombardment gain	1500
avalanche gain	~30
total gain	~45000

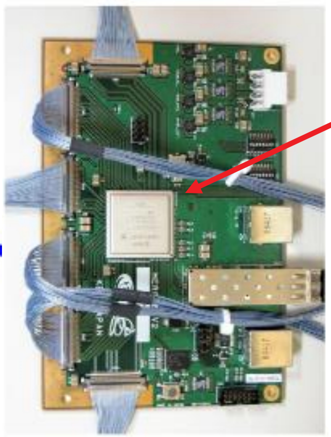




5-6 FEBs per Merger

Front-end Board

Spartan-6 LX45



Virtex-5 LX50T

Merger Board

- Mergers aggregate data from FEBs to Belle2Link and manage FPGA configuration via JTAG

Configuration SEUs in FEB FPGAs

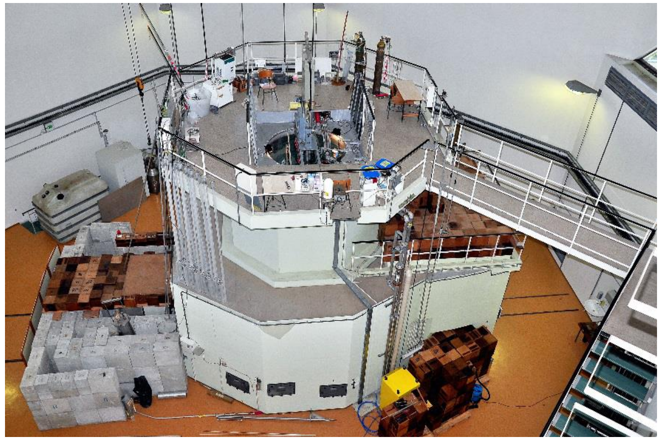
- Spartan-6 devices use Boron as p-type dopant
- B^{10} (20%) has a high σ for thermal neutron capture => single event upsets (SEUs) in configuration SRAM

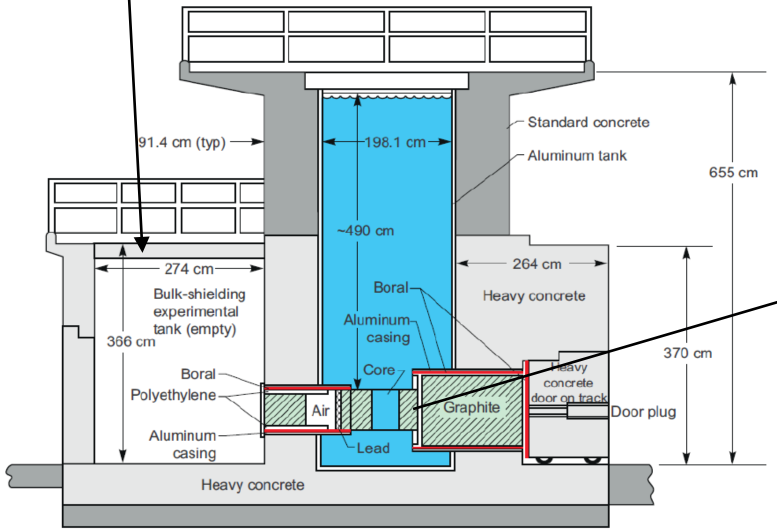
$$\left.\begin{array}{ll} {}^{10}B + n \rightarrow {}^{7}Li + \alpha + \gamma & (94\%) \\ \qquad\quad \rightarrow {}^{7}Li + \alpha & (6\%) \end{array}\right\} \text{3.5 kbarns}$$

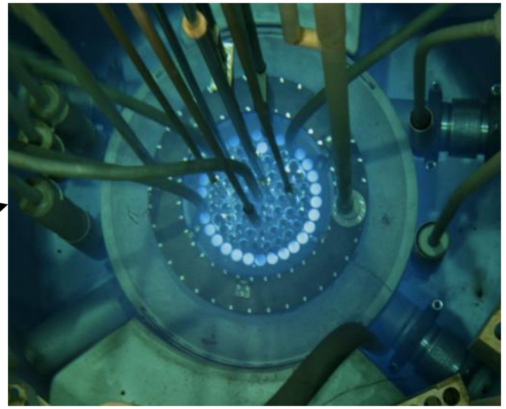
- Previous irradiation tests at the TRIGA reactor of Jožef Stefan Institute (Ljubljana, Slovenia)
  - 250 kW research reactor from General Atomics
  - 10^7 n/(cm^2·s) in dry room
  - neutron spectrum similar to Belle II spectrometer
  - extrapolation at Belle II: 8 SEU/h per board, or 3.3 kSEU/h overall
- In October 2019 runs, nearly 5% of front-end FPGAs were affected by configuration SEUs in 24 hours

Dry room for irradiation

TRIGA layout

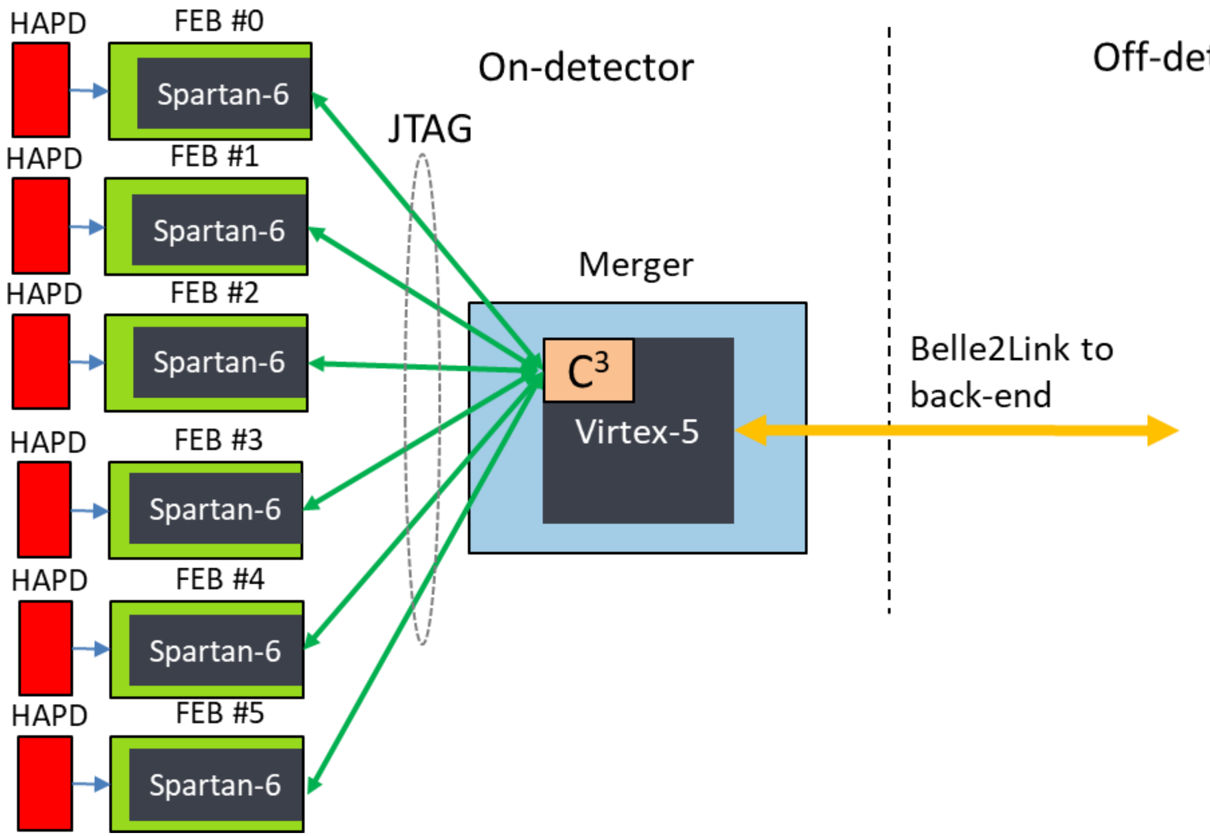




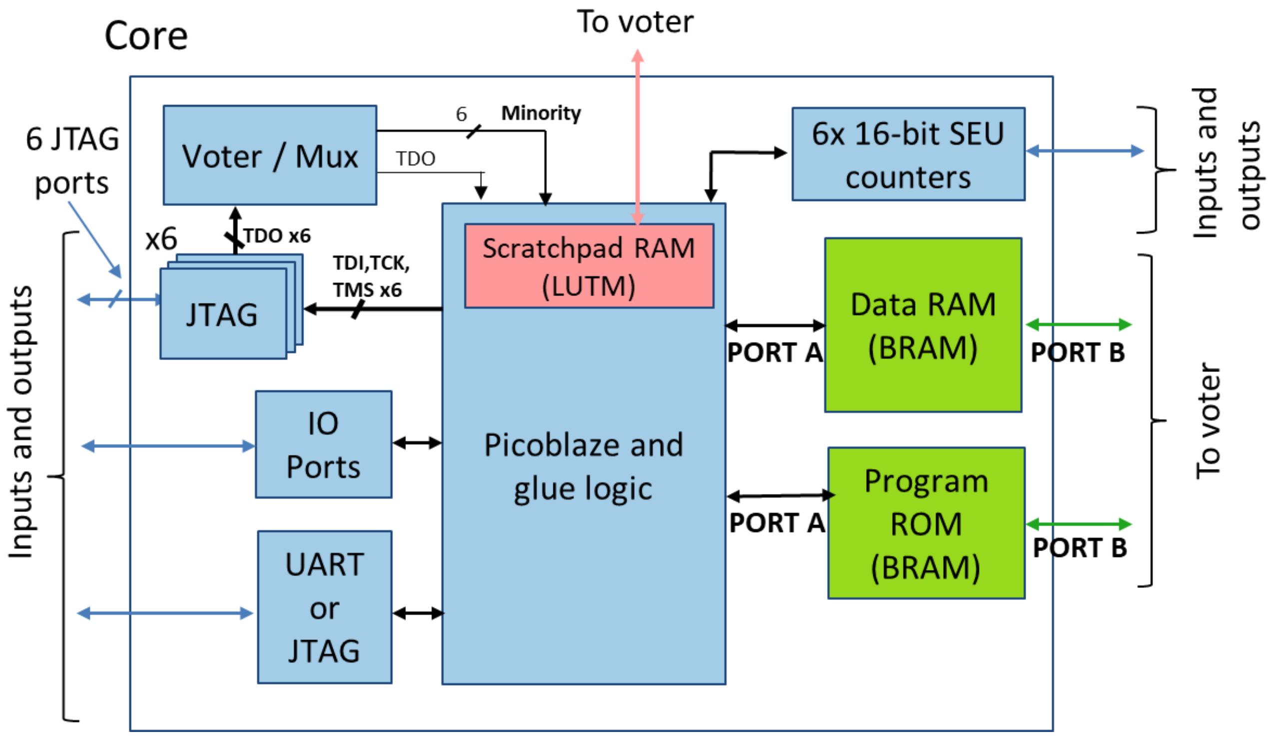


Repairing FEB Configuration On-the-fly

- Star read-out topology
- FEB FPGAs are programmed with the same bitstream => redundancy at system-level
- Idea
  - Parallel readback of FEB (Spartan-6) configuration from Merger (Virtex-5)
  - Real-time 4-out-of-6 bitwise majority voting on JTAG streams (TDOs) for error detection
  - Quick single frame reconfiguration for error correction



The Configuration Consistency Corrector - C^3

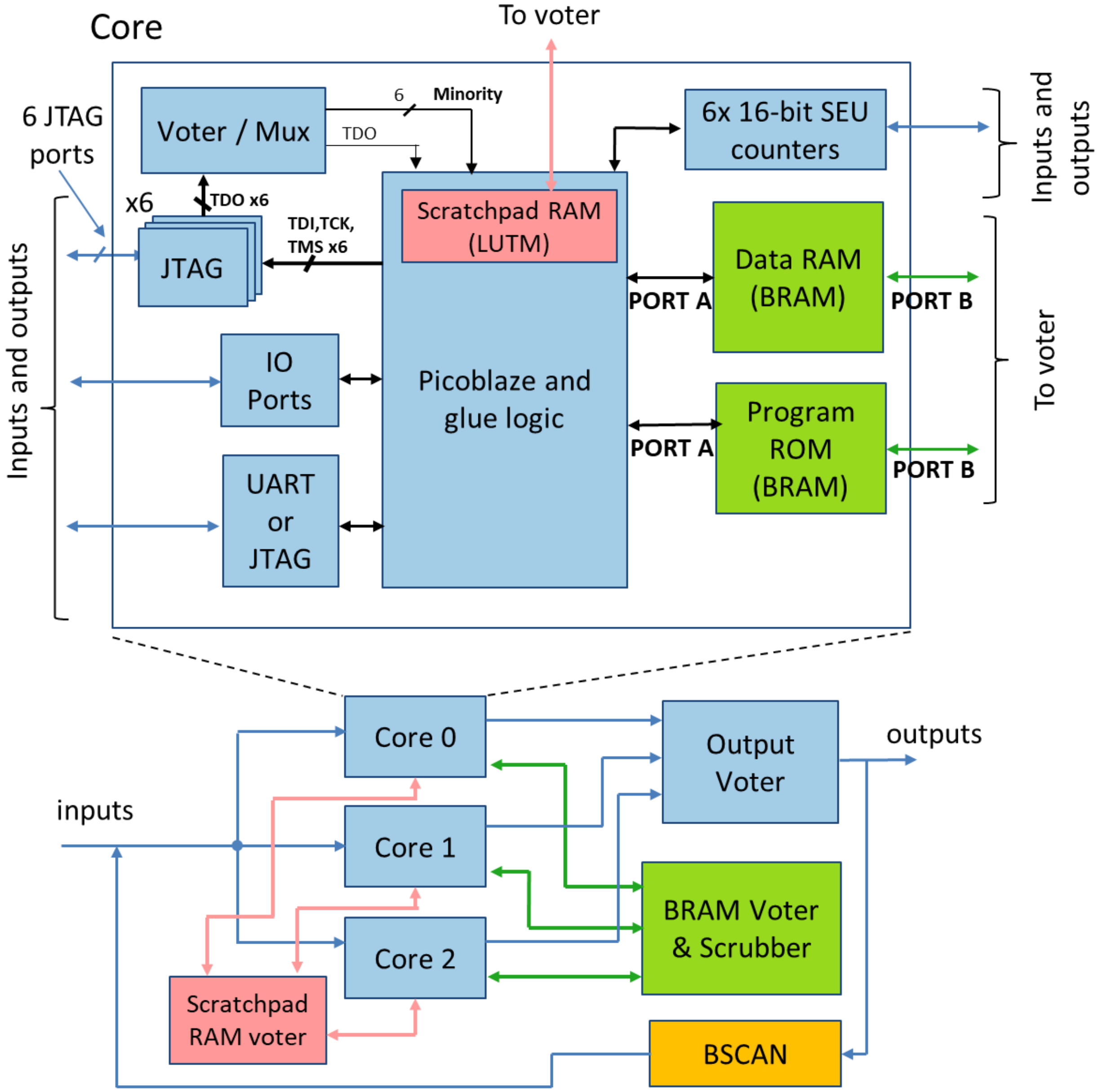


- Features
  - Majority voting configuration of up to 6 FPGAs streams
  - built around Xilinx PicoBlaze6 processor
  - runs at 127 MHz (Belle2Link clock in Merger)
  - 3.3s scrubbing period
  - ~1 ms single frame repair time
- 6 JTAG ports, two IO modes
  1. Single-port Read/Write (used for configuration repair)
  2. All ports Voted Read / Broadcast Write (used for readback)
- BRAMs store
  - Frame buffers (260x8b)
  - Target FPGA frame addressing device-specific information (1252x8b)
  - uP Program (4096x18b)
- 16-bit upset counter for each target FPGA
- UART or JTAG IO for debug/control

- No memory needed for golden bitstream and no a priori limit on # of bitflips per frame that can be repaired
- Xilinx Soft Error Mitigation (SEM) controller in Spartan-6 is limited at 1 bitflip per frame

Architecture derived from
R. Giordano et al., “Configuration Self-Repair in Xilinx FPGAs,” doi: 10.1109/TNS.2018.2868992
R. Giordano et al., “Custom Scrubbing for Robust Configuration Hardening in Xilinx FPGAs,” doi: 10.3390/instruments3040056

The Configuration Consistency Corrector – C³ (2)



- Triple Modular Redundancy for logic and scrubbing for BRAMs and scratchpad
- Periodic reset of uP for internal registers cleanup
- Runs in background, no disruption of user design implemented in FPGA
- UART for scrubber control and logging of upsets details

Scrubbing Logs

Extract from upset logs

FPGA no.
0 to 5

frame address

Bit offset

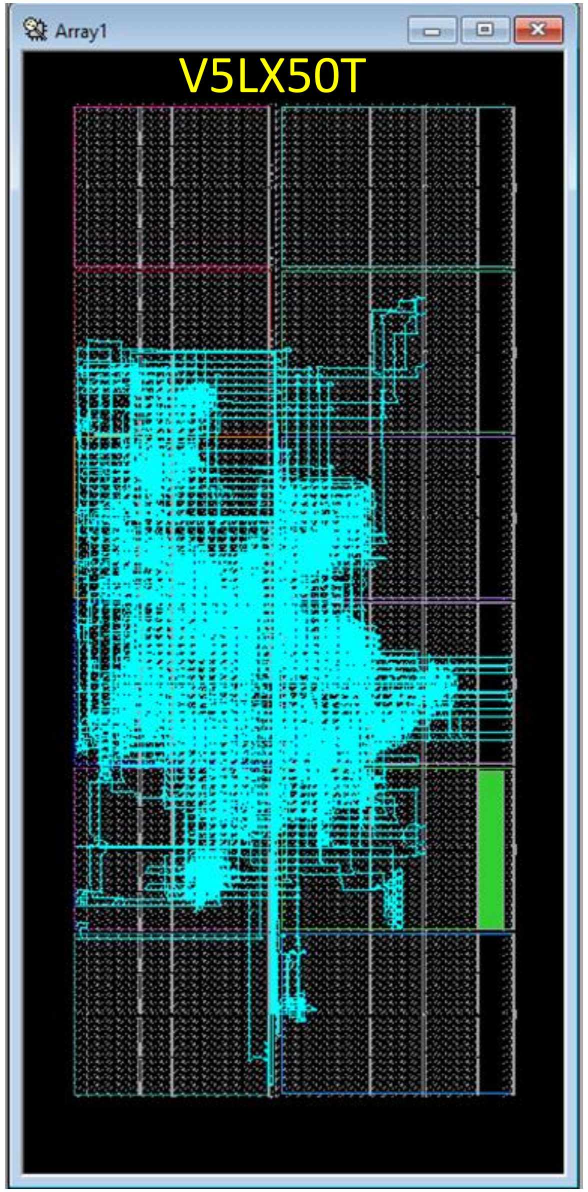
Upset polarity

```
04> V
BEGIN_VOTING
5D3F02C6.045253 FPGA 02 FRAD 0x030D001C 0 000D:0->1 01CD:0->1
5D3F02C6.054449 RDCHECK_COMPLETE
5D3F02C7.049A29 RDCHECK_COMPLETE
04> V
BEGIN_VOTING
5D3F02CA.02A464 FPGA 02 FRAD 0x000B001C 0 00D1:0->1 0116:1->0 024E:0->1
5D3F02CA.0EF51B RDCHECK_COMPLETE
02> V
BEGIN_VOTING
5D3F02CE.08C5A7 FPGA 01 FRAD 0x00070007 0 025B:0->1 0263:0->1
5D3F02CF.06CE5F RDCHECK_COMPLETE …
```

detection time stamp (unix time hex)

- For each upset, the C^3 sends a text line on UART with
  - unix time stamp, FPGA no., frame address, bit offset(s), polarities
- Very useful for testing and debugging, but the same info could be used to study correlations with of upsets to the radiation environment or to reset FEBs only when essential bits are hit

C^3 firmware standalone



Implementation

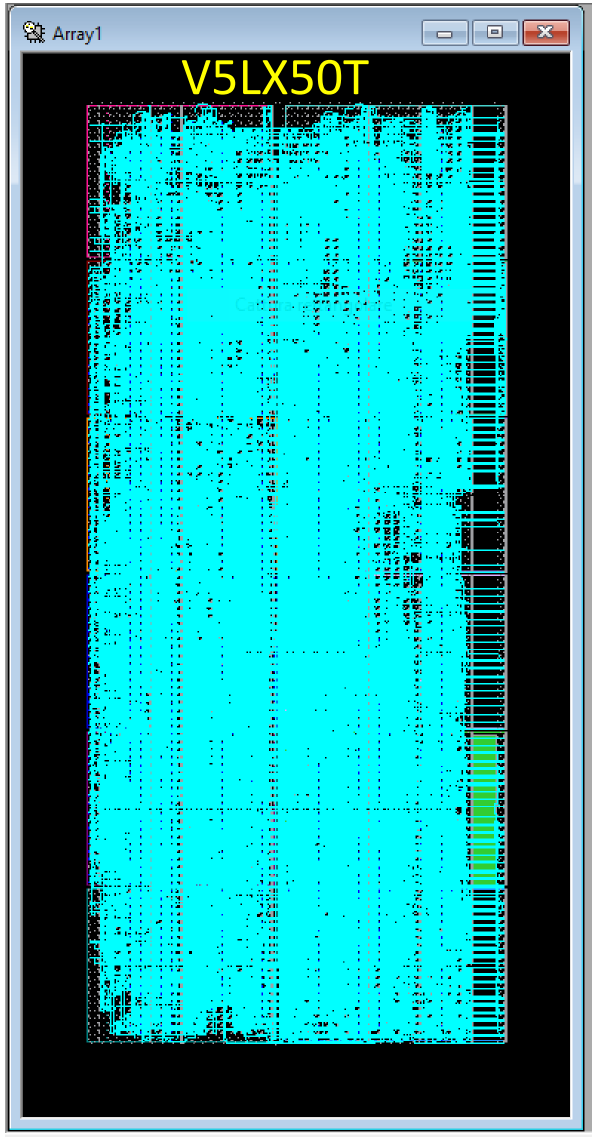
- C^3 has a small logic footprint
- In V5LX50T just 828 slices (11%) and 9 BRAMs (15%)

C^3 firmware standalone

Logic Resources	Used	Available	%
Slices: FFs	1,068	28,800	3
Slices: LUTs	2,005	28,800	6
Slices: overall	828	7,200	11
BUFGs	3	32	9
BRAM 36k	9	60	15
BSCAN	1	4	25

Implementation (2)

Readout + C^3 firmware

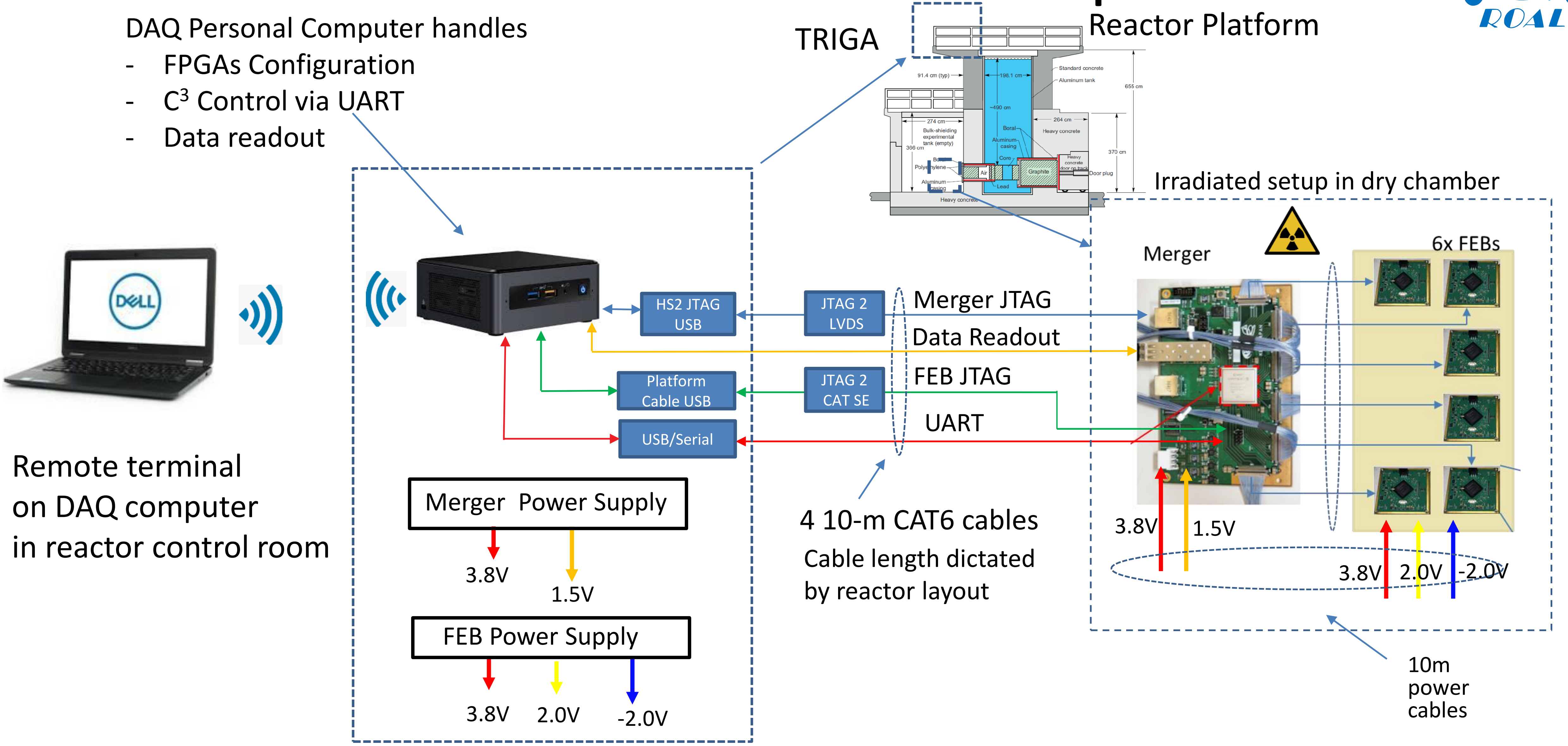


Readout + C^3 firmware

Logic Resources	Used	Available	%
Slices: FFs	14,932	28,800	51
Slices: LUTs	16,159	28,800	56
Slices: overall	5,977	7,200	83
BUFGs	10	32	31
BRAM 36k	35	60	58
BSCAN	1	4	25

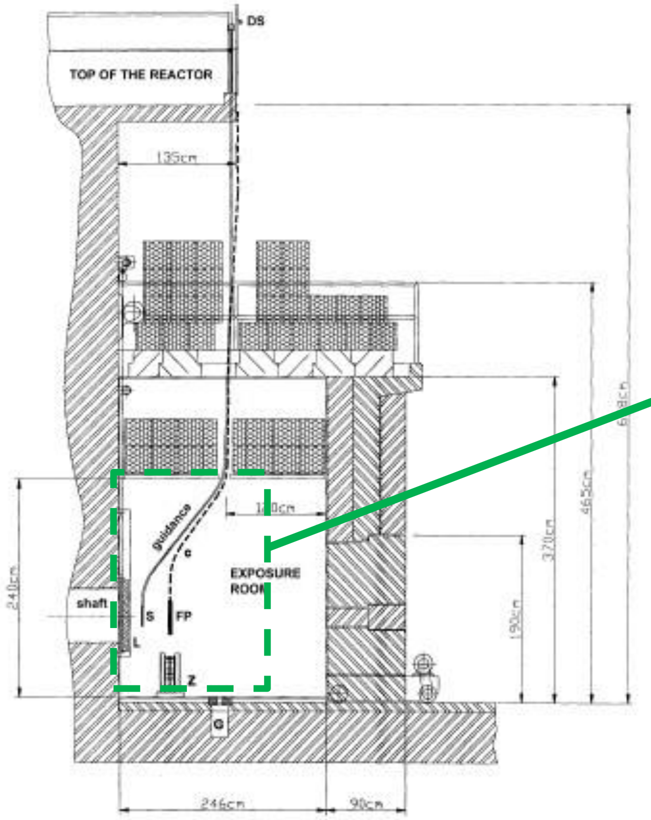
- Implementation of Merger firmware w/ C^3
- Fits V5LX50T resource availability
  - Slices at 80%, BRAMs at 58%

Irradiation Test Setup



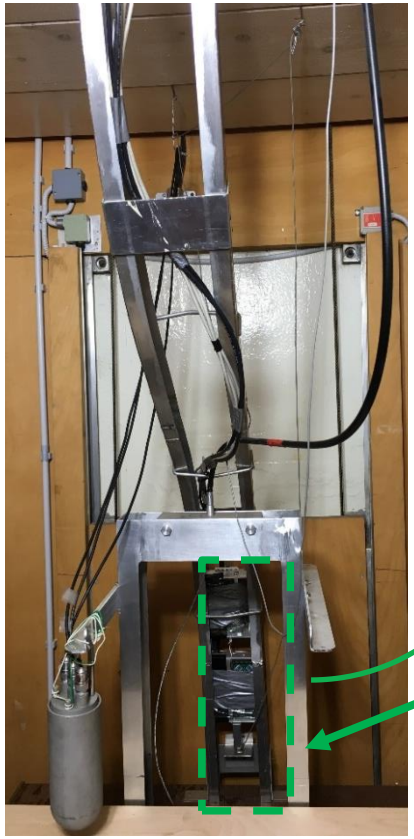
Dry Chamber

Reactor Platform



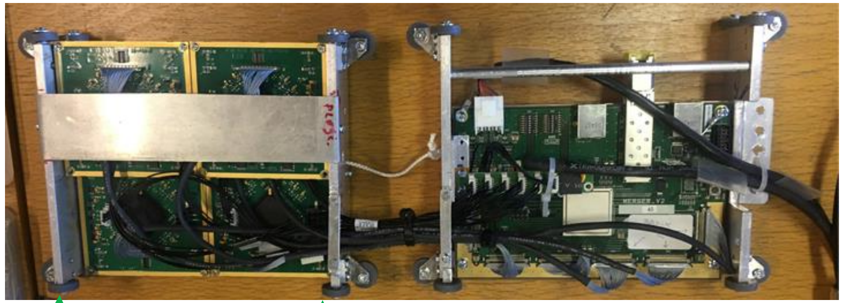
Dry chamber section

Sledge



6 FEBs: 2 layers
Bottom 4, top 2

Merger



90°

trays

- Prepared two chained trays: one w/ Merger & one w/ 6 FEBs
- Sledge for sliding DUTs in and out irradiation channel for quick irradiation start/stop
- Reactor always on during test

Test Results: Cross Sections

- 29 runs, total irradiation time 14 hours, on average 29 minutes per run

$$\sigma = \frac{\mathrm{N_{events}}}{\Phi}$$

Description	Value
Total # of C3 failures	10
Total # of upsets (bitflips) in 6 FEBs	$3.8 \cdot 10^5$
Average upsets rate detected by C3 per FEB (1/s)	1.26
Mean # upsets per FEB	$6.3 \cdot 10^4$
Total # of upsets Merger	$1.1 \cdot 10^3$
Mean # of upsets per 6 FEBs between C3 failures	$3.8 \cdot 10^4$
Mean # of upsets per FEB between C3 failures	$6.3 \cdot 10^3$
Mean # of upsets per Merger between failures	$1.1 \cdot 10^2$

Failure cross section

$$\frac{\sigma_{C3}}{\sigma_{FEB}} = 1.6 \cdot 10^{-4}$$

upset cross section

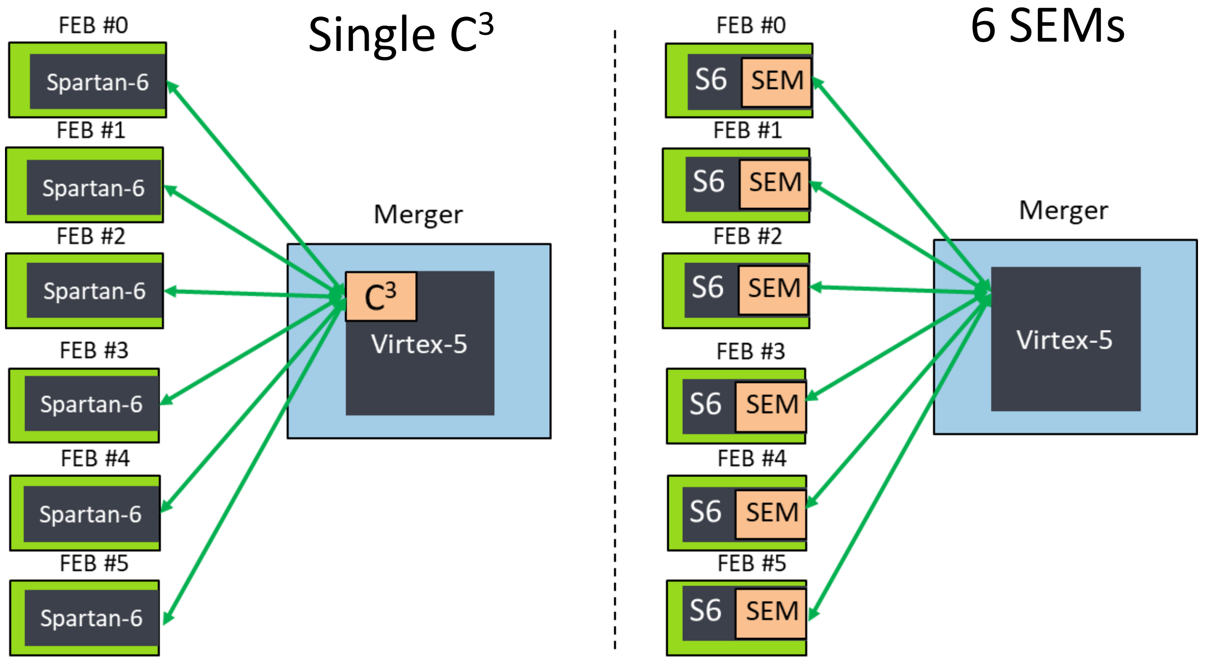
Upset cross sections

$$\frac{\sigma_{MERGER}}{\sigma_{FEBs}} = 1.7 \cdot 10^{-2}$$

Assuming same neutron fluence on merger and FEB

Impact on Readout: C^3 Vs SEM

- Failure defined as readout interrupted or data corrupted
- Two sets of runs
  - A single C3 implemented in Merger
  - A SEM implemented in each FEB (total of 6 SEMs)

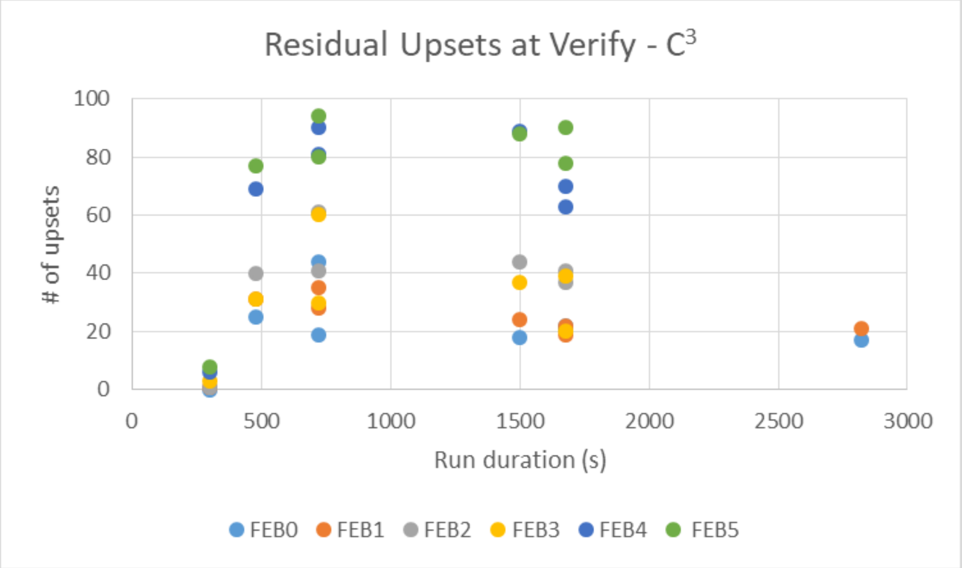


Test summary	C^3 in Merger	SEMs in FEBs
# of runs w/ readout testing	13	11
Test time (h)	8.0	4.8
# of read out failures	13	10
Average upset rate per FEB (1/s)	1.26	1.26
Readout MTBF (s)	$2.2 \cdot 10^3$	$1.7 \cdot 10^3$
Readout MTBF (upsets)	$2.8 \cdot 10^3$	$2.2 \cdot 10^3$

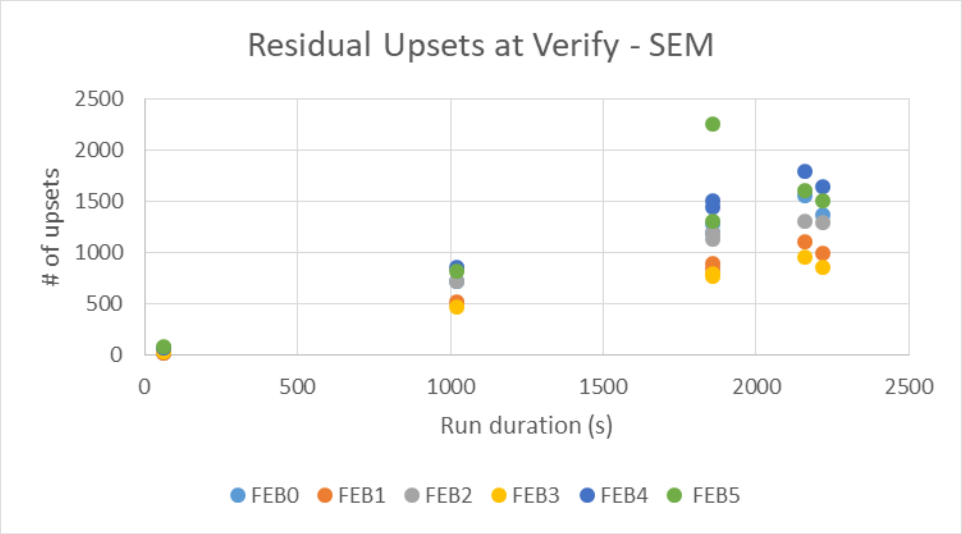
$$\frac{MTBF_{C3}}{MTBF_{SEMs}} = 1.3$$

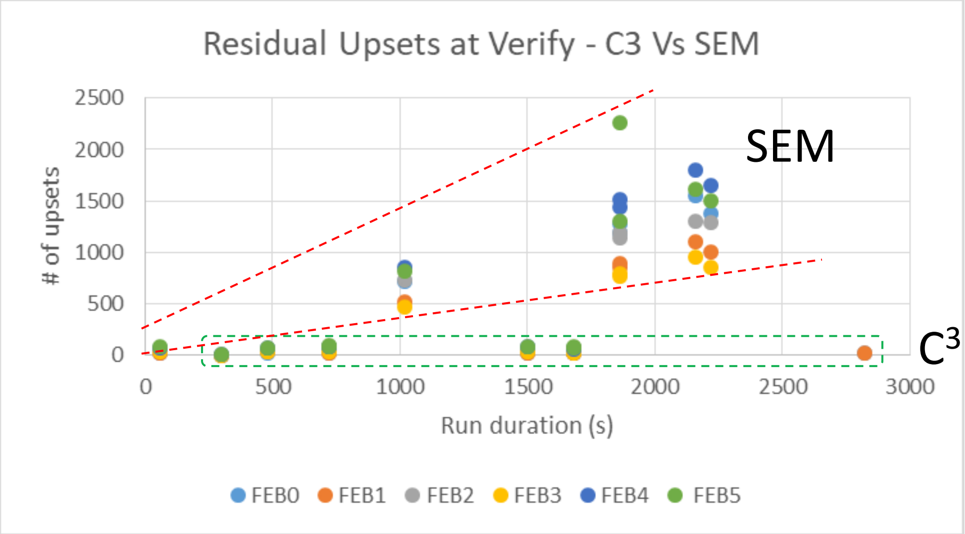
30% improvement moving from SEM to C^3

Upset Correction Capability: C^3 vs SEM

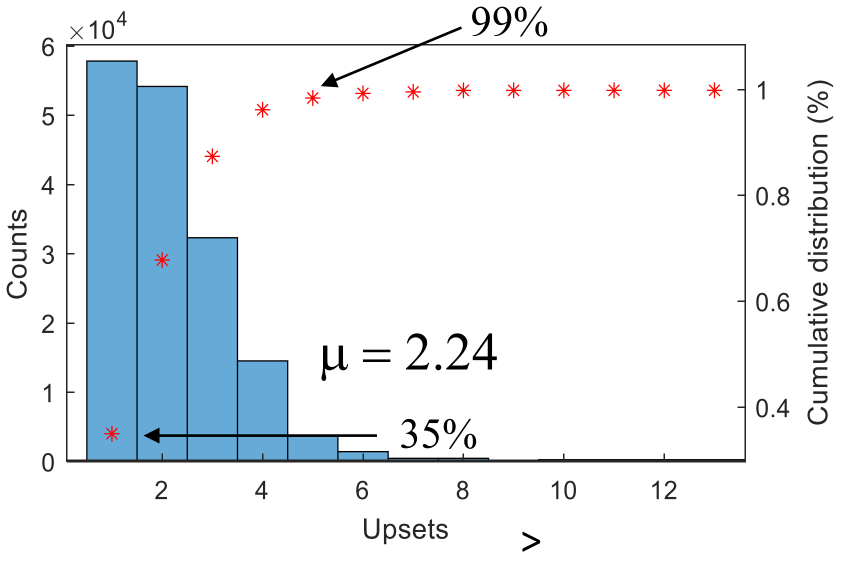


- Residual upsets in FEBs at the end of the run
- SEM lets upsets accumulate over time
- C^3 avoids accumulation
  - Small amount residual related to stop (or failure) of C^3 at the end of the run before verify

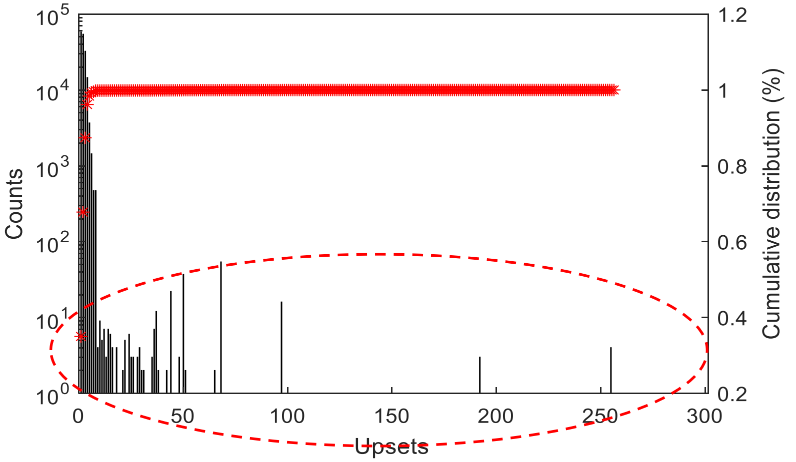




Number of Upsets per Frame



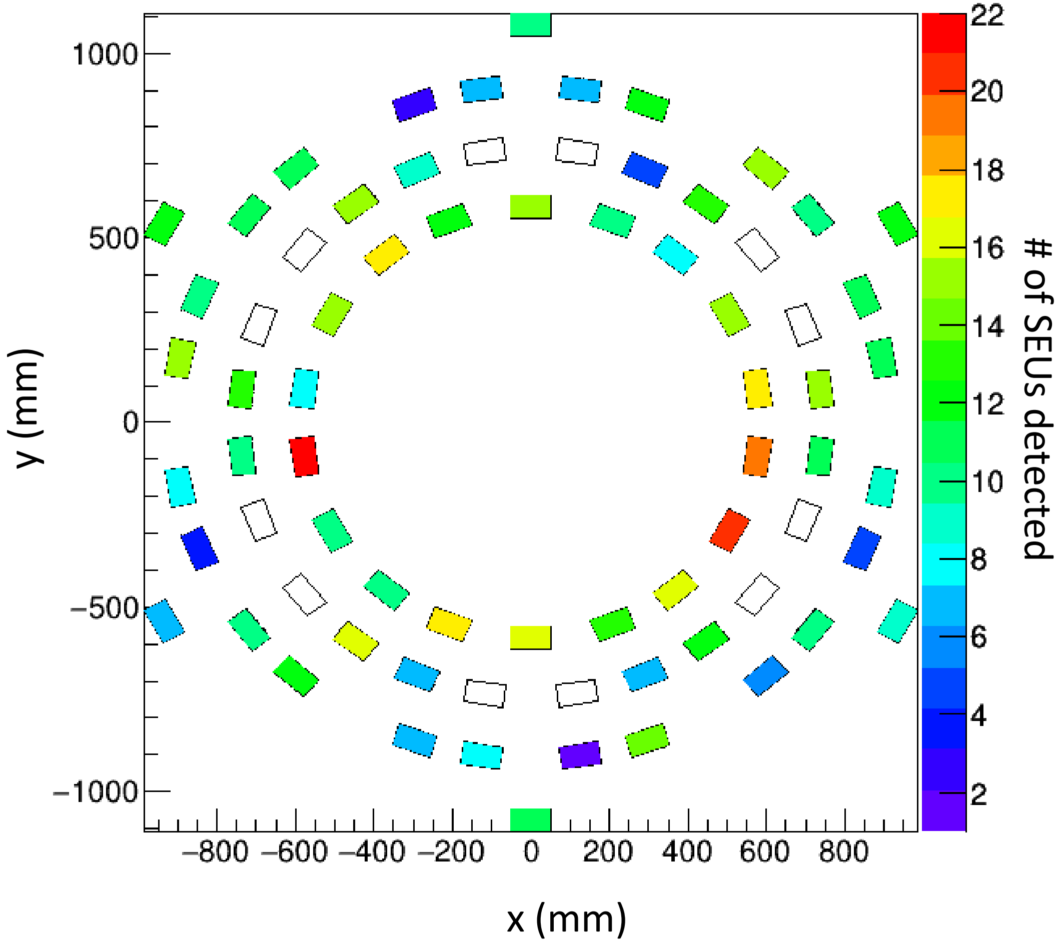
Notice the log scale



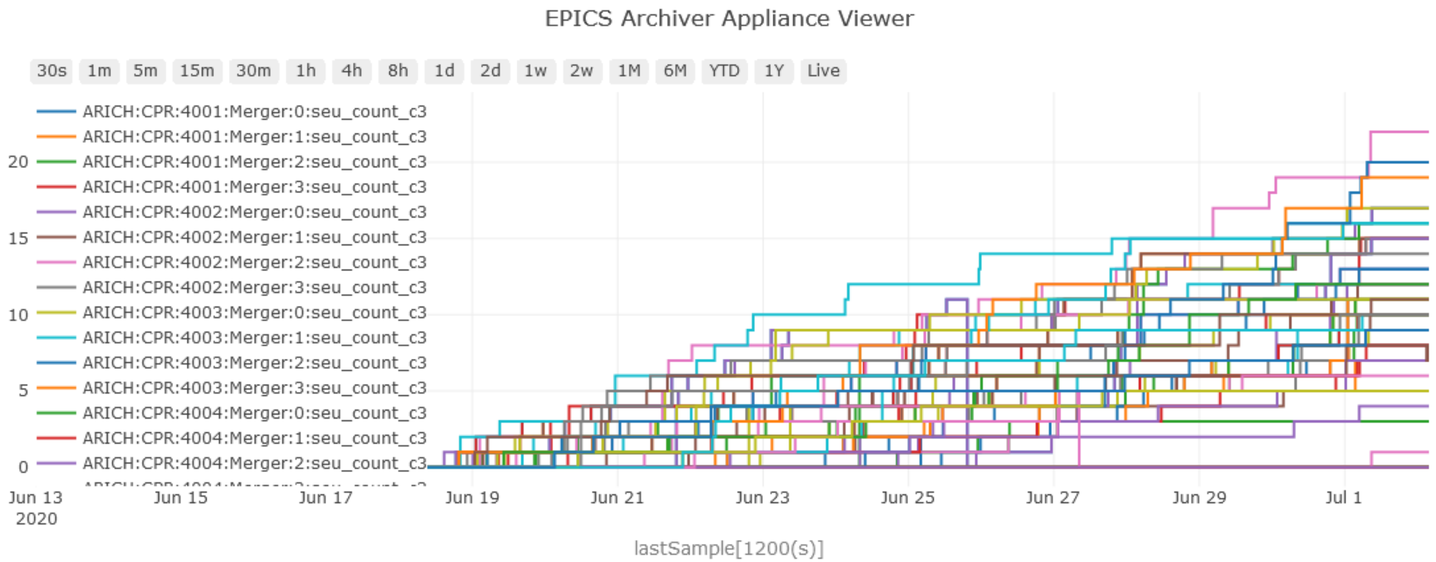
- Distribution of the number of bitflips per frame (multiplicity) in each SEU event detected by C3
- Average multiplicity 2.24 upsets per SEU event
- 65% of events have multiplicity > 1 (not correctable by SEM)
- Total events 165k
- Includes also few tens of events w/ up to 256 flips, likely configuration SEFIs

Integration in Belle II

SEU map of FEB groups



- C^3 fully integrated and running in Belle II TDAQ since the middle of 2020 spring run
- SEUs monitored via EPICS slow control system
  - Detected SEU map and SEU trends related to last two weeks of 2020 spring run
  - Up to 20 SEUs per FEB group
- FEB firmware is now robust against SEUs, in the view of SEU rate increase with the foreseen SuperKEKB luminosity increase ($2 \cdot 10^{34}$ -> $8 \cdot 10^{35}$ cm^{-2} s^{-1})



Conclusions and…

- Developed a scrubber (C^3) to majority vote configuration across FPGAs connected in a star topology
- Fast detection by means of parallel readback and correction by partial reconfiguration
- Completed a radiation test at a nuclear reactor
- Results show
  - σ of upsets in Merger almost two order of magnitude lower than in FEBs
  - σ of failures in C^3 almost four orders of magnitude lower than upset σ in FEBs
  - C^3 limits accumulation of upsets in configuration memory and improves MTBF of data read out w.r.t. Xilinx SEM by 30%
  - No hard failures of Merger (Virtex-5) or FEBs (Spartan-6)
- System installed and fully operational in Belle II

…Acknowledgments

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  - A. Boiano, A. Vanzanella, A. Pandalone, E. Masone from SER (Electronics and Detectors Service) of INFN Napoli for their technical support to this activity

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Jožef Stefan Institute