Intermodular Configuration Scrubbing of On-detector FPGAs for the ARICH at Belle II

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Outline

• SuperKEKB, Belle II and ARICH
• Single event upsets in ARICH front-end boards
• The Configuration Consistency Corrector
• Irradiation test results
• Conclusions
SuperKEKB and Belle II

SuperKEKB e⁺e⁻ B factory @ KEK (Tsukuba, Japan)

Design parameters
- Target $L = 8 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$
- LER 4 GeV (e⁺), HER 7 GeV (e⁻)

- Belle2 detector at beam collision point
- Physics beyond the Standard Model at the intensity frontier
  - CKM matrix elements, CPV studies, rare B,D, τ decays and more

### Table: Design Parameters

<table>
<thead>
<tr>
<th>2013/July/29</th>
<th>LER</th>
<th>HER</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>4.000</td>
<td>7.007</td>
<td>GeV</td>
</tr>
<tr>
<td>I</td>
<td>3.6</td>
<td>2.6</td>
<td>A</td>
</tr>
<tr>
<td>Number of bunches</td>
<td>2,500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bunch Current</td>
<td>1.44</td>
<td>1.04</td>
<td>mA</td>
</tr>
<tr>
<td>Circumference</td>
<td>3,016.315</td>
<td></td>
<td>m</td>
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</tbody>
</table>
Aerogel Ring Imaging CHERENKOV Counter

- **Goals**
  - Particle Identification in end cap
  - K/π separation > 4σ in momentum range 1-3.5 GeV/c

- **Requirements**
  - operation in 1.5T magnetic field
  - limited available space ~280 mm
  - radiation hardness
    - 1MeV eq. neutron fluence: $10^{12}$ n/cm$^2$
    - Total ionizing dose: 1 kGy

- Proximity focusing aerogel RICH
  - $\langle n \rangle \approx 1.05$
  - $\theta_{c(\pi)} \approx 307$ mrad@ 3.5 GeV/c
  - $\theta_{c(\pi)} - \theta_{c(K)} = 30$ mrad@ 3.5 GeV/c
  - pion threshold 0.44 GeV/c, kaon threshold 1.54 GeV/c
Photon Detector & Readout Electronics

- 420 x 144-channel Hybrid APDs
  - Custom design with Hamamatsu

  ![Diagram of Photon Detector](image)

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Package</td>
<td>73×73mm²</td>
</tr>
<tr>
<td>sensitive area</td>
<td>64%</td>
</tr>
<tr>
<td># of pixels</td>
<td>144(36 x 4 chips)</td>
</tr>
<tr>
<td>capacitance</td>
<td>80pF</td>
</tr>
<tr>
<td>weight</td>
<td>220g</td>
</tr>
<tr>
<td>peak QE</td>
<td>28%</td>
</tr>
<tr>
<td>bombardment gain</td>
<td>1500</td>
</tr>
<tr>
<td>avalanche gain</td>
<td>~30</td>
</tr>
<tr>
<td>total gain</td>
<td>~45000</td>
</tr>
</tbody>
</table>

- Mergers aggregate data from FEBs to Belle2Link and manage FPGA configuration via JTAG

Front-end Board
- Spartan-6 LX45
- Virtex-5 LX50T

Merger Board
- 5-6 FEBs per Merger
Configuration SEUs in FEB FPGAs

- Spartan-6 devices use Boron as p-type dopant
- $^{10}\text{B} + n \rightarrow ^7\text{Li} + \alpha + \gamma$ (94%) and $^7\text{Li} + \alpha$ (6%)

Previous irradiation tests at the TRIGA reactor of Jožef Stefan Institute (Ljubljana, Slovenia)
- 250 kW research reactor from General Atomics
- $10^7 \text{n/(cm}^2\text{-s)}$ in dry room
- Neutron spectrum similar to Belle II spectrometer
- Extrapolation at Belle II: 8 SEU/h per board, or 3.3 kSEU/h overall

In October 2019 runs, nearly 5% of front-end FPGAs were affected by configuration SEUs in 24 hours
Repairing FEB Configuration On-the-fly

- Star read-out topology
- FEB FPGAs are programmed with the same bitstream => redundancy at system-level

Idea

- Parallel readback of FEB (Spartan-6) configuration from Merger (Virtex-5)
- Real-time 4-out-of-6 bitwise majority voting on JTAG streams (TDOs) for error detection
- Quick single frame reconfiguration for error correction
The Configuration Consistency Corrector - C³

- Features
  - Majority voting configuration of up to 6 FPGAs streams
  - built around Xilinx PicoBlaze6 processor
  - runs at 127 MHz (Belle2Link clock in Merger)
  - 3.3s scrubbing period
  - ~1 ms single frame repair time

- 6 JTAG ports, two IO modes
  1. Single-port Read/Write (used for configuration repair)
  2. All ports Voted Read / Broadcast Write (used for readback)

- BRAMs store
  - Frame buffers (260x8b)
  - Target FPGA frame addressing device-specific information (1252x8b)
  - uP Program (4096x18b)

- 16-bit upset counter for each target FPGA
- UART or JTAG IO for debug/control

• No memory needed for golden bitstream and no a priori limit on # of bitflips per frame that can be repaired
• Xilinx Soft Error Mitigation (SEM) controller in Spartan-6 is limited at 1 bitflip per frame

Architecture derived from
R. Giordano et al., "Configuration Self-Repair in Xilinx FPGAs," doi: 10.1109/TNS.2018.2868992
The Configuration Consistency Corrector – C³ (2)

- Triple Modular Redundancy for logic and scrubbing for BRAMs and scratchpad
- Periodic reset of uP for internal registers cleanup
- Runs in background, no disruption of user design implemented in FPGA
- UART for scrubber control and logging of upsets details
For each upset, the C³ sends a text line on UART with
- unix time stamp, FPGA no., frame address, bit offset(s), polarities

Very useful for testing and debugging, but the same info could be used to study correlations with of upsets to the radiation environment or to reset FEBs only when essential bits are hit.
Implementation

- $C^3$ has a small logic footprint
- In V5LX50T just 828 slices (11%) and 9 BRAMs (15%)

$C^3$ firmware standalone

<table>
<thead>
<tr>
<th>Logic Resources</th>
<th>Used</th>
<th>Available</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slices: FFs</td>
<td>1,068</td>
<td>28,800</td>
<td>3</td>
</tr>
<tr>
<td>Slices: LUTs</td>
<td>2,005</td>
<td>28,800</td>
<td>6</td>
</tr>
<tr>
<td>Slices: overall</td>
<td>828</td>
<td>7,200</td>
<td>11</td>
</tr>
<tr>
<td>BUFGs</td>
<td>3</td>
<td>32</td>
<td>9</td>
</tr>
<tr>
<td>BRAM 36k</td>
<td>9</td>
<td>60</td>
<td>15</td>
</tr>
<tr>
<td>BSCAN</td>
<td>1</td>
<td>4</td>
<td>25</td>
</tr>
</tbody>
</table>
Implementation (2)

• Implementation of Merger firmware w/ C³
• Fits V5LX50T resource availability
  – Slices at 80%, BRAMs at 58%

<table>
<thead>
<tr>
<th>Logic Resources</th>
<th>Used</th>
<th>Available</th>
<th>%</th>
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</thead>
<tbody>
<tr>
<td>Slices: FFs</td>
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<td>51</td>
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<tr>
<td>Slices: LUTs</td>
<td>16,159</td>
<td>28,800</td>
<td>56</td>
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<tr>
<td>Slices: overall</td>
<td>5,977</td>
<td>7,200</td>
<td>83</td>
</tr>
<tr>
<td>BUFGs</td>
<td>10</td>
<td>32</td>
<td>31</td>
</tr>
<tr>
<td>BRAM 36k</td>
<td>35</td>
<td>60</td>
<td>58</td>
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<tr>
<td>BSCAN</td>
<td>1</td>
<td>4</td>
<td>25</td>
</tr>
</tbody>
</table>
Irradiation Test Setup

DAQ Personal Computer handles
- FPGAs Configuration
- C³ Control via UART
- Data readout

Remote terminal on DAQ computer in reactor control room

TRIGA

Reactor Platform

Irradiated setup in dry chamber

6x FEBs

Merger JTAG
Data Readout

Merger JTAG
FEB JTAG
UART

4 10-m CAT6 cables
Cable length dictated by reactor layout

3.8V 1.5V
3.8V 2.0V -2.0V

R. Giordano - RT2020
Dry Chamber

- Prepared two chained trays: one w/ Merger & one w/ 6 FEBs
- Sledge for sliding DUTs in and out irradiation channel for quick irradiation start/stop
- Reactor always on during test
Test Results: Cross Sections

- 29 runs, total irradiation time 14 hours, on average 29 minutes per run

\[ \sigma = \frac{N_{\text{events}}}{\Phi} \]

### Description

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total # of C3 failures</td>
<td>10</td>
</tr>
<tr>
<td>Total # of upsets (bitflips) in 6 FEBs</td>
<td>(3.8 \cdot 10^5)</td>
</tr>
<tr>
<td>Average upsets rate detected by C3 per FEB (1/s)</td>
<td>1.26</td>
</tr>
<tr>
<td>Mean # upsets per FEB</td>
<td>(6.3 \cdot 10^4)</td>
</tr>
<tr>
<td>Total # of upsets Merger</td>
<td>(1.1 \cdot 10^3)</td>
</tr>
<tr>
<td>Mean # of upsets per 6 FEBs between C3 failures</td>
<td>(3.8 \cdot 10^4)</td>
</tr>
<tr>
<td>Mean # of upsets per FEB between C3 failures</td>
<td>(6.3 \cdot 10^3)</td>
</tr>
<tr>
<td>Mean # of upsets per Merger between failures</td>
<td>(1.1 \cdot 10^2)</td>
</tr>
</tbody>
</table>

**Failure cross section**

\[ \frac{\sigma_{C3}}{\sigma_{FEB}} = 1.6 \cdot 10^{-4} \]

**Upset cross section**

\[ \frac{\sigma_{\text{MERGER}}}{\sigma_{\text{FEBS}}} = 1.7 \cdot 10^{-2} \]

Assuming same neutron fluence on merger and FEB.
Impact on Readout: C³ Vs SEM

• Failure defined as readout interrupted or data corrupted
• Two sets of runs
  – A single C³ implemented in Merger
  – A SEM implemented in each FEB (total of 6 SEMs)

<table>
<thead>
<tr>
<th>Test summary</th>
<th>C³ in Merger</th>
<th>SEMs in FEBs</th>
</tr>
</thead>
<tbody>
<tr>
<td># of runs w/ readout testing</td>
<td>13</td>
<td>11</td>
</tr>
<tr>
<td>Test time (h)</td>
<td>8.0</td>
<td>4.8</td>
</tr>
<tr>
<td># of read out failures</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>Average upset rate per FEB (1/s)</td>
<td>1.26</td>
<td>1.26</td>
</tr>
<tr>
<td>Readout MTBF (s)</td>
<td>2.2×10³</td>
<td>1.7×10³</td>
</tr>
<tr>
<td>Readout MTBF (upsets)</td>
<td>2.8×10³</td>
<td>2.2×10³</td>
</tr>
</tbody>
</table>

\[
\frac{MTBF_{C³}}{MTBF_{SEMs}} = 1.3
\]

30% improvement moving from SEM to C³
Upset Correction Capability: $C^3$ vs SEM

- Residual upsets in FEBs at the end of the run
- SEM lets upsets accumulate over time
- $C^3$ avoids accumulation
  - Small amount residual related to stop (or failure) of $C^3$ at the end of the run before verify
Number of Upsets per Frame

- Distribution of the number of bitflips per frame (multiplicity) in each SEU event detected by C3
- Average multiplicity 2.24 upsets per SEU event
- 65% of events have multiplicity > 1 (not correctable by SEM)
- Total events 165k
- Includes also few tens of events w/ up to 256 flips, likely configuration SEFIs

Notice the log scale
Integration in Belle II

- $C^3$ fully integrated and running in Belle II TDAQ since the middle of 2020 spring run
- SEUs monitored via EPICS slow control system
  - Detected SEU map and SEU trends related to last two weeks of 2020 spring run
  - Up to 20 SEUs per FEB group
- FEB firmware is now robust against SEUs, in the view of SEU rate increase with the foreseen SuperKEKB luminosity increase $(2 \cdot 10^{34} \rightarrow 8 \cdot 10^{35} \text{ cm}^{-2} \text{ s}^{-1})$
Conclusions and...

- Developed a scrubber (\(C^3\)) to majority vote configuration across FPGAs connected in a star topology
- Fast detection by means of parallel readback and correction by partial reconfiguration
- Completed a radiation test at a nuclear reactor
- Results show
  - \(\sigma\) of upsets in Merger almost two order of magnitude lower than in FEBs
  - \(\sigma\) of failures in \(C^3\) almost four orders of magnitude lower than upset \(\sigma\) in FEBs
  - \(C^3\) limits accumulation of upsets in configuration memory and improves MTBF of data read out w.r.t. Xilinx SEM by 30%
  - No hard failures of Merger (Virtex-5) or FEBs (Spartan-6)
- System installed and fully operational in Belle II
…Acknowledgments

- We wish to thank
  - A. Boiano, A. Vanzanella, A. Pandalone, E. Masone from SER (Electronics and Detectors Service) of INFN Napoli for their technical support to this activity

- JSI TRIGA staff for their technical support during the irradiation test