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Clock-centric Serial Communication Links for the Synchronization of Distributed Readout Systems

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Detector readout systems for medium to large scale physics experiments, and instruments in some other fields as well, are generally composed of multiple front-end digitizer boards distributed over a certain area. Often, this hardware has to be synchronized to a common reference clock with minimal skew and low jitter. These front-end units usually also need to receive messages synchronously, for example trigger information. The high speed serial transceivers (a.k.a. SerDes) embedded in modern Field Programmable Gate Arrays (FPGAs) are primarily meant for moving large data volumes, but a reference clock can also be propagated via their serial clock. While using the SerDes clock recovery technique to transport synchronization over fast serial links has now become a mainstream solution, it has some limitations. An alternative option uses distinct clock and data links. This can potentially reach higher synchronization accuracy, at significant hardware expenses. This work reports some first steps to explore a third scheme for clock and synchronous message distribution. Like the standard approach, the same media is used to convey clock and data, but instead of using today's "data-centric" links where the recovered clock is only a by-product of a SerDes, this paper defines and investigates "clock-centric" links where, at the opposite, a clock is carried by the link, and synchronous data are embedded into it by a modulation technique. After defining the concepts and principles of data-centric links, experimental studies are presented. Finally, the merits and limitations of the proposed approach are discussed.

Minioral

Yes

IEEE Member

No

Are you a student?

No

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