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# A reconfigurable digital dataflow controller for large-scale pixel arrays with power-efficient RISC-V core

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In high energy physics experiments, large-scale pixel arrays are desired because of the requirements in accurate measuring time and position in the effective detector range. When pixel detectors form a unified module in a limited area, multi-controller interconnections and pixel array control interfaces become the bottlenecks to prevent application of larger pixel arrays. This paper proposes a reconfigurable digital readout system to overcome this problem. The controller includes three parts: Core module, communication interface and pixel scanning array. The core module of the controller uses a compact and power-efficient CPU with the RISC-V instruction set. The communication interface is capable of data exchange and programming between core controllers. The pixel scanning array implements the digital logic for readout and supports up to 256x256 pixels. The power supply voltage, scanning area, and pixel threshold can be configured according to the requirements in different situations. This feature improves the system compatibility and reduces the power consumption when operating under low voltage. When scaling up to a large array of pixels, multiple controllers can be connected using a daisy-chain topology through the stitching technology without changing the definition of the ports. The prototype has been set up and verified by simulation successfully. The core is taped out using a commercial 130nm CMOS process.

## Minioral

Yes

## IEEE Member

No

## Are you a student?

Yes

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