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PCI-express based high-speed readout for the Belle II DAQ Upgrade

Friday, October 23, 2020 1:20 AM (20 minutes)

Belle II is an experiment dedicated to explore the new physics beyond the Standard Model of elementary particles at the beam intensity frontier, SuperKEKB accelerator, which is located at KEK, Japan. Belle II has started data-taking since April, 2018, with a synchronous data acquisition (DAQ) system based on a pipelined trigger flow control. Belle II DAQ system is designed to handle 30 kHz trigger rate with about 1% dead time under the raw event size more than 1 MB. It is a big challenge to maintain the DAQ stability under the requirement in a long term with current read out system, meanwhile, the readout system also becoming a bottleneck for providing higher speed data transfer. A solution of PCI-express based readout module with data throughput as high as 100 Gbps, was adopt for the upgrade of Belle II DAQ system. We focus on in particular the design of firmware and software driver based on this new generation of readout board called PCIe40 with an Altera Arria 10 FPGA chip. 48 GBT (Gigabit transceiver) links, DMA mechanism, interface of Timing Trigger System, as well as the slow-control system have been designed for integrating with current Belle II DAQ system. We present the development of firmware and software for the new readout system, and the test performance with pocket Belle II DAQ, specifically involve the FrontEnd Electronics of Belle II TOP sub-detector.

Minioral

No

IEEE Member

No

Are you a student?

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