Advanced Gamma Tracking Array Project

40 Gbps Readout interface STARE for the AGATA Project

Serial Transfer Acquisition and Readout over Ethernet

AGATA project
- 150 segmented crystals (50 triple clusters)
- 362 kg of Ge
- 82% solid angle
- 58 millicrystal counting rate
- Data reduction from 14.4 TBps to 40 TBps/week
- Energy resolution 5% range: 0.2% (5 keV-180 MeV)
- Angular resolution: ~1'1
- Efficacy: 25% M=4; 17% M=30%
- Higster: 6/10 (0.9); 4/4 (0.8)
- Medium detector
- Large fan-in box to accommodate auxiliary devices

36-Fold segmented HPGe Detector signal processing
- 100 kHz 14-bit sampling FADC per segment 3.8 MBps/kch 44 Gbps @ 2GHz
- Online parallel data re-processing of the 32 channels
- Readout data rate to STARE 10 to 10 Gbps
- Monitoring and diagnostic data rate to STARE 10 Gbps
- A 4-10 Gbps link data distribution from the STARE to Computer farm.

STARE Characteristics
- FMC (PCIe Module Card) standard board
- Input data rate from pre-processing: 4 x 10 Gbps (2 for data 1 for monitoring 1 spare)
- 2 Power supply sources (internal and external PSU using hot swap max)
- Spare USB-10 with the pre-processing for future use
- Full clock management for the SOM and the FMC carrier
- Network Bandwidth up to 6 x 10 Gbps in parallel
- Reliability UDP protocol with 5% data loss using external Memory data rate @ 10 Gbps
- Transmitting side uses Selective Repeat Protocol with stopping mechanism and sending side timeouts.
- Receiving side algorithm using AXI (package received) and NACK (package lost) messages.
- 1 Gbps (FPGA Interface for slow control)
- On board facilities to make diagnostics and SPF data (raw data storage, local histograms, built in self test etc...)

The STARE Concept
- Decoupled the custom hardware from the server farm
- Input through FMC
- 4 Transceivers
- 20 USB links
- Ethernet output
- 4 FIFO links
- UDP Transport
- IPless slow control

STARE FPGA Architecture

Frame life External Memory Interface and the RUDP Core Algorithm.

First Results of the Receiving Selective Repeat Protocol algorithm, Rate was limited by the server lack of computing power

Transmitting and Receiving Selective Repeat Protocol architecture and Algorithm

Attempts were also made to increase the bandwidth further. Unfortunately the implemented Data Generator has no steps between 5Gbps and 10Gbps. When tested at 10Gbps the software only re-reported a total transfer rate of around 6Gbps. At the same time the monitors in the firmware report that the full link capacity was used. The reason for this is most likely that the server is unable to process the incoming data.

A more optimised software is therefore needed to make a final evaluation of the performance of the Selective Repeat protocol implementation. The current software could however prove that no errors occurred during transfer and showed clear signs that the implementation could reach higher speeds.