

Application of heterogeneous computing techniques for image-based hot spot detection

V. Costa, S. Esquembri, J. Nieto, A. de Gracia, A. Carpeño, M. Astrain, M. Ruiz
 s.esquembri@upm.es
 Instrumentation and Applied Acoustic Research Group,
 Universidad Politécnica de Madrid (UPM), Madrid, Spain

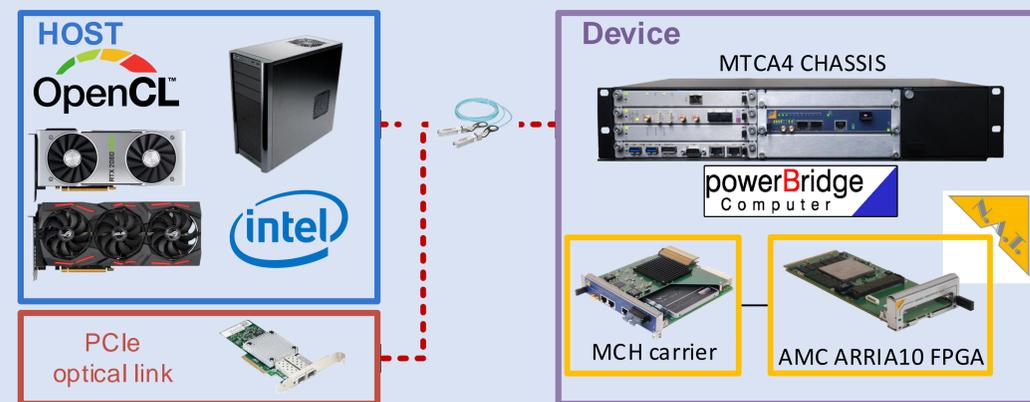
BACKGROUND

- Computer vision (CV) is a technology currently used in numerous environments.
- There are multiple frame grabber solutions capable of high throughput. (1/10 GigE Visio, Cameralink, etc.)
- Computer vision algorithms can be run on multiple platforms and devices (FPGAs, GPUs, CPUs).
- Connected Component Labeling (CCL) is a computer vision algorithm capable of extracting a set of pixels which are connected in an image.
- OpenCL offers a standard which makes easier to develop heterogenous computing systems.

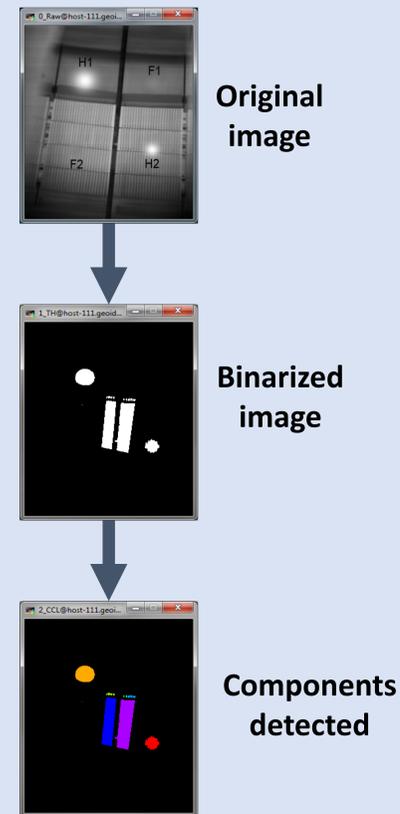
OBJECTIVES

- Create an heterogenous architecture capable of process computer vision algorithms used in fusion environments like hot spot detection.
- Modularize the CCL algorithm
- Propose execution flows using different platforms and devices.
- Analyze performance using synthetic image testbench.
- Compare the results.

ARCHITECTURE



PROCESSED IMAGE STATES

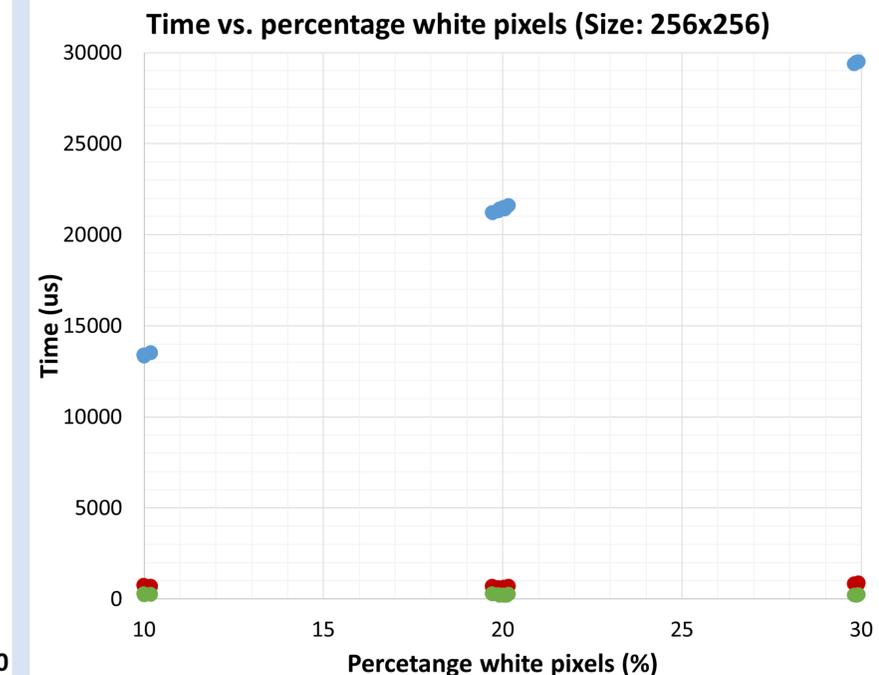
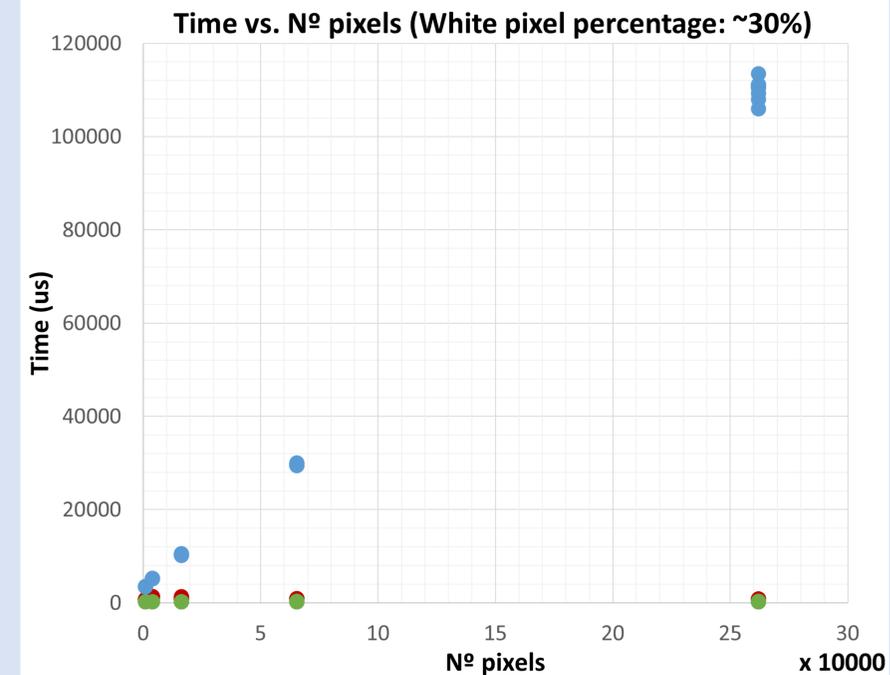


TESTS

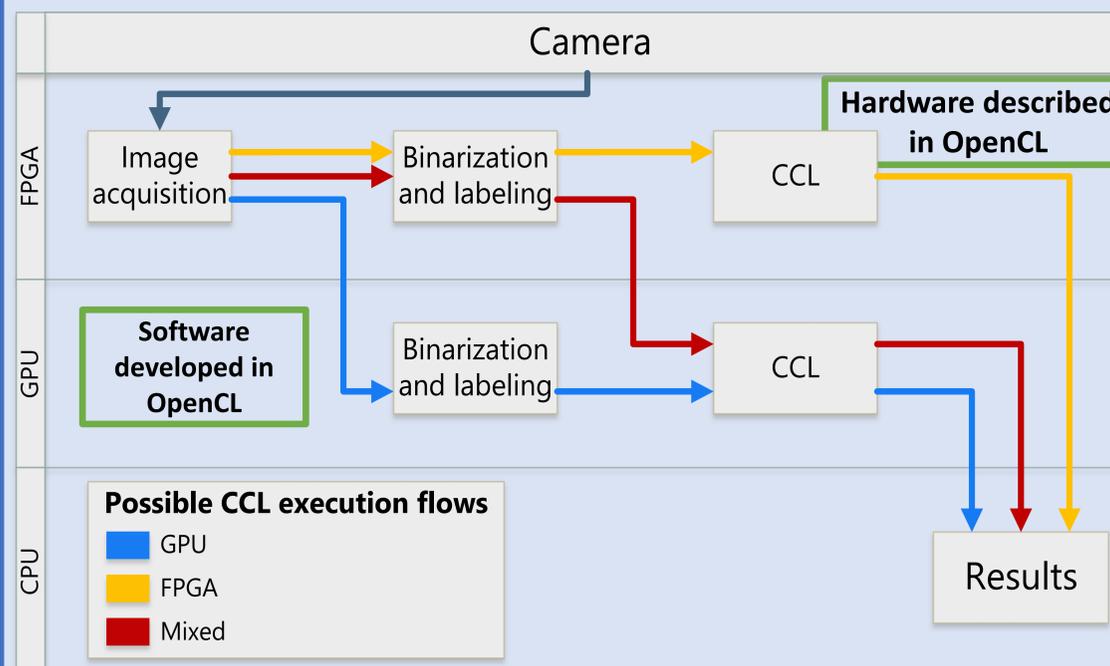
- Synthetic images composed of black and white pixels placed randomly.
- From densities of 10% white pixels up to 30%.
- Sizes from 32x32 to 512x512. (Due to memory limitations on the FPGA)
- Repeated 1000 times in each device

Legend for performance graphs:
 ■ FPGA (Blue)
 ■ AMD RX 5600 (Red)
 ■ NVIDIA RTX 3080 SUPER (Green)

*FPGA running at 146.07 MHz



POSSIBLE EXECUTION FLOWS



CONCLUSION

- Currently there are no modules available that integrates a GPU for data acquisition platforms (such as PXIe or MTCA). This result in a time loss as the data must pass through some other interface before it reaches the GPU. Due to this, if an FPGA would be used for data acquisition (in this case image acquisition), binarizing and labeling the image in the FPGA as the pixel arrive would result in a time improvement of the whole system without adding latency due to the simplicity of the operations.
- Using an FPGA results in a lower power consumption.
- OpenCL makes easier testing different execution flows due to only using one programming language.

ACKNOWLEDGEMENTS

This work was supported by: the Spanish Ministry of Economy and Competitiveness, Project N° ENE2015-64914-C3-3-R ; Spanish Education Ministry Mobility grant number PRX19/00449 and Comunidad de Madrid grant number PEJ-2019-AI/TIC-14507 (Ayudante de investigación)