Institute for Hadronic Structure and Fundamental Symmetries Physik Department Technische Universität München

Performance of the DHH readout system for the Belle-II pixel detector Stefan Huber*, Igor Konorov, Dmytro Levit, Stephan Paul

Belle-II pixel detector

- thickness: 75 mm
- rolling shutter read-out integration time: 20 ms
- 2 layers consisting of in total 40 half-ladders
- 4 digital data processors per half-ladder zero suppression pedestal and common mode correction •4 x 1.2 Gb/s optical links
- High occupancy (max. 3 %) \rightarrow high date-rate in total 20 GB/s

Crosspoint switch

- Allows to map any sensor to any DHE
- Check optical power from the detector
- Change over to spare module without access to radiation area
- Fanout feature \rightarrow independent verification of data flow
- Configurable load-balancing between different DHHs

DHE

- Receiver for detector data
- Accepts data which corresponds to triggers
- Long integration time + high trigger rate Several trigger per detector frame
- DHE splits and copies data in order to have full frames for every trigger
- Formatted data sent further to DHC

20us Frame M Frame M+1 Frame M+2 Frame M+3 DHPT data Ev.N+3 Ev.N Ev.N+1

Ev.N+2

Pixel Data Back Pressure

Data format after processing overlapping triggers Ev.N+1 Ev.N+2 Ev.N+3 Ev.N





Unified Communication Framework

- Single high-speed serial link for data, slow control, trigger, and timing information
- Three different communication channels used (Trigger, Data, Ethernet)
- Fixed latency for one channel



- Priority handling for all channels
- Self recoverable after connection losses
- Independent from physical layer





DHC

- Master module in one ATCA carrier
- Interface to the Belle-II trigger and timing system
- Ethernet hub
- UCF speed currently 2.5 Gbit/s
- UDP interface for monitoring data







• Distribution of control signals to 5 DHEs and one DHI

Event-building of data from 5 DHEs via DDR3 memory

• Round-robin event distribution via 4 6 Gbit/s Aurora links

FTSW Backpressure	TRG FIFO		
DHE BUFFER	DDR3 WRITER		ONSEN
DHE BUFFER	DDR3 WRITER		DDR3 READER0
DHE BUFFER			DDR3 READER2
DHE BUFFER	DDR3 WRITER	Y	DDR3 READER3
DHE BUFFER	TRG FIFO DDR3 WRITER		
SEL	ECT DESTINATION		

CLK Fanout+ **CLK Synthesi**



DHI



Galvanically isolated control signals

- JTAG for detector configuration
- Manchester encoding for real-time signal Sync, trigger, synchronization and veto

0 50 100 150 200 column

Power for optical transmitters

Switching off gated-mode

Gated mode

- High background after freshly injected bunch Switching on gated-mode
- Veto signal from DHI
- Sensor stores currently accumulated charge Sensor does not collect new charge
- Baseline oscillations while switching on and off gated mode Inhibit trigger signal during that time
- Functionality proven and noise reduction seen in the experiment
- Baseline fluctuations to be understood before final commissioning

Performance

- DHH running stably with 20 sensors attached
- Currently operation at low trigger rates (<5 kHz)
- Maximum trigger rate limited by UCF link speed ~20 kHz @ 3% occupancy

System capable of handling 20 GB/s



Outlook

- Install full system (40 sensors / 8 DHHs)
- Change UCF to 5Gbit/s links
- Commission gated mode
- Replace UDP for local DAQ by PCIe readout
- Online clustering

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