Abstract

We present the design principle and test results of a data transmitting ASIC, GBS20, for particle physics experiments. The goal of GBS20 will be an ASIC that employs two serializers each from the 10.24 Gbps IgBT SerDes, sharing the PLL also from IgBT. A PM4 encoder plus a VCSEL driver will be implemented in the same die to use the same clock system, eliminating the need of CDRs in the PM4 encoder. This way the transmitter module, GBT20, developed using the GBS20 ASIC, will have the exact IgBT data interface and transmission protocol, with an output up to 20.48 Gbps over one fiber. With PM4 embedded FPGAs at the receiving end, GBT20 will halve the fibers needed in a system and better use the input bandwidth of the FPGA.

A prototype, GBS20v0 is fabricated using a commercial 65 nm CMOS technology. GBS20v0 is tested barely up to 20.48 Gbps. With lessons learned from this prototype, we are designing the second prototype, GBS20v1, that will have 16 user input data channels each at 1.28 Gbps. We present the design concept of the GBS20 ASIC and the GBT20 module, the preliminary test results, and the design of GBS20v1 which will be not only a test chip but also a user chip with 16 input data channels.

Introduction

In particle physics experiments, especially those on the Large Hadron Collider (LHC), high-speed data transmission still faces many challenges. The state-of-the-art in detector data transmission is the IgBT [1] SerDes ASIC and the VTRx+ [2] optical transceiver working up to 10.24 Gbps per fiber. And at the given size of the experiments, VL+ uses 150 m as the default length for the selected fibers, and the data rate of 10 Gbps is near the maximum on present transmission distance. The idea of GBS20 grows from the success in LOCx2 in which two serializers share one PLL. GBS20 output goes directly to a VCSEL, making it possible to build the optical transmitter mezzanine with the serializer ASIC. This module, called GBT20. With all these improvements, the GBS20 ASIC and the GBT20 module are aimed to double the bandwidth in data transmission, which will reduce cost of the optical transmitter mezzanine with the serializer ASIC. This module, called GBS20, for particle physics experiments. The goal of GBS20 will be an ASIC that aims to double the bandwidth in data transmission, which will reduce cost of the optical transmitter mezzanine with the serializer ASIC. This module, called GBS20, for particle physics experiments.

GBS20V0 Test Results

GBS20v0 is fabricated in a 65 nm commercial CMOS technology and tested up to 20 Gbps. The measured PM4 electric output is shown in Fig. 5 and Fig. 6. The power supply is chosen to be 1.2 V and this is found to limit the dynamic range of the PM4 driver. When we set a fixed 2:1 ratio of the MSB and LSB inputs to the encoder, we observe significant nonlinearity in the MSB amplitude, which is partially due to a mistake in the layout. The CTLE technique further cuts into the dynamic range of the MSB amplifier. Because of these design issues, plus a few other mistakes in the layout that contribute to power noise, we decide not to continue the test with a VCSEL. Instead we move on to the next ASIC prototype design work.

GBS20V1 Design

Taken the lessons from GBS20v0, we are implementing the following changes in GBS20v1: the PM44 stage will operate under 2.5 V to increase the modulation current and leave more headroom for the CTLE bandwidth extension. The gain control to the MSB and LSB amplifiers will be independent from each other. The inductance peaking in the output driver is stronger than before.

GBS20V1 Test Results

The PAM4 electric output from GBS20v0 at 16G and 20G. The PAM4 electric output from GBS20v1 at 20G.

Conclusions

We present the new concepts employed in the R&D of the GBS20 ASIC and the GBT20 transmitter mezzanine with a goal to reach 20.48 Gbps per fiber using PM4 for detector data transmission in particle physics experiments. Test results from the first prototype indicate a speed barely at 20.48 Gbps and revealed several design faults that are to be corrected in the second prototype. Taken the lessons from GBS20v0, we are working on the next prototype GBS20v1, with an aim to submit in November 2020. This R&D using a 65 nm CMOS technology may also serve as guineapig of PM4 in radiation environment for higher data rates using more advanced CMOS technologies in the future.

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References


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