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Short Course: Achieving High Performance Using Low Tech - Topics and Examples on FPGA and ASIC TDC

Tuesday, October 13, 2020 4:45 PM (1 hour)

Silicon technologies have been constantly progressing but intrinsically they will never satisfy demands of performance in HEP projects, so that current available technologies with reasonable cost can always be considered low tech. In our daily design jobs, however, there are rooms for the designers to put in various good thinking to eliminate unnecessary elements or operations which will dramatically reduce silicon area, power consumption and costs for given requirements. Such improvements may enable functionalities that otherwise would be impossible.

The development of FPGA TDC was based on its forerunner developed in ASIC and the TDC implemented using FPGA platform was considered problematic. The limitation of available circuits in FPGA forced the TDC designers to choose unadjusted delay lines with uneven bin widths while calibrating the bin widths using measurement data, which is an approach deviated from its counterparts in ASIC. The approach of using unadjusted delay lines succussed in FPGA platform after efforts of hundreds of developers worldwide in past decade. Today the approach has been transplanted back into AISC TDC and finest bin width allowed by certain technology has been achieved along with significant power reduction.

In this presentation, I will discuss several topics in digital designs including silicon resource saving, power consumption reduction, timing uncertainty confinement, etc. using examples seen in TDC and other digitizers. The discussion will cover several practical building blocks such as digital delay lines, adjustable gated ring oscillators, coarse time counter and data readout circuits.

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